Design of Supply Regulators for High-Efficiency RF Transmitters

Jose Silva-Martinez[1], *Fellow, IEEE*, Bertan Bakkaloglu[2], *Fellow, IEEE*, Sayfe Kiaei[2], *Fellow, IEEE*, Tanwei Yan[1], *Student Member, IEEE,* Zhiyong Zhang[1], *Student Member, IEEE,* and Parisa Mahmoudidaryan[2], *IEEE Member.*

Abstract: The increasing performance demanded by emerging wireless communication standards motivates the development of various techniques devoted to improving the efficiency of power amplifiers (PA) because this is one of the most power-demanding blocks in RF transceivers. Power-amplifier efficiency is proportional to the ratio of the average voltage delivered by the PA to the voltage level of the PA's power supply. Efficiency is affected by the peak-to-average ratio of the transmitted signal. The envelope tracking modulator maximizes this ratio, correlating the PA's power supply with the envelope of its output signal. Efficient modulators must satisfy certain critical conditions: i) it must be very agile to track the amplitude variations of PA's output voltage; ii) it must reduce the timing mismatch between the PA modulator's supply and PA output waveform envelope to optimize power efficiency and avoid PA saturation, and iii) the envelope tracking modulator must be highly power efficient.

This paper reviews several relevant envelope tracking techniques. Hybrid modulators consisting of switching regulators and linear amplifiers have become mainstream envelope tracking systems for wideband applications, in which linear amplifiers complement the functionality of highly efficient but narrow bandwidth switching modulators. Replacements for linear amplifiers include a combination of power-efficient ADC and DACs that provide very agile feedback, increasing the system's slew rate, which allows the modulator to track faster envelope signals. Multi-level switching is another relevant approach utilizing multiple switching voltages to reduce current ripples and enable the use of wider bandwidth switching regulators with high power efficiency. The use of multiple inductors is another interesting approach. Multi-phase switching techniques utilize multiple switching stages in a time-interleaved manner to extend the switching modulator's bandwidth. A slow buck converter can be combined with a fast buck converter and optimized for different switching frequencies; this architecture covers the signal envelope's low- and high-frequency components.

The approaches mentioned use switching modulators with analog feedback controllers (Pulse-width modulation [PWM] or hysteretic). However, an alternative approach is prediction-based digital feedforward control. This tutorial discusses all of these approaches.

1. Introduction

Recent developments in mobile computing and wireless internet have led to increasing demand for portable devices and smartphones equipped with wireless local area networks (WLAN) operating with multi-standard capabilities. More standards and applications will soon be incorporated because minimum

[1] Manuscript received June 23rd, 2022.
This work was partially sponsored by National Science Foundation under contract ECCS-2123625.
Jose Silva-Martinez, Tanwei Yan and Zhiyong Zhang are with the ECE department, Texas A&M University, College Station, Texas, USA. (e-mail: {jose-silva-martinez, ytw9429, hzzy}@tamu.edu)
Bertan Bakkaloglu and Sayfe Kiaei are with the School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, Arizona, USA. (e-mail: **bertan.bakkaloglu@asu.edu**). Parisa Mahmoudidaryan was with the School of Electrical, Computer and Energy Engineering, Arizona State University; she is currently with Qualcomm.

feature size transistors in nanometer CMOS technologies allow more devices on a single chip with massive digital signal processing capabilities [1]. Fig. 1 shows the current and predicted market for connected smart devices, reaching over 75 billion by 2025. The estimated number of connected smart devices will increase by 500% from 2015 to 2025. Each one of these devices requires at least one RF transceiver. Thus, the design of power-efficient RF front ends is a primary concern for the telecommunication and consumer electronics industries.

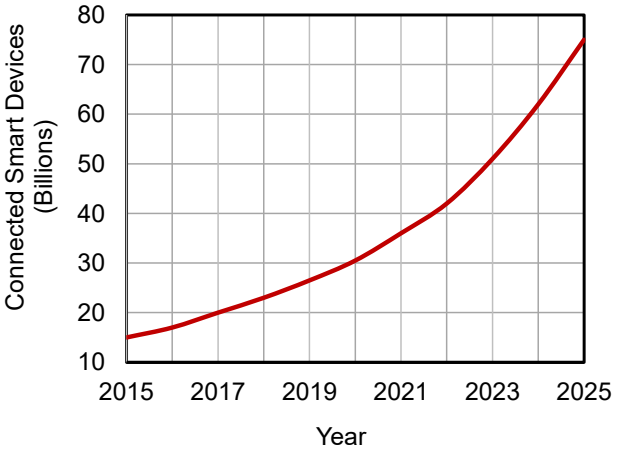


Fig. 1. Connected Smart Devices and predictions till 2025. Source: Statista 2018.

The sixth generation (6G) of wireless systems will demand more bandwidth and more efficient use of the spectrum to satisfy the demand for faster and more reliable communication systems. Emerging applications will demand effective signal bandwidths over 160MHz for in-house short-range communications. Mm-Wave communication systems will demand even larger effective signal bandwidths.

To increase the spectral efficiency of the communication systems, complex digital-domain modulation schemes such as OFDM are becoming necessary; in these modulation schemes, both amplitude and phase are modulated [2-4]. As a result, the signal envelope presented to the PA is not constant; and the signal's peak-to-average power ratio (PAPR) increases significantly [5]. IEEE 802.11ax (Wi-Fi 6) enables gigabit wireless communication and allows enterprise and service providers to support emerging applications while maintaining legacy services. IEEE 802.11ax supports more customers in complex environments and provides superior performance for advanced applications such as high-definition video, faster wireless office services, and more options for Internet of Things (IoT) applications. This standard's benefits come at the expense of more demanding hardware specifications: i) more spectral efficient modulation schemes such as 1024 Quadrature Amplitude Modulation (QAM) are employed; ii) this standard takes advantage of the properties of the Orthogonal Frequency Division Multiple Access (OFDMA) modulation schemes to increase system robustness and spectrum efficiency; iii) IEEE 802.11ax OFDMA technology supports up to eight spatial streams and delivers up to 4.8 Gbps at the physical layer. Wi-Fi 6 supports bandwidths up to 160MHz and transmit average power can be as high as +23dBm while maintaining the constellation's quality with error vector magnitude (EVM) under -43dB. However, the broadband QAM-1024 standard is sensitive to transmitter and receiver magnitude and phase errors. Consequently, RF front-end linearity requirements increase. The effects of noise leakage due to noisy power supplies are more critical in this case.

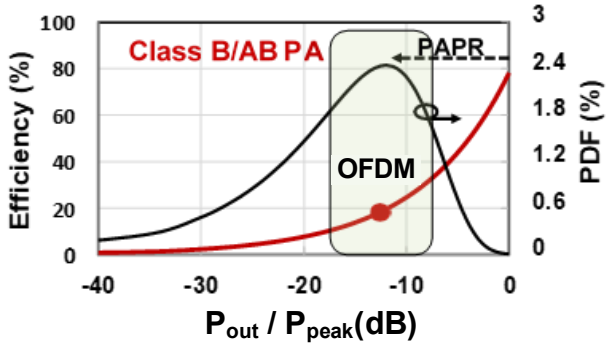


Fig. 2. Power Efficiency of class-B Power Amplifier and Power Density Function for a typical OFDM signal.

Fig. 2 illustrates a typical OFDM signal's probability density function (PDF). The x-axis is the output power normalized to the peak power. The PDF peaks at around -12 dB from the peak output power value, but the peak value varies for different modulation schemes. Most of the time, the PA output

is within the 6–30 dB back-off power range. It is highly advisable to optimize the PA power efficiency in that range. Fig. 2 also shows that the ideal peak drain efficiency of a class-B amplifier is about 78.5%, but at 10 dB back-off, its efficiency drops below 25%; the amplifier's drain efficiency is under 8% for -20 dB back-off power, which makes it evident that the PA power efficiency increases as the signal amplitude comes closer to the value of the power supply.

The organization of this tutorial is as follows: Section II revisits the design issues and limitations of the power amplifier and discusses correlating the PA's supply with the envelope of the transmitter output signal. Sections III and IV discuss the fundamentals of hybrid envelope tracking modulators combining linear amplifiers and switching modulators. Section V covers recently reported solutions. Section VI discusses the mismatch issues when accommodating a PA with an envelope tracking modulator and how to calibrate it. The last section provides conclusions.

II. Fundamentals of Envelope-Tracking Modulators

Properties of RF Power Amplifiers. A PA's efficiency is especially critical for mobile communications systems that require low-power consumption for increased battery life and reduced size, weight, and cost. The efficiency of linear PAs reaches its maximum at the peak output power and then drops when operating at power back-off (PBO) regions. Ideally, the inductor/transformer terminated class-A amplifier's power efficiency is limited to 50%. At 10 dB back-off power, the expected power efficiency is around 15% and less in practice due to the transistor's voltage headroom requirements. A class-B amplifier's efficiency is proportional to (π/4)*(Vout/VDD), leading to a peak-drain efficiency of around 78%; for 10 dB back-off power, the drain efficiency will usually drop to under 26% [3]. In practice, the conventional class-A and class-B PA architectures achieve drain efficiencies of less than 10% and 15%, respectively, at 10 dB back-off power [3-4], which drastically reduces the talking time in handheld devices.

There are different techniques to increase the efficiency of linear PAs. Doherty's technique increases the efficiency by active load-line modulation and providing optimum PA loading for different input signal levels [6]. The Doherty PA's matching network and load-modulation circuit are frequency dependent and limited to narrow-band applications with a fixed center frequency. The out-phasing technique finds use where the input signal has two constant-amplitude, phase-only modulated signals, thus maintaining the PA near compression to operate more efficiently [7, 8]. The nonlinear mapping from a complex signal to the two-phase domain-only signals will cause significant out-of-band spectral regrowth, which will not only demand a wider bandwidth for the two amplifying paths but also contaminate the output signal for any mismatch between the two paths, so it is challenging to apply this technique for wideband applications.

A highly efficient supply modulator controls the PA's envelope. The polar technique, also known as envelope elimination and restoration (EER), is an effective supply modulation method that separates the RF phase and envelope [9, 10]. This method is highly effective for low and medium bandwidth applications. If phase and envelope signals experience different delays, non-linearity and spectral regrowth will arise; then, precise timing alignment mechanisms are necessary. The timing mismatch is critical for broadband applications.

Switching-mode class-D or class-E amplifiers offer the best possible power efficiency. However, they may not be suitable for broadband and demanding specifications with EVM figures under -40 dB. In this tutorial, we focus on linear power amplifiers.

Envelope Tracking Modulator: Principle of Operation. The envelope-tracking supply modulator (ETM) has gained attention for wideband applications as it utilizes a linear PA and the information employs a single RF path, so the calibration scheme for timing mismatch between envelope and RF path is simpler [11-14]. In a PA employing an envelope tracking engine, the power supply is adjusted to the minimum voltage level needed for linear operation; this approach takes advantage of the fact that the RF PA's gain presents minor sensitivity to baseband drain-voltage variations. The ETM concept is illustrated in Fig. 3. In this method, the envelope signal is extracted in the digital domain and used to bias the PA using a highly efficient supply modulator. It is necessary to ensure a good match between the output of the envelope tracking modulator and the PA's drain voltage. Two main issues can be identified for this technique to be practical and to maintain PA linearity properties: i) the output of the envelope modulator must follow the PA drain voltage swing, which demands a measurement (or an accurate predictor) of the PA's RF power gain; and ii) timing offsets between the ETM signal and the PA drain envelope signal must be minimized.

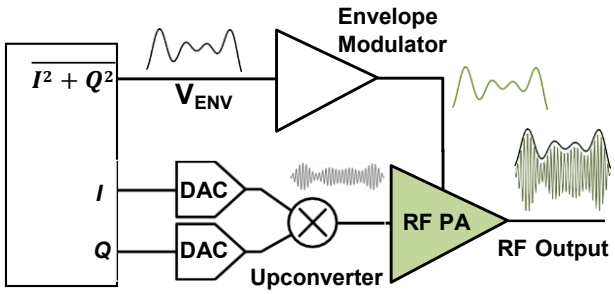


Fig. 3. Typical RF transmitter with Envelope Tracking Engine.

III. Envelope Tracking Modulator

Supply Modulator based on a switching modulator. The simplest envelope tracking modulator employs a power-efficient switching regulator [15]. The RF path is initially characterized to evaluate the voltage gain and propagation delay. The delay mismatch between the ETM and the signal path is equalized using a programmable delay element, as depicted in Fig. 4. The envelope of the digital input signal is then extracted and converted to analog format; the PGA (programmable gain amplifier) is used to adjust the ETM output to the PA's output magnitude.

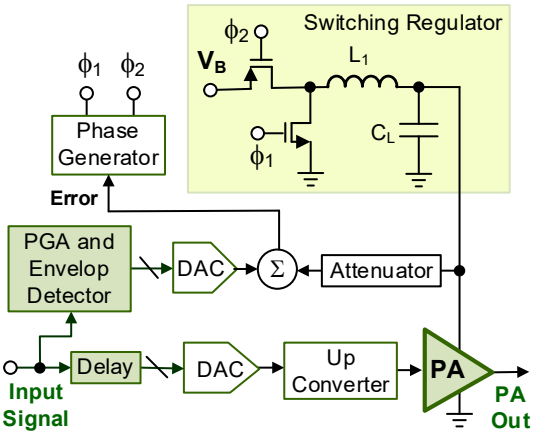


Fig. 4. Basic envelope tracking system employing a conventional switching regulator.

The ETM output voltage is monitored and compared with the adjusted input signal's envelope to generate the error function, which controls the duty cycle of the switching regulator's clock phases ϕ_1 and ϕ_2. The phase generator block employs a loop filter with high gain and a pulse-width-modulator (PWM) engine that adjusts the clock phase's duty cycle. The output voltage of the power-efficient switching modulator then tracks the PA's output envelope within its frequency range.

Switching Modulator's Tradeoffs. A significant limitation of this technology is that power-efficient switching regulators cannot efficiently track fast signal variations simultaneously with low ripple. Fast loops are required to reduce the LC product, while low-ripple solutions demand large LC products. Smaller inductors generate higher current because the current is inversely proportional to L, while smaller capacitors require less current to quickly charge/discharge it, making the LC network more agile. For the case of a

buck converter, it can be shown that the normalized voltage ripple during the steady state is computed (approximately) as follows:

$$\frac{\Delta v_{DD}}{V_{DD}} = \frac{(1-D)}{16LCf_{sw}^2} \tag{1a}$$

Note that D is the duty cycle of the clock signals driving the modulator's clock phases ϕ_1 and ϕ_2. In this equation, f_{sw} is the clock frequency used in the phase generator. According to eqn (1a), a large LC product reduces the normalized output ripple. Notice that the worst case happens when D=0.5. That usually happens when the output voltage is around mid-rail, e.g., -6 dB back-off power. Another interpretation of this result is obtained by replacing the LC product with the resonant frequency of the tank:

$$\frac{\Delta v_{DD}}{V_{DD}} = \left(\frac{(2\pi)^2(1-D)}{16}\right)\left(\frac{f_0}{f_{sw}}\right)^2 \; ; \quad \omega_0 = 2\pi f_0 = \sqrt{\frac{1}{LC}} \tag{1b}$$

Hence, a small output ripple requires that the ratio of the LC resonant-frequency to clock-frequency $\frac{f_0}{f_{sw}} \ll 1$. For the worst case in eqn. 1b (D=0.5) the normalized ripple is under 4% if $f_{sw} > 5f_0$. For broadband input signal, the resonant frequency f_0 is placed at even higher frequencies, and so is the clock frequency. Signal bandwidth of 160 MHz may require placing f_{SW} close to or above 1 GHz. Switching losses for GHz range clock frequencies may be excessive since switch dimensions become large to reduce switch resistance. Hence, the switching modulator is not efficient for emerging broadband applications and cannot track fast signal variations with reduced voltage ripple. Recent approaches that overcome this limitation are discussed in the following sections.

Most modern wireless standards require PAPR even over 12 dB. The peak of the probability density function of the transmitted power is in the back-off region, where the signal amplitude is around 25-50% of the peak value. A fast variation in the envelope signal is infrequent, but it happens and must be driven by the ETM. The governing equation step response of the LC network is given by:

$$v_O(t) = V_{BAT}\left(\frac{s_2 e^{s_1 t} - s_1 e^{s_2 t}}{s_1 - s_2} + 1\right) - v_O(0)\left(\frac{s_2 e^{s_1 t} - s_1 e^{s_2 t}}{s_1 - s_2} + \frac{e^{s_1 t} - e^{s_2 t}}{RC(s_1 - s_2)}\right) + \frac{i_L(0)}{C\,(s_1 - s_2)}\,(e^{s_1 t} - e^{s_2 t}). \tag{2}$$

The initial condition in the capacitor and inductor are modeled by $v_0(0)$ and $i_L(0)$. The solutions of the resulting homogenous equation $s_{1,2}$ are given by:

$$S_{1,2} = -(1/2RC) \pm \sqrt{(1/2RC)^2 - (1/LC)} \tag{3}$$

The rising (or falling) time can be calculated with the help of (2) and (3), but the resulting expression is complex and cumbersome; simulation results can be used to estimate the regulator's slew rate and rise time. Details can be found in [16, 17]. Note that the current delivered by the inductor is computed as:

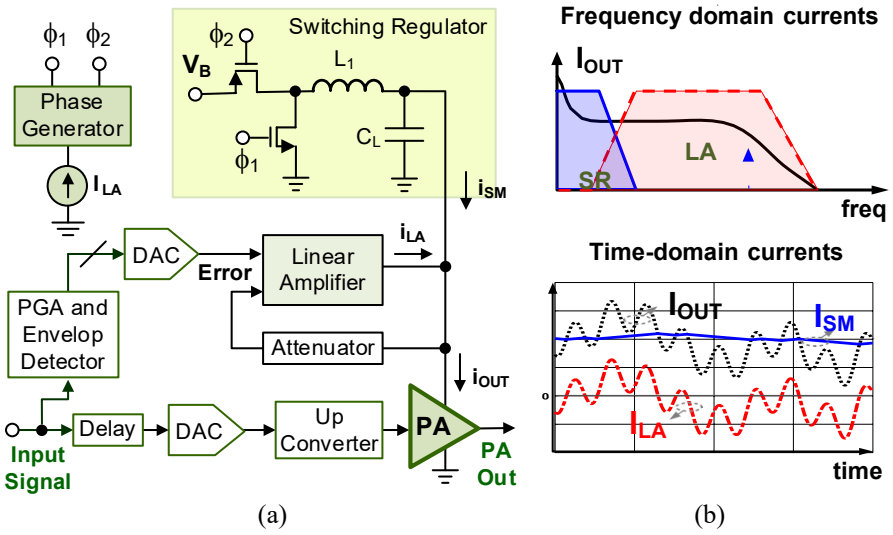
$$i_L(t) = i_L(t_0) + \frac{\int_0^t v_L(t)\,dt}{L} \tag{4}$$

For slow output voltage variations, the current rate is constant with a ramping rate of $v_L(t)/L$ amps per second. Reducing the inductance value increases the amount of current delivered to the modulator's output, leading to a more agile regulator, but the output voltage ripple increases according to equation (1a). Several topologies that track broadband signals while maintaining the properties of conventional switching regulators have recently been reported. Two of these techniques are revisited in the following section, and some more advanced approaches are briefly covered in Section V.

IV. Hybrid Envelope Tracking Modulators

Switching Modulator with Analog Linear Amplifier. The modulator's functionality can be improved by using an analog amplifier [18]; class-AB or even class-B amplifiers are preferred because they are more power efficient and usually exhibit a higher slew rate than conventional class-A amplifiers. The block diagram of this architecture is depicted in Fig. 5(a). In this architecture, different from the switching regulator controlled by a voltage feedback loop, as shown in Fig. 4, the switching regulator is based on a ripple current feedback control scheme. The linear regulator reduces the ETM voltage ripple and offers superior high-frequency performance. A linear amplifier's output current is proportional to the error function and used to control the switching regulator's clock phases $\phi 1$ and $\phi 2$. The current feedback loop of the switching regulator forces the linear regulator's current i_{LA} to be minimal, which reduces the amplifier's power consumption, thus maximizing the ETM system's power efficiency. This approach requires accurate characterization of the TX gain to predict the switching regulator's output correctly. Timing equalization between the PA output and ETM output is equally critical.

In this architecture, the switching regulator provides most of the current with a contribution by the amplifier to follow fast signal variations and reduce output ripple. The power-efficient switching regulator ISM delivers the low-frequency current, as illustrated in Fig. 5(b). Due to inherent design tradeoffs, the switching regulator cannot manage the high-frequency components. The high-frequency current demanded by the PA is provided by the broadband linear amplifier, I_{LA} in Fig. 5b. The attenuator in feedback and the DAC at the input of the linear amplifier generates the error function. The purpose of the local loop is to minimize this error. The amplifier must provide high gain in the frequency range of interest for that purpose.



(a) (b)

Fig. 5. Envelope tracking system employing a buck converter and a linear amplifier; a) block diagram and b) current components in frequency and time domains.

The linear amplifier power losses can be divided into two primary sources. The first component is the static power loss due to the quiescent current of the linear amplifier. The second component is dynamic due to the class-AB operation of the amplifier when processing the signal, which bounds the amplifier's power efficiency to 78.5%. An expression for the linear amplifier's approximate power consumption is:

$$P_{LA} = V_{DD} I_Q + \overline{(V_{DD} - V_{OUT}) I_{LA}} \tag{5}$$

where I_Q is the quiescent current of the linear amplifier. The power consumption of the linear amplifier increases when the delivered current I_{LA} increases; optimal power efficiency is achieved if I_{LA} is minimized. This goal can be achieved if the modulator's output current closely matches the current demanded by the PA. The second aim of recent power optimization techniques is to reduce I_Q [19]. There is a preference for class-AB amplifiers operating close to class-B mode with minimum bias current.

Loop Controller: PWM versus Hysteresis. There are two principal control methodologies to distribute current between linear and switching regulators: i) pulse-width modulation (PWM) control method and ii) hysteresis control. These control methods' primary operational principles, advantages, challenges, and techniques derived from the conventional hysteresis and PWM control are discussed here.

The linear amplifier's current is converted to a control voltage in a PWM control system. Then, after passing through the compensation circuit, the current is compared with a synchronization signal and modulates the duty cycle of the PWM signal to generate the proper signals to control the switching converter. Switching noise from the switching converter can be attenuated by employing switching converters with complementary phases. Multi-phase switching converters use PWM control with proper alignment between phases to increase the effective frequency at the regulator's output and reduce ripple current. The PWM control loop requires a compensation circuit for stable operation. The PWM control is an averaging process, and its bandwidth is a fraction of the switching frequency [20].

In a hysteresis-controlled modulator, the linear amplifier is sensed and drives a hysteresis comparator to control the switching amplifier's current. The comparator continuously compares its two inputs and generates the proper signal to control the loop. Consequently, the sense signal is bounded by the hysteresis window. The advantage is that the hysteresis-controlled loop is stable and does not require compensation circuits. Thus, the loop speed can be as high as the switching frequency. The switching frequency of a hysteresis-controlled loop is [21]:

$$f_{sw} = \frac{R_{sense}\, V_{out}\, (V_{DD} - V_{out})}{2\, L\, V_{DD}\, A_I\, V_{hysterisis}} \quad (6)$$

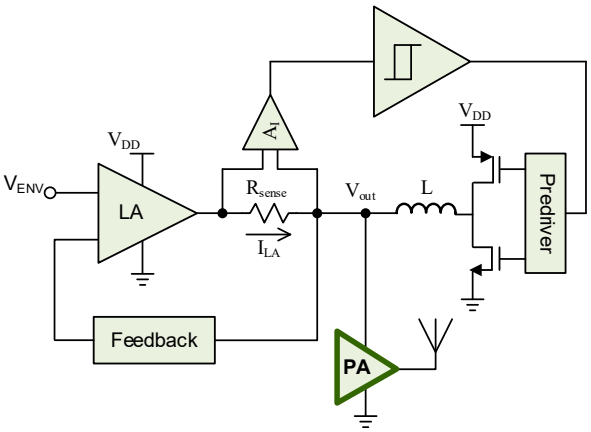


Fig. 6. Hybrid envelope tracking modulator adopting hysteresis control.

where V_{DD}, V_{out}, $V_{hyserysis}$, R_{sense}, L, and A_I are the supply voltage, the output voltage of the supply modulator, the comparator's hysteresis voltage, current sensing resistance, inductance value, and the current sensing gain, respectively, as shown in Fig. 6. By selecting different design parameters, the switching frequency can be optimized to benefit system power efficiency [17]. Since the output voltage V_{out} is a time-variant, the switching frequency of this control method is also a variable. Current-sensing devices are needed in this approach because this is a vital block. The block is needed to ensure the stability of the modulator. Sensing elements based on small series resistance or using strategy current mirroring are two preferred techniques.

ETM Incorporating a Current Steering DAC. The amplifier-aided switching regulator shown in Fig. 5(a) presents several advantages. The closed loop operation of the amplifier represents an equivalent impedance inversely proportional to its transconductance; the amplifier can reduce the glitch during the PA's output signal transients that the highly efficient switching regulator cannot manage. However, sufficient phase margin and wideband functionality are of primary concern.

Digital control feeds back discrete packages of current instead of the continuous-time current generated by a linear amplifier. Consequently, a linear amplifier can be replaced by a judicious combination of ADCs and DACs. The schematic is shown in Fig. 7. The ETM output voltage is monitored and attenuated to fit within the linear range of the mixed-mode blocks. Then, the error signal is driven by both the switching regulator loop and the digitally controlled loop. A digital controller manages the fast path; the performance tradeoff is that agile ADC and DAC blocks are required. The architecture discussed in [16, 17] employs a single-bit DAC and a comparator with hysteresis, but the principle can be extended to the case of multi-bit ADCs and DACs. Recent advances in flash ADCs and current steering DACs have demonstrated full functionality with conversion rates above 1GSample/sec and modest power consumption. This architecture can deliver a large amount of current in a few nanoseconds, which is impossible when using linear amplifiers. This approach presents a higher slew rate and faster settling time when the loop encounters large input signal variations; the ADC/DAC loop functionality benefits from the trend of the technology towards faster digital circuits. On the downside, the ADC-DAC auxiliary system introduces quantization noise when converting analog signals into a digital format.

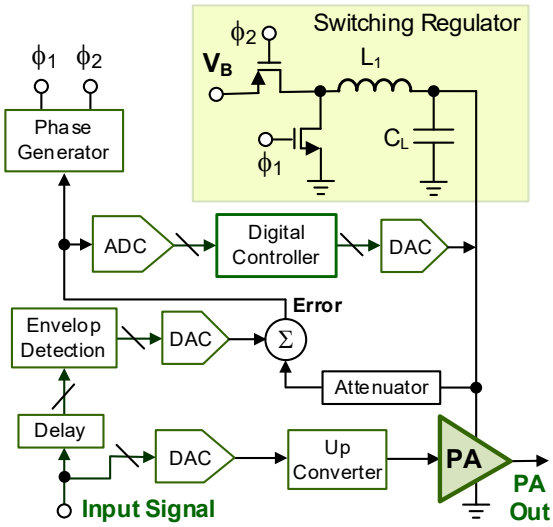


Fig. 7. Envelope tracking system employing a switching regulator and ADC-DAC loop.

Comparison of LA and DAC-aided switching modulators. The conventional switching modulator, the ETM combined with a linear amplifier, and the ETM with an auxiliary DAC are compared through transient simulations. The switching modulators are loaded by paralleling a 4Ω resistor and 300pF capacitor and using a pulsed current source. The inductance value is set at 75nH. The clock frequency used in the DAC-ADC is set at 1GHz. The transient response is characterized by applying a voltage step at the modulator's input at t=1nsec. An additional load current changes from 0-250mA at t=30nsecs.

The conventional switching modulator's (SM) output follows the exponential behavior of a second-order system until t=30nsecs; see Fig. 8(a). The load current is provided entirely by the inductor. The voltage across the inductor dictates the current's value. The current value is depicted in Fig. 8(b). The inductor's current slew rate is then limited by v_L/L, where v_L is the voltage across the inductor's terminals. The current's slew rate can be increased by reducing the inductance value. However, this approach increases the modulator's output ripple. At t=30nsecs, the output of the conventional switching modulator reaches 2.4V, still far from the ideal output voltage of 3V. A sinusoidal signal of 3V at 10MHz presents a peak voltage variation of 3.8V in 10nsecs. The conventional modulator is not able to track large and fast envelope signals.

The effect of the linear amplifier is visible in the trace SM+LA case in Fig. 8. In this case, the amplifier's small-signal transconductance gain of 100 mA/V is used. A very fast transition occurs during the first few nanoseconds, but the smaller the voltage difference at the amplifier's input, the less effective the amplifier is because the current contribution is correlated with the magnitude of the error voltage. In this case, the inductance current is smaller since the LA provides the additional load current; the tradeoff is that the PE decreases since the LA is not 100% efficient.

The flash ADC and DAC react very quickly. Theoretically, a single clock period is sufficient to deliver a large amount of current. However, the example case used three bits of current steering: DAC (±62.5mA, ±125mA, ±250mA, and ±500mA). The large current delivered by the DAC drastically reduces the modulator's settling time, although the output is not 100% accurate due to the ADC-DAC's limited resolution. The current steering DAC can deliver/extract approximately 1 A in one clock period; see Fig. 8. Inductance current does not increase significantly because the voltage across the inductor decreases because of the DAC current. Power consumption during a transient is determined primarily by the DAC's power consumption.

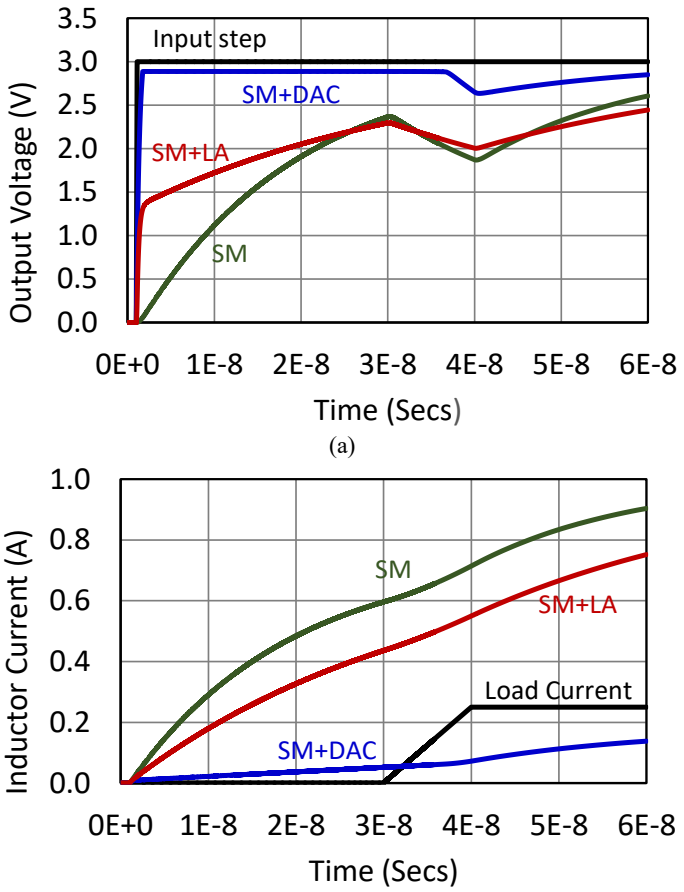


Fig. 8. Transient response for the conventional modulator, modulator plus linear amplifier (SR+LA) and modulator plus DAC (SM+DAC): a) output voltage and b) inductor current.

Load Current Variation. In addition to the voltage variation, the load current was changed from 0 to 250mA during the 30-40nsecs time frame. The output voltage variation is evident in the case of the conventional modulator and the case of the modulator equipped with the linear amplifier. The modulators require over 30nsecs after the step in the load current. Also, the results for the DAC-aided modulator are depicted. Due to the fast response of the ADC and DAC, the glitch is relatively minor compared with the other two cases. However, the ETM is more agile, with reduced glitches and a shorter recovery time. The inductance current increase is lower in the case of the ETM with a DAC, making it extremely attractive for cases with large input transients, which is the case for highly spectral-efficient modulation schemes.

V. Advanced Techniques in Hybrid Supply Modulators

Class-H Linear Amplifier. Recent optimization schemes use a dedicated system to modulate the power supply that feeds the linear amplifier [22-25] Figs. 9(a) and (b) show two different techniques. The architecture shown in Fig 9(a) modulates the supply voltage of the LA according to envelope level V_{ENV}. A conventional buck converter is used for this purpose. The LA is AC-coupled to improve mid-range power efficiency [22]. As shown in Fig 9(a), capacitor C isolates the low-frequency LA output and provides a

voltage-level shift between them. It also ensures that the linear amplifier provides no DC. Since the series capacitor is embedded in the loop of the linear amplifier, it blocks the DC feedback; hence care must be taken to ensure that the amplifier is stable and its operating point is well controlled.

The supply voltage of the class-AB LA does not need to be highly accurate but must be very power efficient. It is worth mentioning that the disadvantages of the AC-coupling method include the following: a) the extra off-chip capacitor C is usually large, even in the range of mFarads; b) the effect of the bond-wire inductors must be carefully evaluated and accounted for during the design process; c) the DC level of the linear amplifier needs to be carefully controlled; d) multi-loop control with increased complexity is required.

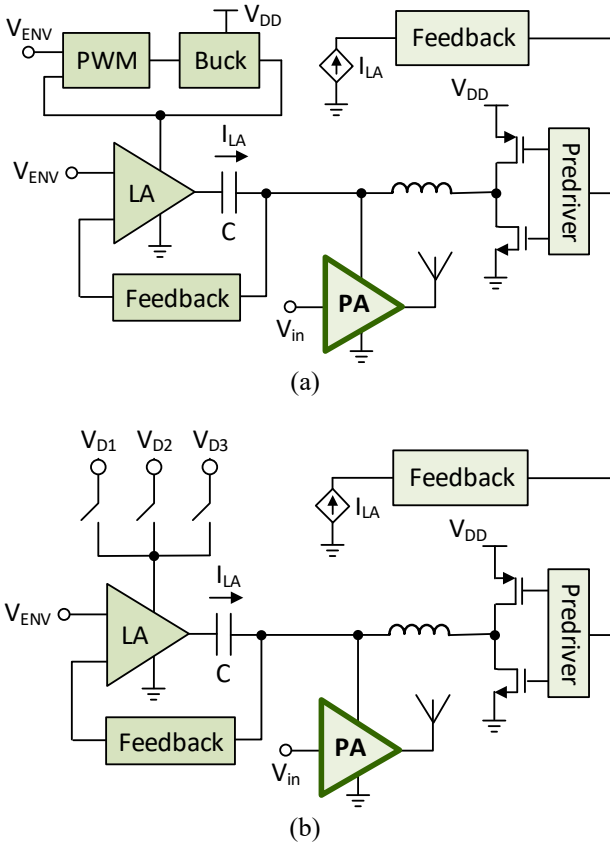


Fig. 9. Advanced Hybrid Supply Modulators; a) AC-Coupled class-H linear amplifier and b) Supply Modulated with class-G linear amplifier.

Class-G Linear Amplifier. Fig. 9(b) shows several discrete supply voltages biasing the linear amplifier [25]. The DC power supply is selected according to the expected signal's envelope level; the amplifier belongs to the class-G category. The switching between power supplies is digitally controlled and can be very agile, but this approach has limitations since the number of levels is usually limited to 3 or 4 in practical applications. The issue in this topology is the efficient generation of the multiple power supply levels; a single-inductor multiple output level topology is an attractive option, but other solutions employing switched-capacitor techniques are possible. If the power supply levels are external, the effect of the bond wire inductors must be further evaluated.

Efficient Linear Amplifiers. Wideband signal applications employing highly efficient spectrum coding schemes demand linear amplifiers with stringent slew-rate specifications. The linear amplifier must have sufficient bandwidth, a high slew rate, and a significant drive capability to track the envelope signal of the large PAPR. A high slew rate is required. Consequently, the linear amplifier must use large bias current levels, degrading its power efficiency. However, a further study of the OFDM signals shows that a high slew rate is required only during a low percentage of the transmit time. The solution proposed in [26] employs adaptive biasing and a gain-enhanced operational transconductance amplifier (OTA) connected in parallel with the buck modulator. Authors in [27] use a current reuse technique to improve the amplifier's gain-bandwidth product without increasing its current consumption. Numerous other solutions are available in the open literature.

Hybrid ETM employing multi-level switching modulators. Multi-level switching is another technique devoted to reducing the modulator's output ripple and improving the ETM's power efficiency [28], as shown in Fig. 10(a). The proper supply voltage level is selected according to the envelope level to reduce the ETM ripple and adjust the slew rate of the inductance's current. The class-G principle is used in the

example switching regulator. The linear amplifier's current is monitored. The class-G loop minimizes the current such that the overall system efficiency improves. A single inductor requires multiple power supplies to implement this architecture. The multiple switching levels usually reduce the inductance current ripple. This property allows us to design wider band switching regulators with higher efficiency. The multiple supply voltages are usually off-chip, then the board and chip area increase.

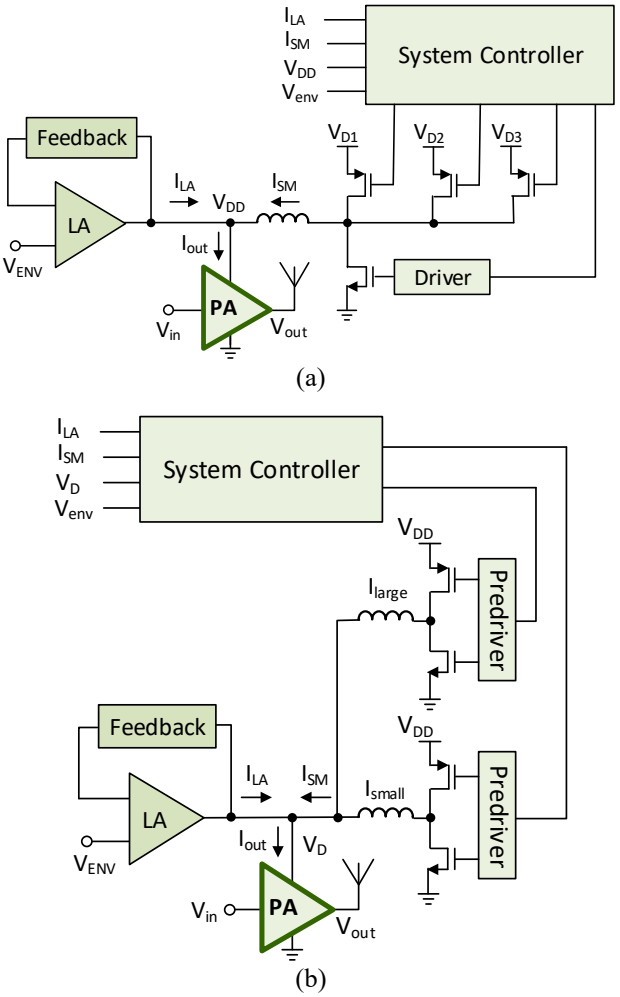


Fig. 10. Hybrid Supply Modulators: a) with multi-level power supply and b) with dual switching inductors.

Dual switching stages. Dual switching has been proposed to minimize the LA's current [29]. Fig. 10(b) shows dual switching stages in a hybrid structure. The switching stages are classified as follows: 1) L_{large} inductor, slow switching stage, which operates at the same frequency as the switching stage in a conventional hybrid structure, provides the DC and low-frequency modulator's output components; 2) L_{small} inductor implements a fast stage that switches at higher frequencies with increased bandwidth to help the linear amplifier in providing high-frequency current. The controller is more complex because it requires current sensing elements. Indeed, the goal is to arrange the clock phases lumped to L_{small} such that LA's current, $I_{LA,}$ is minimized. This goal is achievable for frequency components within the modulator's bandwidth. Still, the linear amplifier is required to track fast envelope variations.

Multi-phase switching. An alternative method uses a multi-phase switching scheme that differs from the architectures that use slow and fast switching stages. The multi-phase switching modulators have several identical stages/channels, working in a time-interleaved fashion. Consequently, the bandwidth of the regulator is extendable without increasing the switching frequency of each stage. The phase of each channel is managed so that, ideally, the ripple is canceled. However, the DC and fundamental current components are added. In [30], four multi-phase channels are used; the switches are divided into 16 identical unit cells. Then, the envelope signal is quantized to 16 different levels. The multi-phase switching mainly benefits large signal variations, so the four channels can work in several phase modes. Adaptive control switches the mode according to the envelope's amplitude.

Multi-level switching modulators with single supply voltage. The three-level switching converter (3L-SWC) with a single supply voltage has also been used, as shown in Fig. 11. The multi-level input power needed for class-G operation is provided by switching-capacitor techniques. The hybrid modulator has extra switches, S_1 and S_4, that pre-charge the flying capacitor C to V_{dd}. After the pre-charging phase, the capacitor is used as a charge pump to generate a 2Vdd output when S7 is activated. The capacitor can also be strategically pre-charged to $V_{dd}/2$ through S_5 and S_6 when driving low-power signals. The capacitor can be bypassed and

V_{dd} Applied. Thus, three different voltage levels can be applied to the inductor. This solution is attractive for IC integration if the capacitor can be integrated on-chip. This approach is claimed to reduce the switching current ripple amplitude by at least 50% compared to conventional two-level converters [31-36]. PWM is the typical control methodology in 3L-SWCs, which poses several challenges. First, the loop bandwidth is only a fraction of the switching frequency [11]. Therefore, the converter may have high switching losses when it provides wideband output current. Feedforward paths compensate for the low-speed switching loop [10, 20] at the cost of increased complexity in the control loop. Second, a compensation circuit is required, which may reduce the modulator's overall bandwidth even more. Usually, a PWM-controlled 3L-SWCs requires accurate timing signal generators. This scheme relies on the process, voltage, temperature (PVT) variations, device mismatch, control signal duty-cycle error, and device parasitics [34, 35]. Consequently, an additional calibration loop may be required [32].

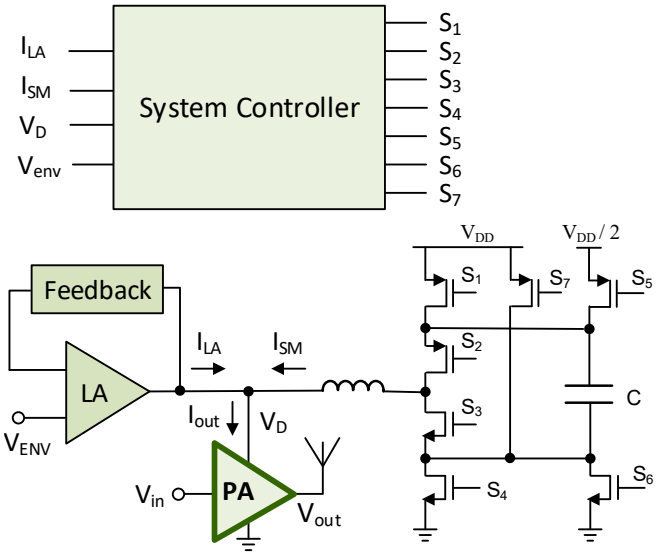


Fig. 11. Hybrid Supply Modulator with multi-level power supply generated by a switched-capacitor circuits.

Recently, a three-level switching converter with a hysteresis control loop was reported [37]. Using a hysteresis-based controller, the 3L-SWC provides a high-speed control loop. This topology results in low-ripple and low-loss properties while relaxing the challenges associated with PWM-controlled loops. The architecture uses a concurrent flying capacitor voltage regulation. Authors in [38] proposed a dual-channel three-level buck-boost converter that reduces the complexity of the control loops needed to regulate the flying capacitor voltage.

Digitally controlled switching regulators. Hysteretic control presents several advantages due to its straightforward control loop and higher system bandwidth than the conventional PWM control engine. Large hysteresis factors result in lower operating frequencies but additional latency and higher output ripple. Small hysteresis values result in less latency but higher switching frequencies. Long latency is due to the hysteretic control, resulting in higher linear amplifier power consumption. The latency has some implications: 1) the loop can only respond after a signal variation larger than the hysteresis value occurs; 2) for limited loop bandwidth, it is challenging to track fast signal variations. The digital feedforward controllers based on predictions are viable alternatives.

The solution reported in [39] predicts the output current of the switching regulator instead of monitoring and feeding it back. The predicted current is then compared with the input signal's future envelope value to generate the switching regulator's control sequence. These operations are all performed in the digital domain, leading to an agile predictive controller. This solution adopts a fixed lookahead approach, making it very effective for narrow-band applications but of limited benefit for wideband applications. Solutions reported in [40, 41] suggest using intelligent digital algorithms, adaptively adjusting the lookahead amount based on signal properties (signal velocity and amplitude), to find the optimal switching timing that

minimizes the mismatches between the load current and the output current of the switching regulator. Further developments would result in wideband functionalities with better power efficiency figures.

Table I compares the performance of a few recently reported broadband modulators with similar output power and peak-to-average power ratio. Although fabricated in 90nm technology, the architecture based on slow and fast modulators ([29]) achieves 88% peak efficiency for 0.8W output power while handling a 100 MHz signal bandwidth. Very competitive results are achieved if the 3-level buck-boost modulator ([37]) is added, achieving 91% peak efficiency in a bandwidth of 80MHz. [30] employs CMOS and GaN technologies and is based on the 4-phase switching approach; power efficiency is very similar to the ones reported in [38], which employs vanilla 90nm CMOS. Fabricated in a 40nm CMOS technology, the architecture reported in [40] can manage signal bandwidth up to 160MHz and achieves a power efficiency of 74% while tracking a signal envelope with a PAPR of 5 dB.

The last two rows of Table I provide the performance characteristics of the entire RF transmitter (ETM + PA). The testing signals are around the same average power and PAPR when testing ETM only and testing ETM + PA if not annotated.

Table I

Reference	[29] ISSCC' 19	[30] JSSC' 21	[37] JSSC' 19	[38] ISSCC' 21	[40] JSSC' 22
Architecture	Slow SM* + fast SM*	4-phase switching	Three-level buck	Slow SM* + fast SM* & Three-level buck-boost	Digitally controlled switching
Process	90nm CMOS	0.5µm GaN + 180nm CMOS	65nm CMOS	90nm CMOS	40nm CMOS
Protocol	5G NR 100MHz	5G NR 130MHz	LTE-A 80MHz	5G NR 130MHz	OFDM 160MHz
Avg. Out Power (W)	0.8	3.5	1	3.53	0.6**
Peak Efficiency (%)	88	85.7	91 @80MHz 93 @40MHz	84.1	74
PAPR (dB)	6	6.3	7.84 @80MHz 8.06 @40MHz	6	5
Performance of ETM + PA					
RF Power (dBm)	23	26	24	26	22.3 @12 dB PAPR
ACLR (dBc)	-38.1	-39.2	-32.5	-37.7	-35 @12 dB PAPR

* SM is the abbreviation of supply modulator
** Extracted and calculated from the graph

VI. Practical Design Issues

Since the drain voltage generated by the ETM and main signal paths experience different delays, a timing alignment engine is required to avoid excessive nonlinear PA operation and spectral regrowth. As the signal bandwidth increases, the timing mismatch becomes more critical. Another significant issue is the magnitude mismatch between the envelope modulator's drain voltage and the PA's output magnitude. The PA experiences early saturation if the ETM's output is less than required, and the system power efficiency degrades if the ETM output is larger than needed. Therefore, the practical ETM system demands a calibration engine.

ETM: Design Issues. TX timing and gain characterization are necessary for the effective operation of the envelope tracking system. Fig. 12 illustrates several scenarios. The envelope of the PA output voltage is shown in black. The ideal voltage generated by the envelope tracking system must be identical to the envelope of the PA output but shifted by a voltage offset needed for PA functionality; the ideal ETM voltage corresponds to this case. If the magnitude of the signal generated by the ETM is larger than needed (ETM with excessive voltage), then the power efficiency will be reduced. In the other case, if the ETM voltage is smaller than needed, the PA will become very nonlinear, and signal clipping will arise. It is also evident that timing mismatch is detrimental.

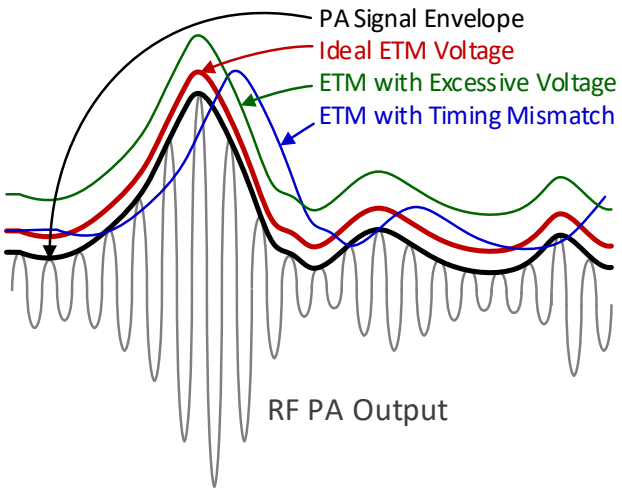


Fig. 12. PA output waveform and its envelope. Several ETM output voltages are shown including the ideal ETM voltage as well as the effect of ETM magnitude and timing errors.

A potential calibration scheme is displayed in Fig. 13. An analog multiplexer MUX selects either the calibration mode or the regular operation mode. During calibration, the calibration signature is routed to a digital calibration scheme. After up-conversion, the input signal is routed to a programmable digital delay element and then applied to the PA. The signal is also injected into the ETM system. Two controlling loops can be identified in this architecture. The PA output is monitored and down-converted, and the baseband information is converted into a digital format. The baseband signals are compared. The magnitude and phase errors are identified and corrected through a smart-calibration algorithm. The programmable delay element ΔT is adjusted to calibrate for delay mismatches in the two paths based on the results of the timing estimation engine. The parameters of the ETM are adjusted according to the results of the power estimation block.

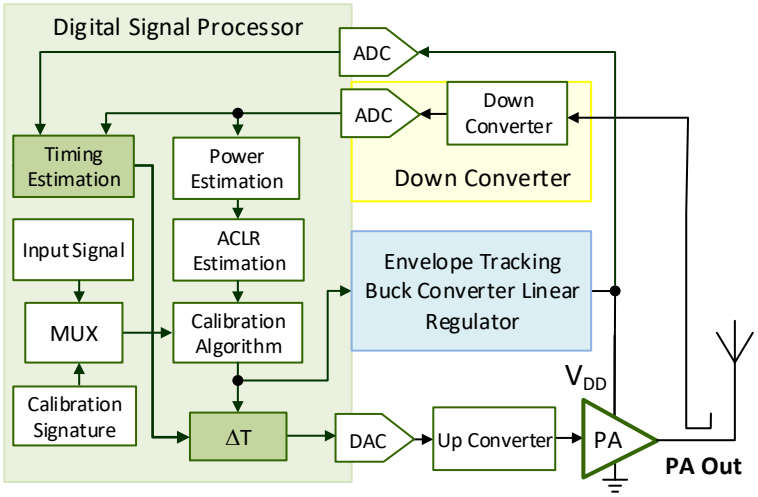


Fig. 13. Transmitter with digital calibration scheme employing linear feedback to measure its non-idealities and power gain. PA's biasing is generated from the combination of switching and linear regulators.

The PA characterization scheme can be incorporated into the architecture shown in Fig. 13. During the PA calibration process, the TX gain must also be characterized. The calibration algorithm compares the PA's output magnitude and input signal to characterize the power gain for different power levels. These measurements help to provide an educated prediction of the TX output level. The ACLR can also be measured by proper filtering. A digital linearization engine can be trained to reduce the power of the aliased components in neighbor channels.

Conclusions

This paper revisited the most promising techniques for designing power-efficient power amplifiers. The power efficiency of linear power amplifiers is often improved by using class-H and class-G techniques. The principle behind these techniques is to modulate the power supply providing the minimum voltage needed for the proper operation of the PA. For this purpose, the time-variant power supply must be correlated with the PA's output signal envelope. For the case of a sinusoidal signal, its envelope consists of a DC component and even-order components, dominated by the second-order component. Therefore, the bandwidth of the envelope signal is at least twice the bandwidth of the original signal. If additional accuracy is needed, the bandwidth of the envelope tracking system must be as much as four times the original signal bandwidth. Thus, current trends in ETM systems focus on increasing the bandwidth of the linear amplifiers. Alternative techniques include using multiple power supplies, current steering DACs, or multiple inductors. Each technique presents a different challenge.

Hybrid modulators using switching regulators and linear amplifiers have become the mainstream envelope tracking systems for wideband applications. However, there are switching frequency issues because of the limited bandwidth of switching regulators. Multi-level switching results in lower inductor ripple and more nuanced slew-rate control of the output current. The result is better tracking of wideband signals. The multi-phase switching utilizes multiple switching stages in a time-interleaved manner to extend the bandwidth of the switching regulator. The slow-buck/fast-buck scheme uses two switching regulators optimized for different switching frequencies, covering the envelope's low-frequency and high-frequency parts. Digitally controlled switching regulators optimize the switching timing based on predictions to minimize the difference between the load current and the switching regulator’s output current.

There are two additional requirements. It is necessary to model the PA’s gain function to generate a precise ETM signal. PA pre-characterization employing test signatures is a suitable approach. The second requirement is to synchronize the PA's output signal and the voltage level generated by the envelope tracking modulator. The signal chain delay through the amplifier differs from the delay used by the ETM for the generation of PA bias voltage. Smart-timing calibration techniques are needed. Machine learning techniques may be appropriate for characterizing complex modulation schemes.

References

[1] Yole Development, “RF Front End Modules for Cellphones 2017 report,” March 2017.
A 2017 report provides a market landscape of the existing RF front-end modules and components; points out the roadmap of the development tendency of RF front-end modules and components to meet the new generation communication standards, including 4G and 5G.

[2] S. Egolf, “Intelligent Power Management: A Method to Improve 2G/3G Handset Talk Time,” Microwave Journal, pp. 94-100, July 2007.
This article discusses power management techniques using PA bias-voltage control as a handset talk-time enhancement method. The power management techniques are discussed and demonstrated using experimental data taken on a GSM saturated PA, as well as a WCDMA linear PA. The results show the expected increase in talk time achievable with intelligent power management.

[3] S. C. Cripps, “RF Power Amplifiers for Wireless Communications,” Artech House Inc., Norwood MA, 1999.
This is an outstanding book that covers the most relevant power amplifiers. Linearity noise and power consumption are covered in this textbook.

[4] B. Berglund and U. Gustavsson, “Power Amplifiers for Base-Stations Possibilities and Challenges,” (Chapter 14; “Advanced Analog Circuit Design: Smart Data Converters, Filters on Chip and Multimode Transmitters, Arthur van Roermund, Herman Casier and Michiel Steyaert, Editors); Springer 2010.
This is a book chapter. The book is a collection of contributions from three different disciplines; one of them is devoted to multi-mode transmitters. Different authors cover several types of power amplifiers and some practical issues when designing RF transmitters.

[5] Rahmatallah, Y., Mohan, S., “Peak-to-Average Power Ratio Reduction in OFDM Systems: A Survey and Taxonomy,” IEEE Communications Surveys & Tutorials, Vol. 15, No. 4, pp. 1567- 1592, Sep. 2013.
This highly cited survey provides a broader understanding of the high PAPR problem in OFDM systems with the higher demanding communication needs, the corresponding effects on transmitter systems, and the solutions available to mitigate the problem.

[6] W. H. Doherty, “A New High Efficiency Power Amplifier for Modulated Waves,” in Proceedings of the Institute of Radio Engineers, vol. 24, no. 9, pp. 1163-1182, Sept. 1936, doi: 10.1109/JRPROC.1936.228468.
This classic paper reports on the invention of the Doherty amplifier, increasing the PA efficiency by using active loadline modulation and providing an optimum load to the PA for different signal levels.

[7] H. Chireix, "High Power Outphasing Modulation," in Proceedings of the Institute of Radio Engineers, vol. 23, no. 11, pp. 1370-1392, Nov. 1935, doi: 10.1109/JRPROC.1935.227299.
This classic paper first introduced outphasing modulation, which enables linear amplification with nonlinear components. Many later studies on outphasing transmitters follow the fundamentals described in this paper.

[8] A. F. Aref, T. M. Hone, and R. Negra, "A Study of the Impact of Delay Mismatch on Linearity of Outphasing Transmitters," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 1, pp. 254-262, Jan. 2015, doi: 10.1109/TCSI.2014.2349573.
This paper presents an analytical study of the impact of delay mismatch on the linearity of outphasing transmitters.

[9] L. R. Kahn, "Single-Sideband Transmission by Envelope Elimination and Restoration," in Proceedings of the IRE, vol. 40, no. 7, pp. 803-806, July 1952, doi: 10.1109/JRPROC.1952.273844.
This classic paper introduces an effective supply modulation method that separates the RF phase and RF envelope, enabling the use of nonlinear high-efficiency amplifiers in the transmitter's design.

[10] T. W. Kwak, M. C. Lee, and G. H. Cho, "A 2 W CMOS hybrid switching amplitude modulator for EDGE polar transmitters," IEEE J. Solid-State Circuits, pp. 2666–2676, 2007.
This highly cited paper contributes to the idea of "hybrid switching" with switch modulators and linear amplifiers on polar transmitters with deep-submicron CMOS technology.

[11] M. Tan and W. -H. Ki, "A 100 MHz Hybrid Supply Modulator With Ripple-Current-Based PWM Control," in IEEE Journal of Solid-State Circuits, vol. 52, no. 2, pp. 569-578, Feb. 2017, doi: 10.1109/JSSC.2016.2611513.
This paper introduces a ripple-current-based PWM control to overcome the bandwidth limitations of an absolute current sensor on conventional PWM control. The proposed PWM control approach has an intrinsically high-speed switching loop and thus eliminates the need for the feedforward path used in many PWM controller designs.

[12] W. -Y. Chu, B. Bakkaloglu and S. Kiaei, "A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters," in IEEE Journal of Solid-State Circuits, vol. 43, no. 12, pp. 2809-2819, Dec. 2008, doi: 10.1109/JSSC.2008.2005743.
This paper presents a combined class-AB and switch-mode regulator-based supply modulator with a master-slave architecture achieving wide bandwidth and low ripple.

[13] J. Ham et al., "CMOS Power Amplifier Integrated Circuit With Dual-Mode Supply Modulator for Mobile Terminals," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 1, pp. 157-167, Jan. 2016, doi: 10.1109/TCSI.2015.2512703.
This paper presents a CMOS power amplifier integrated circuit with an optimized dual-mode supply modulator providing two operation modes: envelope tracking for high average output power and average power tracking for low output power.

[14] H. He, Y. Kang, T. Ge, L. Guo, and J. S. Chang, "A 2.5-W 40-MHz-Bandwidth Hybrid Supply Modulator With 91% Peak Efficiency, 3-V Output Swing, and 4-mV Output Ripple at 3.6-V Supply," in IEEE Transactions on Power Electronics, vol. 34, no. 1, pp. 712-723, Jan. 2019, doi: 10.1109/TPEL.2018.2827396.
This paper presents a supply modulator comprising a proposed delay-based hysteresis controller, proposes a wideband class-AB amplifier, and a class-D amplifier for an envelope tracking power amplifier.

[15] G. Hanington, P.-F. Chen, P. M. Asbeck, and L. E. Larson, "High-Efficiency Power Amplifier Using Dynamic Power-Supply Voltage for CDMA Applications," IEEE Transactions on Microwave Theory and Techniques, vol. 47, pp. 1471-1476, Aug 1999.
This highly cited paper reports on improving the PA's efficiency by supply modulation. It uses a boost DC-DC converter to provide the optimal supply voltage for the RF PA.

[16] R. Turkson, S. Prakash, J. Silva-Martinez and H. Martinez-Garcia, "Envelope tracking technique with a bang-bang slew-rate enhancer for linear wideband RF PAs," 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), 2013, pp. 629-632, doi: 10.1109/MWSCAS.2013.6674727.
In this paper, a bang-bang auxiliary system is connected in parallel with the conventional switching regulator to improve its slew rate. The slew rate limitation is identified as the main challenge, and a

`bang-bang' slew-enhancement technique with a single-bit DAC is proposed to use efficient supply modulators in wideband power amplifiers.

[17] S. Prakash, H. Martínez-García, M. H. Naderi, H. Lee, and J. Silva-Martinez, "An Agile Supply Modulator With Improved Transient Performance for Power Efficient Linear Amplifier Employing Envelope Tracking Techniques," in IEEE Transactions on Power Electronics, vol. 35, no. 4, pp. 4178-4191, April 2020, doi: 10.1109/TPEL.2019.2934364.
This article presents an agile supply modulator with optimal transient performance that includes improvement in rise time, overshoot, and settling time for the envelope tracking supply in linear power amplifiers. Its objective is to follow fast variations in input signals with reduced overshoot and settling time without deteriorating the steady-state performance of the buck regulator. An on-demand current source module is employed. This article also introduces an efficient selective tracking of envelope signals for linear PAs.

[18] J. T. Doyle, D. Maksimovic and Y. Li, "Method and System for Providing Power Management in a Radio Frequency Power Amplifier Using Adaptive Envelope Tracking," USA Patent 6914487, July 2005.
One of the early works supplied PA power with adaptive envelope tracking using switchers and an operational amplifier. The tracking control is based on the power control signal, the feedback signal, and the PA input signal.

[19] M. Hassan et al., "High efficiency envelope tracking power amplifier with very low quiescent power for 20 MHz LTE," 2011 IEEE Radio Frequency Integrated Circuits Symposium, 2011, pp. 1-4, doi: 10.1109/RFIC.2011.5940618.
This paper presents a hybrid envelope supply modulator with a switching regulator and a linear amplifier. The modulator was applied for a 20MHz LTE signal. It introduced a source cross-coupled linear amplifier to reduce the quiescent power and hence improved the overall power efficiency of the supply modulator.

[20] P. Y. Wu and P. K. T. Mok, "A Two-Phase Switching Hybrid Supply Modulator for RF Power Amplifiers With 9% Efficiency Improvement," in IEEE Journal of Solid-State Circuits, vol. 45, no. 12, pp. 2543-2556, Dec. 2010, doi: 10.1109/JSSC.2010.2076510.
This highly cited paper exploits the idea of a multi-phase switching regulator in a hybrid ETM. It verifies that with the same equivalent inductance, using two-phase switching can reduce the overall switching loss by half compared to one-phase switching.

[21] J. Choi, D. Kim, D. Kang, and B. Kim, "A Polar Transmitter With CMOS Programmable Hysteretic-Controlled Hybrid Switching Supply Modulator for Multi-standard Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 7, pp. 1675-1686, July 2009, doi: 10.1109/TMTT.2009.2021880.
This highly cited paper presents a linear polar transmitter supporting multi-standard applications. It provided a systematic analysis of hysteretic-controlled switching regulators.

[22] P. Riehl, P. Fowers, H. -P. Hong and M. Ashburn, "An AC-coupled hybrid envelope modulator for HSUPA transmitters with 80% modulator efficiency," 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, 2013, pp. 364-365, doi: 10.1109/ISSCC.2013.6487771.
This paper demonstrates an envelope modulator that improves the mid-range power efficiency by ac-coupling the linear amplifier output to the switching regulator output. The ac-coupling capacitor provides a level shift between the class-AB supply voltage and the PA supply.

[23] C. -Y. Ho et al., "An 87.1% efficiency RF-PA envelope-tracking modulator for 80MHz LTE-Advanced transmitter and 31dBm PA output power for HPUE in 0.153μm CMOS," 2018 IEEE International Solid-State Circuits Conference - (ISSCC), 2018, pp. 432-434, doi: 10.1109/ISSCC.2018.8310369.
This paper focuses on equipping the LA with multi-mode to achieve hybrid ETM for wideband cellular LTE applications up to 80MHz. A dual-mode high-speed AC feedforward class-AB LA was designed to have both high-bandwidth and high-gain modes to meet different bandwidth needs while maintaining high efficiency.

[24] B. Park et al., "High-Performance CMOS Power Amplifier With Improved Envelope Tracking Supply Modulator," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 3, pp. 798-809, March 2016, doi: 10.1109/TMTT.2016.2518659.
This paper uses a hybrid modulator but focuses on providing a non-zero VSS signal for the linear amplifier and switching regulator to save power.

[25] Y. Wang, X. Ruan, Q. Jin, Y. Leng, F. Meng, and X. -W. Zhu, "Quasi-Interleaved Current Control for Switch-Linear Hybrid Envelope-Tracking Power Supply," in IEEE Transactions on Power Electronics, vol. 33, no. 6, pp. 5415-5425, June 2018, doi: 10.1109/TPEL.2017.2735485.
This paper proposes an efficient, improved linear amplifier with multiple supply levels generated by a level provider.

[26] Y. Jing and B. Bakkaloglu, "A High Slew-Rate Adaptive Biasing Hybrid Envelope Tracking Supply Modulator for LTE Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 9, pp. 3245-3256, Sept. 2017, doi: 10.1109/TMTT.2017.2678476.
This paper discusses signal-level tracking adaptive-biasing and a gain-enhanced current mirror operational transconductance amplifier, in parallel with a buck-switching amplifier, to enhance the slew rate of the linear amplifier without increasing the quiescent current consumption.

[27] W. -T. Tsai, C. -Y. Liou, Z. -A. Peng, and S. -G. Mao, "Wide-Bandwidth and High-Linearity Envelope- Tracking Front-End Module for LTE-A Carrier Aggregation Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 11, pp. 4657-4668, Nov. 2017, doi: 10.1109/TMTT.2017.2744622.
This paper demonstrates a wideband envelope-tracking front-end module consisting of an envelope-tracking modulator (ETM), a dual-power-mode power amplifier, and an SPDT switch for the 4 x 20MHZ LTE-A carrier application. The proposed dual-path crossover current-reuse linear mechanism improves the gain-bandwidth of the linear amplifier without increasing current consumption.

[28] Y. Wang, X. Ruan, Y. Leng, and Y. Li, "Hysteresis Current Control for Multilevel Converter in Parallel-Form Switch-Linear Hybrid Envelope Tracking Power Supply," in IEEE Transactions on Power Electronics, vol. 34, no. 2, pp. 1950-1959, Feb. 2019, doi: 10.1109/TPEL.2018.2835640.
This paper presented a multi-level switching modulator that adopted multiple separate voltage supplies generated by a level provider.

[29] J. -S. Paek et al., "15.1 An 88%-Efficiency Supply Modulator Achieving 1.08μs/V Fast Transition and 100MHz Envelope-Tracking Bandwidth for 5G New Radio RF Power Amplifier," 2019 IEEE International Solid-State Circuits Conference - (ISSCC), 2019, pp. 238-240, doi: 10.1109/ISSCC.2019.8662460.
This paper exploits the idea of using a slow-switching buck converter, a fast-switching buck converter,

and a linear amplifier to achieve envelope tracking. The slow-switching buck converter provides the DC and low-frequency components of the envelope, and the fast-switching buck converter with feedforward covers the high-frequency components. The LA compensates for the current mismatched signal and provides a voltage signal. This work supports 100MHz signal bandwidth.

[30] Y. -T. Hsu, Z. -Y. Lin, J. -J. Lee and K. -H. Chen, "An Envelope Tracking Supply Modulator Utilizing a GaN-Based Integrated Four-Phase Switching Converter and Average Power Tracking-Based Switch Sizing With 85.7% Efficiency for 5G NR Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 56, no. 10, pp. 3167-3176, Oct. 2021, doi: 10.1109/JSSC.2021.3079403.
This paper proposes a hysteretic-controlled 4-phase switching regulator with multiple power loss optimization techniques. An APT-based dynamic switch size scaling scheme is introduced to balance the conduction loss and the switching loss for all the signal conditions. The proposed 4-phase modulator can also work in 1/2/3-phase mode to save power when the signal amplitude is small.

[31] V. Yousefzadeh, E. Alarcon and D. Maksimovic, "Three-level buck converter for envelope tracking applications," in IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 549-552, March 2006, doi: 10.1109/TPEL.2005.869728.
This paper is one of the early works showing that a three-level buck converter could offer advantages in terms of small switching ripple, losses, larger bandwidth, or the size of magnetic components compared to a standard buck or a two-phase buck converter.

[32] X. Liu, C. Huang and P. K. T. Mok, "A High-Frequency Three-Level Buck Converter With Real-Time Calibration and Wide Output Range for Fast-DVS," in IEEE Journal of Solid-State Circuits, vol. 53, no. 2, pp. 582-595, Feb. 2018, doi: 10.1109/JSSC.2017.2755683.
This paper proposes using a real-time flying-capacitor voltage-calibration approach for three-level buck converter operation.

[33] W. Kim, D. Brooks, and G. Wei, "A Fully-Integrated 3-Level DC-DC Converter for Nanosecond-Scale DVFS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 1, pp. 206-219, Jan. 2012, doi: 10.1109/JSSC.2011.2169309.
This work proposed a fully integrated three-level buck converter with a flying capacitor and on-chip 1nH spiral inductors implemented in a 130nm CMOS technology. This paper provides detailed efficiency simulation results and compares a wide range of design parameters to prove the merits of the three-level buck converter.

[34] X. Liu, P. K. T. Mok, J. Jiang, and W. -H. Ki, "Analysis and Design Considerations of Integrated 3-Level Buck Converters," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 63, no. 5, pp. 671-682, May 2016, doi: 10.1109/TCSI.2016.2556098.
This paper presents a systematic analysis of integrated three-level buck converters under both ideal and actual conditions as a guide for designing robust and fast three-level buck converters. It verifies the ideal conditions. A three-level buck converter has the same conversion ratio and loop-gain function as a two-level buck converter, while its peak output voltage ripple is much smaller than that of a two-level buck converter; in practice, maintaining V_{CF} as well as aligning the control signal in time is critical to keep the merits of a three-level buck converter.

[35] Thierry A Meynard, Maurice Fadel, and Noureddine Aouda, “Modeling of multi-level converters,” IEEE Trans. Ind. Electron., 44(3):356–364, 1997.
This is one of the early works that model multi-level converters. This paper criticized the previous model based on the average value and focused on developing a static and dynamic model that also considers the dynamic phenomenon that occurs within a switching period.

[36] H. -D. Gwon et al., "2-Phase 3-Level ETSM With Mismatch-Free Duty Cycles Achieving 88.6% Peak Efficiency for a 20-MHz LTE RF Power Amplifier," in IEEE Transactions on Power Electronics, vol. 33, no. 4, pp. 2815-2819, April 2018, doi: 10.1109/TPEL.2017.2754651.
This paper proposes an ETM with a multi-phase and multi-level switching regulator. It also introduces a time-division multiplexing comparator and a duty-cycle calibrator to eliminate the duty-cycle mismatch problem within a multi-level PWM controller.

[37] P. Mahmoudidaryan, D. Mandal, B. Bakkaloglu and S. Kiaei, "Wideband Hybrid Envelope Tracking Modulator With Hysteretic-Controlled Three-Level Switching Converter and Slew-Rate Enhanced Linear Amplifier," in IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3336-3347, Dec. 2019, doi: 10.1109/JSSC.2019.2941014.
This paper uses a hybrid ETM architecture to track an LTE 80MHz signal. This paper contributes to three domains: 1) explores further multi-level control and shows the advantage of power loss reduction when using three-level SWs over two-level SWs with proper control; 2) provides a solution for the smart control of fixed voltage flying capacitor V_{CF} that enabled the multi-level voltage; 3) proposes a neat three-level hysteresis controller.

[38] D. Kim et al., "33.9 A Hybrid Switching Supply Modulator Achieving 130MHz Envelope-Tracking Bandwidth and 10W Output Power for 2G/3G/LTE/NR RF Power Amplifiers," 2021 IEEE International Solid-State Circuits Conference (ISSCC), 2021, pp. 476-478, doi: 10.1109/ISSCC42613.2021.9365986.
The authors integrate a wide variety of design hot spots into the hybrid supply modulator to make it suitable for multi-mode/standard operation. The supply modulator architecture consists of a class-AB linear amplifier (LA) with scalable supply voltage/bias current/output stage, a micro buck-boost converter (micro-BB), an interleaved buck-boost converter (interleaved-BB), a 2G LDO, a resonance frequency tuning (RFT), a capacitor pre-charger (CPC) for AC coupling capacitor, and three switches.

[39] C. Hsia et al., "Digitally Assisted Dual-Switch High-Efficiency Envelope Amplifier for Envelope-Tracking Base-Station Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 11, pp. 2943-2952, Nov. 2011, doi: 10.1109/TMTT.2011.2166084.
This highly cited paper enlightens research on applying predictive control for the hysteresis controller to eliminate the time delay caused by the hysteresis controller. The hysteresis delay can cause time misalignment between the current generated by the switching regulator and the current being tracked. Hence, it triggers more current being compensated by the linear amplifier and degrades the overall ETM performance.

[40] W. Leng et al., "Envelope Tracking Supply Modulator with Trellis-Search-Based Switching and 160-MHz Capability," in IEEE Journal of Solid-State Circuits, vol. 57, no. 3, pp. 719-733, March 2022, doi: 10.1109/JSSC.2021.3128394.
This paper proposes a hybrid ETM with an optimized digitally controlled buck converter to achieve envelope tracking time alignment. It uses a Viterbi-like trellis search (TS) digital signal processing (DSP) algorithm to find the optimal switching sequence for the buck converter in the hybrid amplifier, lowering the RMS error current in the op-amp and minimizing switching. For 20-MHz channels, it lowers op-amp current by 27%. Hsia C's research enlightens this work.

[41] Z. Chen et al., "An Open Loop Digitally Controlled Hybrid Supply Modulator Achieving High Efficiency for Envelope Tracking With Baseband up to 200-MHz," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 11, pp. 4142-4153, Nov. 2020, doi:

10.1109/TCSI.2020.3014087.

This paper proposes a hybrid ETM with an open-loop digital control solution out of PWM and hysteresis control to achieve envelope tracking time alignment. It uses the average voltage alignment (AVA) algorithm to align segmented waveforms' peaks and valleys with pre-cached envelope signals to reduce the power loss due to the mismatch. The paper segments the envelope signal according to different peaks and valleys.