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# On-chip heating effects in electronic measurements at cryogenic temperatures

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ABSTRACT

Heating is a major concern for electrical measurements at cryogenic temperatures. In this study, the statics and dynamics of heating effects induced on a $Si/SiO_2$ chip by the application of DC and AC power to an on-chip heating element are measured using on-chip cryogenic thermometers. It is found that large on chip temperatures, ~ 100 mK above cryostat temperature, and large on-chip thermal gradients, 100s of mK over ~ 10 μm distance, are generated at relatively small (~ 0.1 μW) input powers. As expected, the heating effects are larger at lower cryostat temperatures. With applied AC voltages, it is found that the average temperatures generated are similar in magnitude to the DC voltages, but the temperature gradients are smaller. The average temperatures reached on the surface of the chip increase with increasing frequency. At 5 Hz frequency, the thermal dynamics are too slow to allow temperature oscillations following the input power, instead resulting in a steady state temperature increase.

## 1. Introduction

Electrical measurements at cryogenic temperatures provide insight into the fundamental Physics of a wide array of fascinating systems such as superconductors, topological materials, Hall systems, 2D electron gases, and quantum dots. The application of electrical power on the chip causes local heating. Temperature gradients are then generated between the heating element and the cooler parts of the chip. The electrical circuits used for these measurements are designed based on intuition about heat dissipation built from room temperature measurements. However, heat dissipation at cryogenic temperatures is very different from room temperature thermalization since the thermal conductivities are low [1,2], heat capacities are small [3], thermal boundary resistances are high [4], and the cooling powers available are small [5]. This problem is compounded when the circuits being measured are nanoscale, in which the heat due to electrical measurements is introduced into extremely small volumes. With the growth of functional nanoscale cryogenic circuits, the increasing number of circuit elements per unit volume is an additional compounding factor. Insights into on-chip thermal flows at cryogenic temperatures are therefore important.

Thermalization at cryogenic temperatures has been the subject of many studies [6]. For example, the thermal conductivity of greases and other materials connecting the sample to the cooling stage of the cryostat have been examined in detail [7–10]. With the recognition of on-chip heating as a major problem in room temperature electronics [11–13], in the last two decades, a lot of attention has been paid to technologies for on-chip cooling at cryogenic temperatures. Nanomagnetic devices [14,15], tunneling junctions [16,17], and quantum dots [18] have all been leveraged in proof-of-principle experiments demonstrating electronic cooling at cryogenic temperatures. Further advancements in some of these technologies over the years have also resulted in progress towards practical on-chip cryogenic refrigeration [19]. In a different but related direction, growing interest in the low temperature thermal properties of materials and micro- and nanoscale devices has also led to research on cryogenic on-chip heat management and thermalization of on-chip electronics. For instance, experiments measuring the thermal conductivities of single crystals [20] and nanowires [21,22], and those examining Nernst effect of superconducting thin films [23] have been performed. The thermalization of metallic islands has also been studied in detail [24]. These advances have come hand-in-hand with the development of a number of tools for on-chip thermal measurements such as noise sources [25] and sub-Kelvin thermometers [26–28].

In this paper, we measure temperatures generated across the surface

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of a silicon/silicon dioxide substrate at sub-Kelvin temperatures upon the application of AC and DC voltages to a micro-scale on-chip heater. The complexity of thermal transport near the surface with nanostructures and the scarcity of measurements of relevant thermal transport parameters, such as boundary resistances, makes theoretical estimates of these quantities challenging. As a result, authentic estimates of heating as a function of the distance, power, and measurement frequency are not available. This lack of information can be seen in the wide range of input powers different cryogenic experiments use to avoid heating. Some cryogenic studies, such as measurements of topological effects, use very low powers ($< 1 \times 10^{-9}$ W) [29–32], while others, such as field effect measurements on nanowires and electron spin resonance studies on quantum dots, use powers that are several orders of magnitude higher than that ($\sim 1 \times 10^{-7}$ W) [33–36,23]. The quantitative study of the heating effects on a chip at cryogenic temperatures presented here will enable deliberate design of cryogenic circuits and measurement protocols to avoid heating effects while minimizing noise and optimizing measurement time.

## 2. Methods

In this study, an Oxford Instrument Triton dilution refrigerator (DR) was used to cool down a Si substrate with a 240 nm thermally grown $SiO_2$ layer on top. The DR has a base temperature of 8 mK and cooling powers of 20 μW and 450 μW at 19.1 mK and 91 mK for the mixing chamber (MC) plate respectively. Since $SiO_2$ is a poor thermal conductor relative to Si, increasing its thickness increases the thermal resistance between the device and the cold finger. This increases the maximum on-chip temperatures for a given heater power. Conversely, reducing $SiO_2$ thickness localizes on-chip heating, thereby increasing on-chip thermal gradients.

To generate on chip heating, heating elements were made on the chip using focused ion beam induced deposition (FIBID) of a C-Pt alloy. Each heater is a zig-zag pattern composed of 12 wires 5 μm long, 100 nm wide, and 150 nm thick which are spaced 1 μm apart (Fig. 1b). These long wires are connected (alternating top and bottom) by short wires 1.5 μm long, 100 nm wide, and 150 nm thick to form one ~ 71 μm long winding wire. These wires act as on-chip Joule heaters when voltages are applied to them. All heater wires were deposited simultaneously using the parallel deposition mode on the focused ion beam (FIB) at 24 pA ion beam current, 30 kV ion voltage, 307 pC/μm$^2$ dosage, and 150 % overlap. The use of parallel deposition increases the uniformity between components compared with serial deposition. The immediate electrical connections to the zig-zag heating element are also made using FIBID C-Pt. The next level of contacts are made using aluminum. The geometry of the immediate contacts is such that the heat generated in them is about two orders of magnitude lower than the heat generated in the zig-zag part of the heater.

To perform local measurements of these generated on-chip temperatures, five FIBID C-Pt thermometers were fabricated at five different locations on the sample across a 10 μm × 10 μm area (Fig. 1b). These on-chip cryogenic thermometers are described in detail elsewhere [27]. The thermometers are each 5 μm in length, 100 nm in width and 150 nm in thickness.

Electrical contacts were made to the thermometers via FIB deposited C-Pt electrodes and lithographically patterned Al leads. Indium assisted gold wire bonding was used to connect the Al pads to the sample stage (Fig. 1a). The sample was adhered to the copper sample stage using silver paint. The electrical contacts were then connected to room temperature electronics using phosphor-bronze twisted pairs. Pomona boxes with low pass RC filters with a bandwidth of 250 Hz were connected at room temperature to the electrical leads connected to the sample.

Each thermometer was individually calibrated against the $RuO_2$ thermometer mounted on the MC plate of the DR. This calibration was performed by measuring their resistance as a function of temperature via standard four-probes AC lock-in techniques using a frequency between 90 and 170 Hz and an excitation current of 100 nA. The thermometer calibration for the five thermometers is shown in Fig. 2. The thermometers have a resistance of ~ 1 kΩ in the temperature range of interest. Thus the temperature measurements using the 100 nA current will lead to a power dissipation of ~ 10 pW. The thermometers have a sensitivity (defined as $\frac{T}{V}\frac{dV}{dT}$) of 0.1–130 in the 100–500 mK range where the temperature measurements are made. The resistance remains temperature dependent down to 100 mK attesting to the fact that no thermal decoupling nor self-heating from the thermometer is occurring at these temperatures and excitation currents.

## 3. Results

### 3.1. Time taken to reach thermal equilibrium

A preliminary study was conducted to examine the system's behavior in terms of thermalization time and effects on the global temperature of the DR. It was observed that, at low heater powers (less than 4 μW), the heating remains local and the cryostat shows no increase in global temperature (measured by the $RuO_2$ thermometer on the MC). Conversely, above 4 μW the cryostat temperature begins to increase. This is because as the power applied to the heating element is increased,

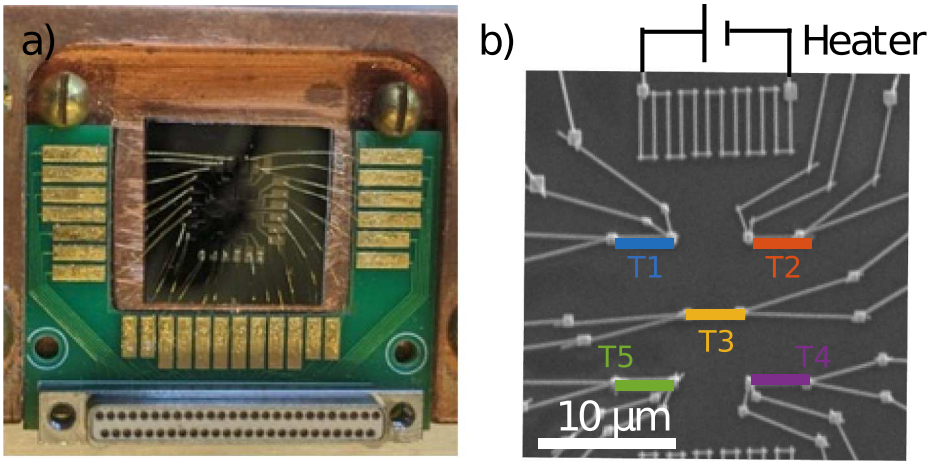


**Fig. 1.** a) Image of the sample mounted on a copper stage. Gold wires bonded to photolithographically patterned aluminum pads connect the sample to the measurement electronics. b) Scanning electron micrograph of the sample. The zig-zag lines on the top and bottom of the sample are used to generate on-chip heating. The 5 resistors between the two heaters marked in blue (T1), red (T2), yellow (T3), purple (T4), and green (T5) are used as on-chip thermometers.

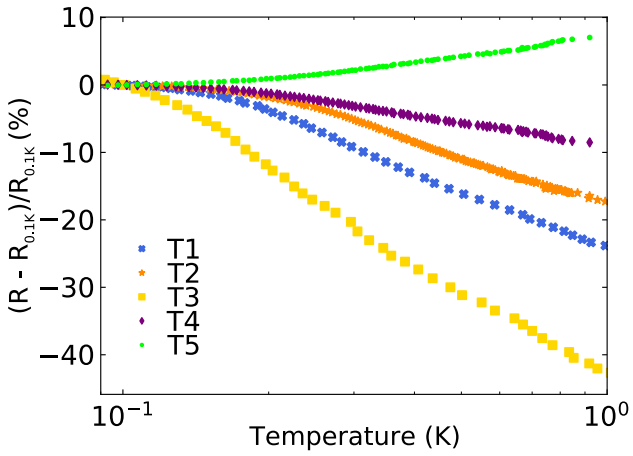


**Fig. 2.** Calibration data for C-Pt FIB deposited thermometers T1, T2, T3, T4, and T5 shown in Fig. 1b in the form of percent change in resistance $(R - R_{0.1K})/R_{0.1K}$. These resistive thermometers were calibrated against the built-in $RuO_2$ thermometer of the DR using a four-probe AC lock-in technique and an excitation current of 100 nA. The resistance at 0.1 K varies between 500 Ω for T1 and 4.25 kΩ for T5. Error propagation gives a lower resolution limit of 2.0 % for T1, 0.25 % for T2, 1.5 % for T3, 0.25 % for T4, and 0.24 % for T5 in this temperature range.

it eventually becomes greater than the cooling power of the cryostat. To avoid increasing the global temperature, powers less than 4 μW have been used in this study.

The time dynamics for heating and cooling were studied on a different sample from the one shown in Fig. 1 with the same substrate, heating component, and thermometer. Fig. 3 shows the measured resistance of the thermometer, 9.8 μm away from the heating element as a function of time after a DC voltage of 2 μW, applied to the heater, was turned on or off. Two thermal relaxation time constants are apparent for both heating and cooling. These are determined using a bi-exponential fit to the data. For cooling we find $\tau_{c,1} = 0.57$ s and $\tau_{c,2} = 157$ s, and for heating $\tau_{h,1} = 0.26$ s and $\tau_{h,2} = 225$ s. The two different time scales are hypothesized to be related to the difference in thermal resistance along the surface and perpendicular to the surface.

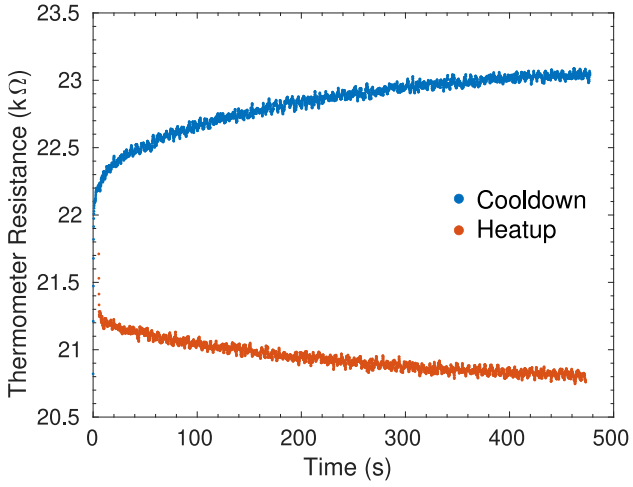


**Fig. 3.** Time dependence of the thermometer resistance for heating and cooling for a 2 μW applied DC heater power. This data was collected on a different sample with geometry identical to the one which is the primary focus of this study.

### 3.2. On-chip temperatures with DC power

To study on-chip temperatures in the presence of Joule heating, DC voltages of different magnitudes are applied across the heating resistor and temperatures are monitored using the 5 on-chip thermometers (see Fig. 1b). The resulting temperature at each thermometer as a function of heater power is given in Fig. 4a. The temperatures of all thermometers increase as a function of applied heater power by ∼ 100 mK even at the smallest heater powers (0.1 μW). The temperature of the sample increases rapidly as a function of heater power at temperatures below ∼ 0.5 K. Above ∼ 0.5 K, the temperature increase slows down and is linear as a function of heater power. This behavior is as expected since the electronic and phononic heat capacities drop off precipitously at low temperatures [37], as do the thermal conductivities of Si [1,2] and $SiO_2$ [3].

It is noteworthy that temperatures probed at T1, T2, and T3 are very similar. If the center-to-center distance is measured, T3 is found seen to be 4 μm further away from the heater compared with T1 and T2. If we assume that the heat spreads radially and the temperature gradient can be approximated to be linear, considering the small distances we are studying [38], the measured temperatures at T3 deviate by 2–20 % from the expected temperatures. The details of the metallic nano-structures in the area of interest are likely to impact the exact temperature distribution and make it vary from the assumed radial heat flow.

The difference in heating between the thermometers near the heater (T1 and T2) and the thermometers far from the heater (T4 and T5) results in a temperature gradient which changes as a function of heater power (Fig. 4b). The temperature gradient across the 10 μm distance between the two sets of thermometers is calculated as the difference between the average temperature measured on the hot and cold side of the sample area, $\frac{T_{T1}+T_{T2}}{2} - \frac{T_{T4}+T_{T5}}{2}$. The temperature gradient across the sample increases linearly, within measurement error, at a rate of 33 mK/μW between 0.1 μW and 4 μW applied heater power. In this region, thermal gradients between 0.1 and 0.3 K are generated. These thermal gradients are expected to grow even larger if the thermal conduction through the substrate is increased by using a thinner $SiO_2$ layer, for example. The Joule heater produces a negligible temperature difference in the transverse direction (left to right in Fig. 1), measured within the size of the heating element. The large thermal gradients perpendicular to the heater length can generate measurable charge, spin, and stress dynamics for many material and device configurations.

### 3.3. On-chip temperatures with DC power as a function of cryostat temperature

The temperature increase on the chip at T2, located 9.8 μm away from the heater (see Fig. 1b), as a function of heater power was measured at different cryostat temperatures (Fig. 5). For all cryostat temperatures below 500 mK, the temperature was found to increase even at the smallest applied powers (0.1 μW). At 500 mK, no on-chip heating effects were seen till 0.4 μW. Unsurprisingly, the heating effects are most prominent at the lowest temperatures. This large on-chip heating is a function of low cooling powers, low thermal conductivities, low heat capacities, as well as high boundary resistances at the lowest temperatures. At powers above ∼ 0.5 μW, on-chip heating was observed at all five cryostat temperatures measured here. It is worth noting though that even these high powers are much lower than the cooling power of the cryostat at these temperatures. At heater powers above 1.2 μW, the on-chip temperatures tend to saturate to the same value for all cryostat temperatures. This is because as the system warms up, the thermal conductivities and heat capacities become less sensitive functions of the temperature [1,3], leading to similar local heat dissipation dynamics regardless of cryostat temperature.

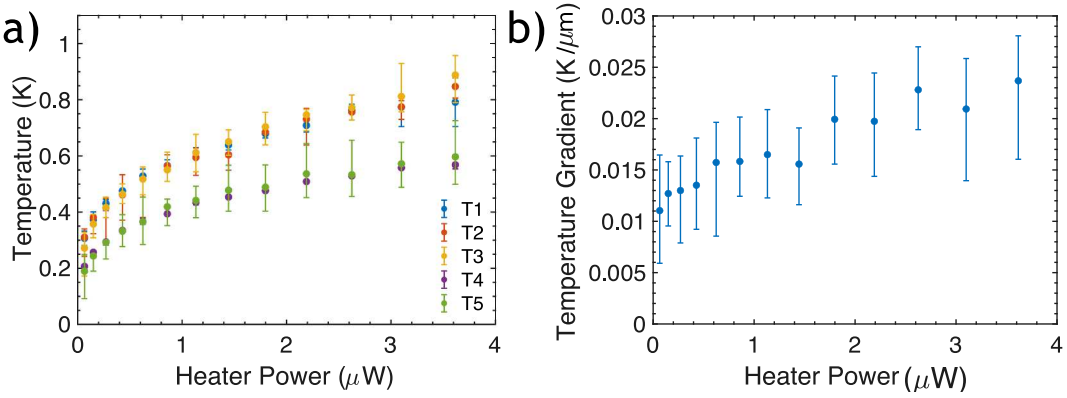


**Fig. 4.** a) Local temperature measured at five locations via C-Pt thermometry as a function of DC power applied to the top heating element (the sample with thermometers and heating elements is shown in Fig. 1b). For all measurements reported here, the temperature is obtained by averaging 200 voltage measurements and converting them to temperature using the thermometer calibrations. The errors shown are standard deviations in the voltage measurement propagated to temperature using standard error propagation. Since the thermometer sensitivity changes with temperature, so does the size of the error bars. b) Temperature gradient across 10 μm perpendicular to the heater length as a function of DC heater power.

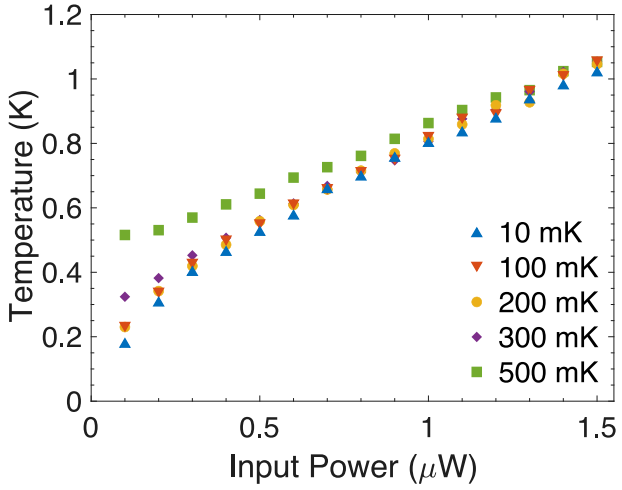


**Fig. 5.** On-chip temperature measured at T2, 9.8 μm away from the heating element as a function of input power at different cryostat temperatures.

### 3.4. On-chip temperatures with AC power

When an AC voltage is applied across the heating element, the average temperature in the region being monitored rises. In addition to the average rise, an oscillating temperature, with a frequency that is two times the frequency of the voltage applied to the heater, is generated. This oscillatory temperature forms the basis of many AC calorimetry techniques [39,40]. Fig. 6a shows the measured temperature response for a thermometer near the heater (red, T2) and a thermometer far from the heater (blue, T4) under the application of a 2 μW, 0.05 Hz power (1 $V_{pp}$ voltage). The DC temperature gradient is the difference in the offset temperatures ($T2_0 - T4_0$), marked as $\Delta T_{DC}$ in the figure. The AC temperature gradient, defined as the maximum of the time varying temperature gradient, is the difference between $T2_{amp}$ and $T4_{amp}$.

The DC component of the temperature gradient as a function of AC heater power is shown in Fig. 6b. The maximum AC temperature gradient as a function of heater power is given in Fig. 6c. Both the DC and AC temperature gradients increase as a function of applied heater power. The magnitude of the gradient as well as the rate of increase with applied power are an order of magnitude smaller than the gradients generated by applying DC power to the heater (see Fig. 4b). However, the absolute on-chip temperatures generated by the applied AC power, at these lowest frequencies, are comparable to those with DC power. The reason for the heat spreading more uniformly on the substrate's surface with AC heating is the highly non-linear dependence of thermal conductivity of the substrate on temperature [41]. As the temperature goes through one sinusoidal cycle ($temperature \propto sin(time)$), the phonon thermal conductivity varies as $(sin(time))^3$. The average thermal conductivity over this cycle, which is the value relevant for the AC heating, is

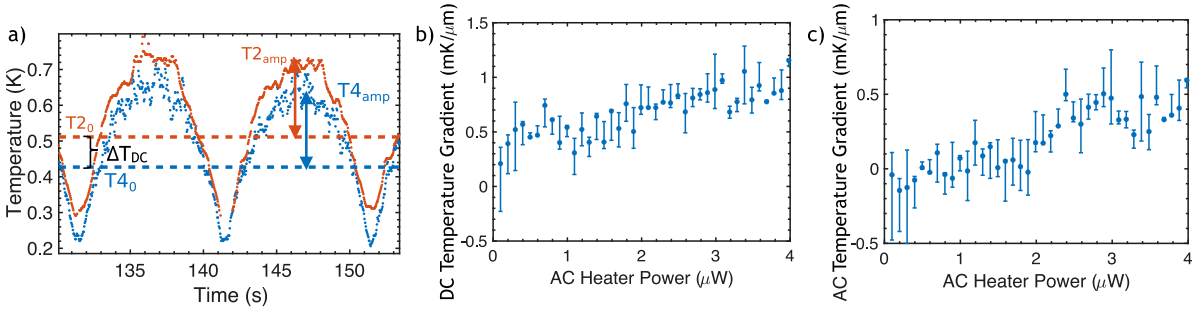


**Fig. 6.** a) Temperature wave resulting from a 2 μW voltage applied to the Joule heater at 0.05 Hz. The temperature as a function of time is shown in red for a thermometer near the heater and in blue for a thermometer far from the heater (T2 and T4 respectively, see Fig. 1b). For both waves, the temperature offset ($T_0$) is marked by a dashed line and the amplitude ($T_{amp}$) is indicated by a double arrow. b) DC temperature gradient across the 10 μm sample as a function of heater power. The temperature gradient is calculated as the difference between the average temperature offset of T1 and T2 and the average temperature offset of T4 and T5 $\left(\frac{T_{0,T1}+T_{0,T2}}{2} - \frac{T_{0,T4}+T_{0,T5}}{2}\right)$. c) AC temperature gradient across the 10 μm sample as a function of heater power. The temperature gradient is calculated as the difference between the average temperature amplitude of T1 and T2 and the average temperature amplitude of T4 and T5 $\left(\frac{T_{amp,T1}+T_{amp,T2}}{2} - \frac{T_{amp,T4}+T_{amp,T5}}{2}\right)$.

therefore greater than the thermal conductivity at the average temperature attained during this cycle, which is the value relevant for DC heating.

The frequency dependence of the measured temperature at T5 at an input power of 2 μW is shown in Fig. 7. Three interesting features are evident. First, the amplitude of the temperature oscillations decreases with increasing frequency. The thermal behavior of a small volume of the substrate can be modeled using the heat flow equation $P = C\frac{dT_m}{dt} - \kappa.\Delta T$ where P is the power input per unit volume, C is the specific heat per unit volume, $T_m$ is the temperature at the center of the volume, $\kappa$ is the thermal conductivity tensor, and $\Delta T$ is the thermal gradient tensor capturing gradients in various directions across the volume. Under the assumption that the temperature variations are small and that the thermal conductivity is constant, one can obtain that the amplitude of the temperature oscillations follows $\delta T \propto \left[1 + \left(\frac{f}{f_c}\right)^2\right]^{-\frac{1}{2}}$ [42], where f is the frequency of the applied voltage and $f_c$ is the cutoff frequency. The cutoff frequency is a measure of the time taken for thermal relaxation. It is found to be highly geometry dependent, varying between 10 Hz and 3 kHz for suspended $Si_3N_4$ membranes [42]. For this $Si/SiO_2$ substrate, $f_c \sim 0.7\ Hz$. A theoretical estimate of this cutoff frequency for the fairly typical measurement geometry being used in our experiment is challenging since the heat flows are non-trivial. Therefore, this experimental determination is particularly valuable. A second feature we observe is the increase in average temperature with increasing frequency. This has been observed before in thin films of copper [43]. The magnitude of the rise in average temperature, about 40 mK over two orders of magnitude increase in frequency, is also comparable to that given by the model in reference [43]. Finally, the temperature response differs from the expected sinusoidal shape [39], the difference increasing with increasing frequency. This is as expected from the thermal relaxation behavior seen in Fig. 3 since the relaxation time constant is larger than inverse of the frequencies in question.

From the measurements here, we can extrapolate that at even higher frequencies, the warming up of the chip remains non-oscillatory but rises to higher and higher steady state temperatures. Furthermore, these measurements set quantitative limits on frequency regimes relevant to the implementation of AC calorimetry techniques at these temperatures.

## 4. Conclusions

In conclusion, the current generated by the application of DC or AC voltages to a resistive element on a $Si/SiO_2$ substrate leads to substantial heating on the substrate's surface. The substrate is thermalized to the MC of a DR using best practices (gold plated, copper sample stage thermally anchored to the MC in multiple places, silver paint connecting chip to sample stage, etc.). The on-chip temperatures and temperature gradients are large even at relatively low powers, comparable to those regularly used in some electronic measurements. Below an applied power of ~ 4 μW, the global temperature of the cryostat, as measured by the $RuO_2$ thermometer on the MC, does not increase. The time scales for thermalization are impacted by sample anisotropy and two time constants ranging from seconds to several hundred seconds are found for both heating and cooling. At 0.1 μW power, AC or DC, local temperatures on the chip, microns away from the heat source are found to increase by 100s of mK. This effect is largest at the smallest cryostat temperatures and disappears for the lowest applied powers at ~ 500 mK. In addition, upon application of a DC voltage, large temperature gradients (100s of mK) are generated. With AC voltages, the heat is more uniformly distributed and therefore the gradients generated are smaller (10s of mK). These are significant heating effects and an underestimation of this heating could lead to misinterpretation of other experimental results or even failed experiments.

These measurements of the local, on-chip heating effects as a function of distance from the heating element, and power and frequency of the applied voltage delineate quantitative limits and constraints to be mindful of while designing cryogenic electronic experiments and are applicable to a wide range of studies.

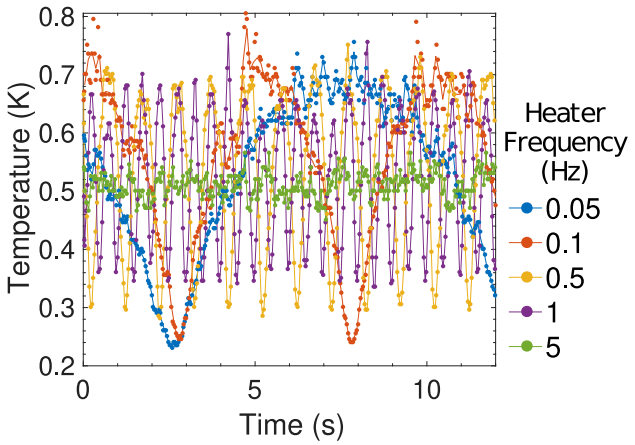


**Fig. 7.** Temperature measured using thermometer T5 (shown in Fig. 1b) upon application of a 2 μW input heater power for increasing frequency.

## 5. CRediT autorship contribution statement

**Kirsten Blagg:** Conceptualization, Methodology, Investigation, Writing - Original Draft, Visualization. **Antoine Castagnède:** Data analysis, Literature survey, Writing - Review & Editing, Visualization. **Meenakshi Singh:** Funding acquisition, Conceptualization, Methodology, Investigation, Data analysis, Supervision.

## Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

## Acknowledgements

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