

Electrostatic Shielding of NAND Flash Memory from Ionizing Radiation

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Abstract—In this paper, we propose and experimentally evaluate an electrostatic shielding technique to protect the health of flash memory cells from ionizing radiation effects. The technique is based on pre-programming the memory module instead of irradiating it in the erase condition. We find that erased cells suffer more oxide degradation compared to programmed cells, suggesting *pre-programming of memory modules before deploying in radiation-prone environments*. We evaluate cell degradation by performing retention test on the irradiated memory chip which reveals significantly quicker charge loss for memory cells that were in the erased state during irradiation.

Keywords—NAND Flash Memory; Data retention; Radiation.

I. INTRODUCTION

Total ionizing dose (TID) effect is a serious concern for flash memory operating in harsh environments [1]–[10]. Ionizing radiation not only causes charge loss from the floating gate, but also introduces trap states in the oxide layers of a flash memory cell [1]–[6]. Some of the trap states are permanent in nature and significantly degrade cell reliability such as data retention, endurance, and read noise. Hence, irradiated memory chips exhibit significantly poor reliability even if the memory was not storing any data in the radiation-prone environment. For example, previous studies show that data retention [1] and read noise [11] of commercial off-the-shelf (COTS) NAND memory significantly degrade after exposure to Gamma irradiation of a total dose of 50krad(Si).

Fig. 1(a) shows the schematic of a flash memory cell. A flash cell stores information in the form of charge in its floating gate (FG) or charge-trap (CT) layer. Fig. 1(b) shows the energy band diagram of a programmed memory cell with all terminals grounded. Ionizing radiation creates electron-hole pairs in the oxide layers [8]. Electrons leave the oxide layer due to the electric field, while holes get trapped creating trap states in the oxide layers [8]. During subsequent programming of the cell, these trap states may act as electron trapping site which degrades data retention property of the memory [1].

In this paper, we describe a technique based on pre-programming of memory bits to protect memory reliability from ionizing radiation effects, especially when it is not holding any useful data. We call this technique “Electrostatic Shielding” since it shields the oxide-channel interface from TID-induced damage. With this aim, we have studied data retention characteristics on multiple COTS 3D and 2D MLC NAND flash memory chips under room temperature baking experiment.

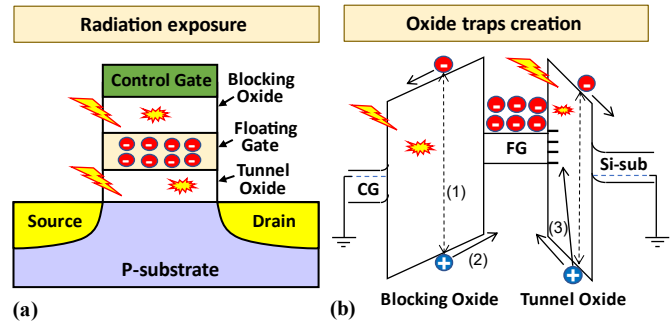


Fig. 1. (a) Schematic of a NAND flash memory cell. Ionizing radiation creates trap states in the oxide layers. (b) Energy band diagram of a programmed flash cell during irradiation with all pins grounded. The effects of ionizing radiation are shown: (1) electron-hole pair generation; (2) electron-hole recombination in the FG; and (3) holes trapping in the oxide layer creating trap states.

II. EXPERIMENTAL DETAILS

The experimental evaluation is performed on multiple COTS 3D MLC NAND (32-layers) and 2D MLC NAND (20 nm) flash memory chips. Table I summarizes the sample details. To interface the raw NAND chip with the computer, we used a custom-designed hardware board, as illustrated in Fig. 2(a). The board includes a socket to insert the NAND flash memory chip and an FT232H mini module from Future Technology Devices International (FTDI) to interface the memory chip with a computer through Universal Serial Bus (USB) connection. We follow the command sets defined by the Open NAND Flash Interface (ONFI) to perform basic memory operations such as read, write, and erase. The hardware setup allows us to access the raw memory bits without any error correction.

Fig. 2(b) shows experimental procedures. To evaluate the ionizing radiation effects on data retention characteristics, we first write data into several memory blocks (group-1) while leaving others in the erase state (group-2). Then, we expose the chips to radiation at the Sandia National Laboratories Gamma Irradiation Facility using a Co-60 source at a dose rate of 18.6rad(Si)/s up to 50krad(Si). Gamma irradiation is performed on packaged devices with all pins grounded. Note that we only expose raw NAND flash chips to Gamma irradiation while the hardware setup does not get exposed to irradiation. After irradiation, we erase and re-write the chips with a new random data pattern. Then, we read the chips periodically at room temperature and calculate the bit error rate (BER) to quantify and compare the retention errors from group-1 & -2 blocks.

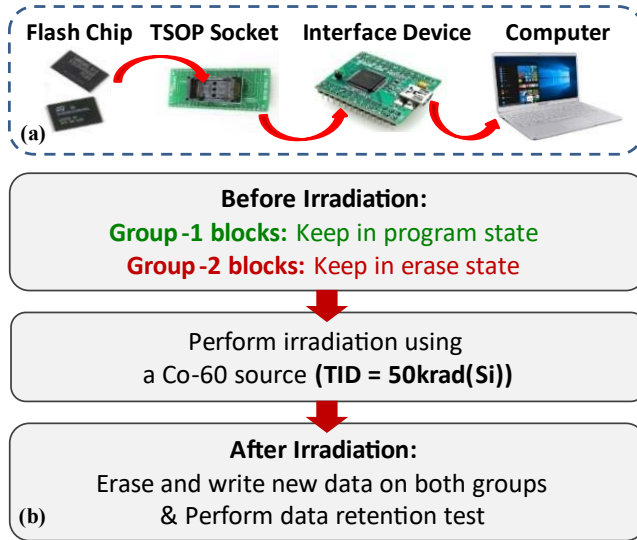


Fig. 2. (a) Experimental set-up. (b) Experimental procedures.

TABLE I. SAMPLE DETAILS

Sample	Details	Number of Block	Number of Page	Page Size	OOB Size
3D MLC	256Gb 32 layers	2,192	1,024	16,384	2,208
2D MLC	32Gb 20nm	2,128	256	8,192	744

III. BACKGROUND

The schematic of a 3D flash memory array is shown in Fig. 3(a). The green layers are the word lines (WLs) of the memory array while the purple pillars are the poly-silicon channel. The blue bottom layer is the silicon substrate, and the red lines at the top are the bit lines (BLs). The yellow bars on the substrate represent the select gate (SG) transistors. Similar SG transistors are also present at the top near the bit lines. Fig. 3(b) shows the circuit diagram of a 3D NAND flash memory structure. A 3D NAND flash memory chip typically contains thousands of flash blocks while each flash block consists of a fixed number of logical pages. Each logical page contains multiple flash cells. A 3D NAND flash memory cell is essentially a floating gate metal-oxide-semiconductor field-effect transistor (MOSFET) with gate-all-around (GAA) geometry [1]. The structure of a single 3D GAA geometry flash memory cell is shown in Fig. 3(c). A flash cell is in the programmed state (logic 0) when electrons are stored on the FG, whereas it is in the erase state (logic 1) when there are no electrons on the FG. The energy band diagram of the corresponding programmed memory cell is illustrated in Fig. 3(d).

It is generally known that flash memory reaches its lifetime when the ability to retain data or electrons in the FG becomes poor. This is due to trap states in the oxide layer. The location

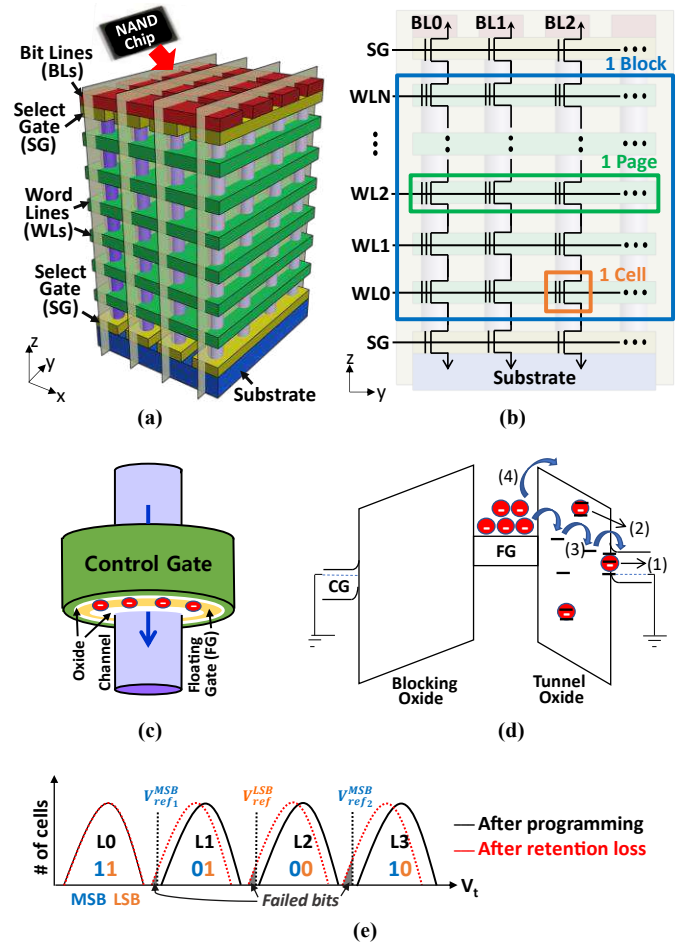


Fig. 3. (a) Schematic of a 3D NAND flash memory block. (b) Circuit diagram of a 3D NAND memory structure. (c) Structure of a single 3D GAA geometry flash memory cell. (d) Energy band diagram of the corresponding programmed flash cell under four data retention loss mechanisms: (1) interface trap recovery; (2) de-trapping; (3) trap-assisted tunneling (TAT); and (4) thermionic emission. The location of the trap states in the oxide layer can dictate the rate of data retention loss. (e) Typical V_t distribution of MLC NAND flash memory right after programming and after retention loss.

of trap states in the oxide layer is important as it can dictate the rate of data retention loss mechanism. We explain four fundamental retention loss mechanisms using the energy band diagram shown in Fig. 3(d). The first mechanism in Fig. 3(d) is called interface trap recovery. Due to the imperfection of the oxide-silicon interface, trap states can be created at the oxide-silicon interface layer [1], [12], [13]. Since the location of the trap states is close to the silicon substrate, the electrons trapped within these states are the quickest ones to escape, leading to data retention loss over time [1], [12]. The second mechanism in Fig. 3(d) is known as de-trapping. This mechanism happens due to the trap states located within the oxide layer. Once the electrons are trapped in these trap states, they can spontaneously escape out to the substrate over time, leading to retention errors. The third mechanism in Fig. 3(d) is called trap-assisted tunneling or TAT. TAT occurs when the stored

electrons in the FG layer travel back to the substrate by hopping through multiple trap states in the oxide layer, resulting in data retention loss [1], [12], [13]. Lastly, the charge loss mechanism-(4) in Fig. 3(d) is called thermionic emission. This mechanism takes place when the stored electrons on the FG escape to the substrate through thermionic emission over the FG-oxide barrier. Since the barrier height is high, this mechanism contributes the least amount of charge loss at room temperature [1], [13]. All these data retention loss mechanisms become dominant as more trap states are created in the oxide layer during ionizing radiation exposure [1]. More discussion on the charge loss mechanism can be found in the previous studies [1], [12].

Fig. 3(e) illustrates the V_t distribution of MLC NAND flash memory. The distribution in black color represents the distribution right after programming while the red color represents the distribution after retention loss. Generally, three different read reference voltages (i.e., V_{ref1}^{MSB} , V_{ref}^{LSB} , and V_{ref2}^{MSB}) are used during read operation to determine the states of flash cells. As the flash cells lose the stored electrons, the V_t distribution shifts to the left and the read reference voltages fail to determine the cell's state correctly causing retention errors. This phenomenon is illustrated in Fig. 3(e), where the shaded area represents the total error bits.

IV. RESULTS AND DISCUSSION

In this section, we present the retention test results from the irradiated chip to illustrate the benefit of pre-programming a memory module (or electrostatic shielding technique) before deploying it to radiation-prone environments.

Fig. 4(a) compares the room-temperature data retention error from the irradiated 3D NAND chip with a non-irradiated 3D NAND chip. We observe a very low retention error ($<10^{-3}\%$) from the non-irradiated chip even after 1000 hours. However, a significantly higher retention error is observed in the irradiated chip. Interestingly, we find that group-1 blocks of the irradiated chip show relatively superior retention characteristics than group-2 blocks even though both of them undergo the same amount of TID. Therefore, we conclude that irradiation effects significantly degrade the data retention property of memory chips. More importantly, the cells that were in the erase state during irradiation (group-2) suffer higher degradation than the cells that were in the programmed state (group-1).

We explain the results using energy band diagrams in Fig. 4(b)-(e). Fig. 4(b) illustrates the energy band diagram of the programmed cell during irradiation. Note that irradiation-induced holes in the tunnel oxide move toward the FG direction due to the electric field created by the FG charge. This phenomenon creates trap states in the oxide layer near the FG. Trap states near the FG and tunnel oxide interface are less harmful compared to the trap states near the tunnel oxide and silicon channel interface. Therefore, we observe an

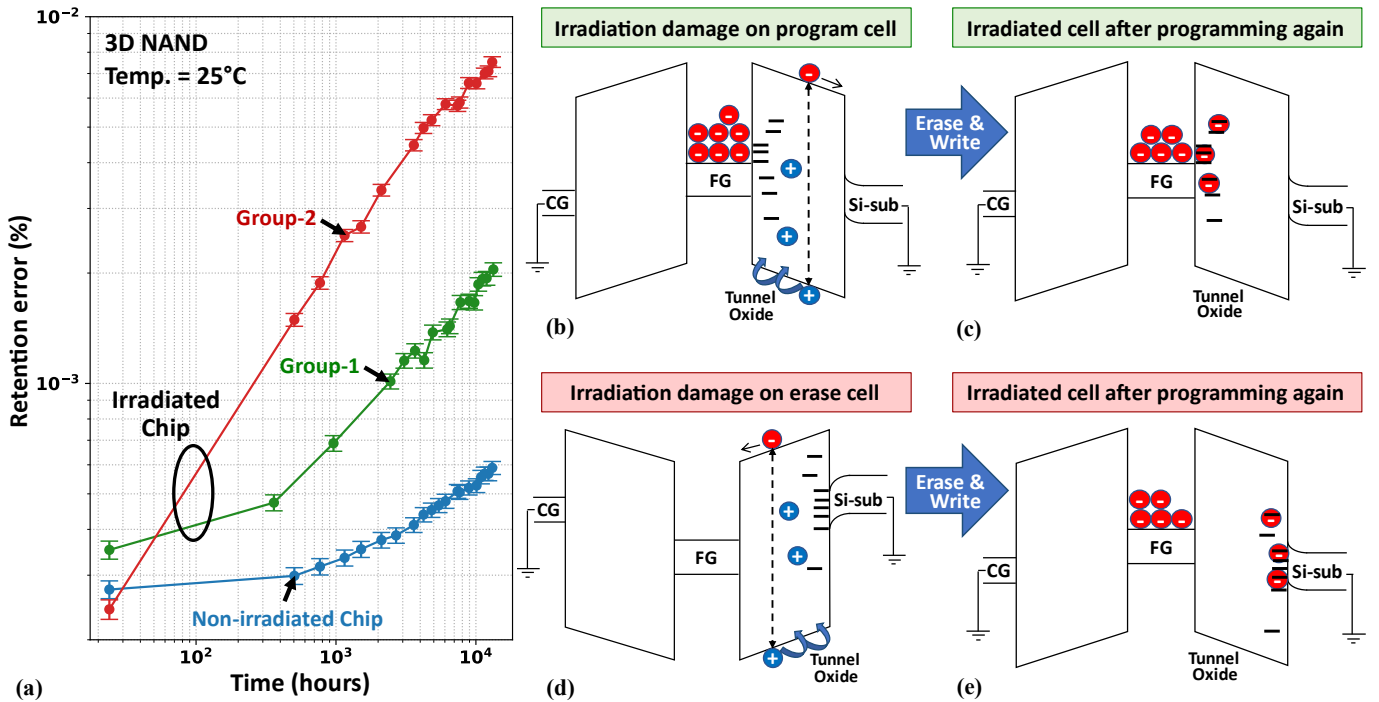


Fig. 4. (a) Plot of 3D MLC retention error vs. time in hours when the chip is left at room temperature. (b) Energy band diagram of a programmed cell during irradiation, where traps are created near FG and tunnel oxide interface. (c) Energy band diagram of the irradiated programmed cell after erase and write again. (d) Energy band diagram of an erased cell during irradiation, where trap states are formed near the tunnel oxide-silicon channel interface. (e) Energy band diagram of the corresponding cell after write operation. Note that electrons are trapped near tunnel oxide and silicon channel interface degrading its retention.

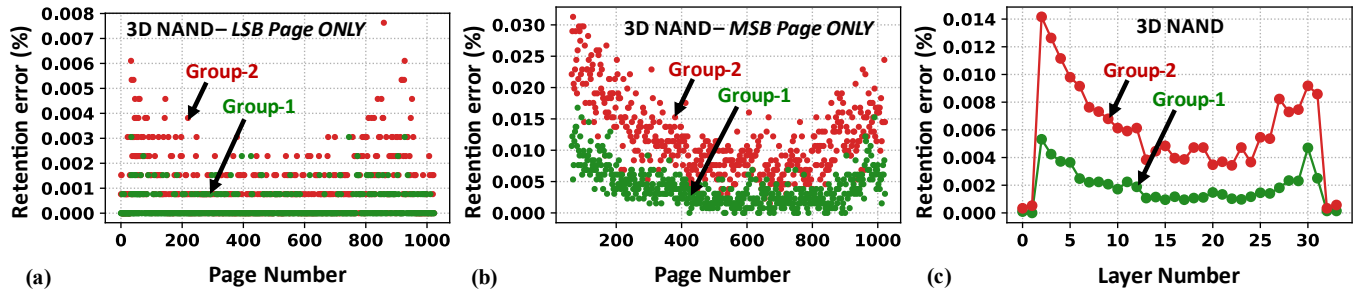


Fig. 5. (a) Plot of retention error of 3D NAND chip vs. page number from *LSB page only*. (b) Plot of retention error of 3D NAND chip vs. page number from *MSB page only*. (c) Plot of retention error vs. layer number of 3D NAND chip.

improvement in data retention characteristics of flash cells in group-1 (programmed state during irradiation) compared to group-2 (erase state during irradiation). However, due to the trap states near the FG in the oxide layer (Fig. 4(c)), the data retention characteristics in group-1 are poor when compared to the non-irradiated chip. Note that the oxide traps in the non-irradiated chip are presumably lower compared to the irradiated chip and hence they exhibit minimum retention errors.

On the other hand, energy band diagrams in Fig. 4(d)-(e) explain the data retention behavior of group-2 memory blocks. During irradiation, holes in the tunnel oxide move toward the silicon substrate in the erased memory cell. This phenomenon creates trap states near the tunnel oxide-silicon interface. The interface traps near tunnel oxide and silicon channel are more harmful to data retention because the trapped electrons at this interface area are more susceptible to escape during the retention period. Therefore, the erased memory cells suffer more degradation in their retention characteristics after irradiation. As a result, we observe the worst data retention characteristics for the group-2 memory blocks.

Fig. 5(a)-(c) show retention errors of the 3D MLC NAND memory chip with respect to its logical page number. Since MLC memory stores two bits of information in a cell, it has two types of logical pages which are called the Least Significant Bit, or LSB page, and the Most Significant Bit, or MSB page. Fig. 5(a) shows retention errors from LSB pages, whereas Fig. 5(b) plots retention errors from MSB pages. Retention errors are typically higher on MSB pages as they involve higher V_t state which loses charge quicker than the lower V_t state. In Fig. 5(a)-(b), under the same period of data retention at room temperature (~13,000 hours), we observe that there are two noticeable groups of retention error, where retention error from pages in group-2 is higher than that of group-1. Moreover, in Fig. 5(c), we find that all the layers of the group-1 memory perform better than the group-2 memory indicating the effectiveness of the electrostatic shielding across all memory layers and logical pages.

We further analyze the data retention characteristics in 2D MLC NAND flash memory chips. The experimental results are shown in Fig. 6(a)-(b). We observe the same trend between group-1 & 2 blocks. This implies that electrostatic shielding is applicable for both 2D and 3D NAND memories. Therefore, we conclude that leaving the memory chip in the programmed state

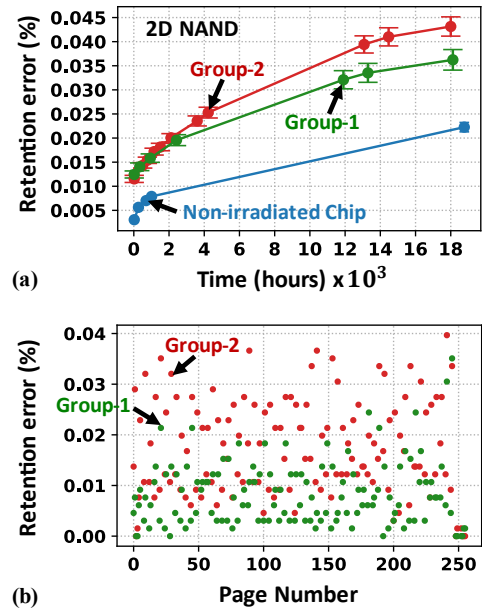


Fig. 6. (a) Plot of retention error vs. time in hours of 2D MLC chip when the chip is left at room temperature. (b) Plot of 2D NAND retention error vs. page number from *LSB page only*.

during irradiation helps reduce damage from the TID, leading to relatively improved retention characteristics.

V. CONCLUSIONS

The key findings of this paper are as follows:

- (1) Experimental evaluation on COTS 3D and 2D MLC NAND flash memories reveals that data retention characteristics of flash memory significantly degrade after irradiation.
- (2) We find that irradiating the memory cells in the erase state is more harmful than the programmed state, suggesting pre-programming of memory modules before deploying in radiation-prone environments.
- (3) We explain the observed results based on radiation-induced trap location in the tunnel oxide layer.

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