11.5 A 21W 94.8%-Efficient Reconfigurable Single-Inductor Multi-Stage Hybrid DC-DC Converter

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The ongoing demand for smaller form factors and faster charging times of mobile products continue to drive the need for efficient, high-density power delivery (PD) for charging with a wide input voltage (V_{IN}) range of 5V to 20V, offered by USB-C PD. A converter solution that efficiently takes advantage of this wide V_{IN} range while providing an output voltage (V_O) range suitable for battery charging (2.8V to 4.2V) remains challenging but highly desirable. Hybrid converters and their benefits such as inductor size reduction and small V_O/V_{IN} voltage conversion ratios (VCRs) at high efficiency provide a path to meet this challenge. While recent commercial [1] and research works [2–4] have demonstrated these benefits, their limited V_{IN} or VCR ranges are unable to take full advantage of USB-C PD or have the inductor located at the high output current (I_O) path [1–3] where DCR conduction losses can become significant for small footprints.

To address these shortcomings, this paper presents a single inductor multi-stage (SIMS) hybrid converter that efficiently provides VCRs needed for battery charging across the wide V_{IN} range while moving the inductor away from the high I_O path. Figure 11.5.1 shows the converter concept and topology where an inductor, L, couples two switched capacitor (SC) stages to provide soft charging benefits to each stage while also reducing the DC inductor current (I_L) to a level equal to I_O scaled down by the conversion ratio of the 2nd stage (M_2). As shown in Fig. 11.5.1, the converter has 4 main operating modes: Lower Series-Parallel (LSP), Lower Parallel-Series (LPS), Upper Parallel-Series (UPS), and Bypass Parallel-Series (BPS). While BPS mode has 2 unique switching states, the other modes have 3 unique states in one switching period (T_S). The inductor is charged with a duty cycle (D) twice in a T_S and discharged in the remaining time. The 1st stage operates at $f_S = 1/T_S$ when active while the 2nd stage operates at $2f_S$. In the LSP, LPS, and UPS modes C_1 is fully soft charged while in BPS mode, C_1 is repurposed as a V_{IN} bypass capacitor. In all modes, C_2 is partially soft charged by L then hard discharged into V_O. The steady-state waveforms in Fig. 11.5.2 show the modes allow 3 voltage levels at the LX node (V_{IN}, $V_{IN}/2$, or 0V) and 2 voltage levels at the C2P node (V_O or $2V_O$) which determine the I_L's di/dt. The I_L plots show the inductor I^2R losses are significantly reduced even at moderate I_O levels (1A) compared to a topology using the same inductor at the output with comparable ripple. These savings continue to quadratically increase at higher loads.

The VCR versus D plot in Fig. 11.5.2 illustrates the topology is theoretically capable of VCRs spanning 0 to 1 across modes. Additionally, modes with intersecting VCRs (i.e., LSP and LPS modes) provide an opportunity to extend the VCR range while minimizing conduction losses by automatically detecting when D=0.5 and inverting the 2nd stage operating phases (Auto mode). The relationship between conduction losses and modes is also shown in Fig. 11.5.2 where R_0 is the equivalent output resistance representing conduction losses in the DC transformer model of the converter. It shows R_0 increases exponentially as the hard charge loss of the 2nd stage begins to dominate. By selecting a mode that meets VCR requirements with smaller R_0, these regions can be avoided.

The power stage implementation is shown in Fig. 11.5.3. Switches S1–S4 are 12V devices since they block $V_{IN}/2$, while S5–S7 are 5V devices since they block V_O. The linear regulator (HS REG) generates a voltage 5V below V_{IN} to power the S1–S2 gate drivers while also limiting the gate drive swing below their V_{SG} rating. It is also used to refresh S2's bootstrap capacitor (C_{B2}) through diode D0 when S1 is on. S3's gate driver is powered by C_{B3} and is refreshed by V_{DD} and D1 when S4 is on. The gate drivers for S5–S6 are powered from C_2 while S7's driver is powered from V_O. The schematic for the level shifters is also shown in Fig. 11.5.3 and consists of a current controlled push-pull output stage with the HV devices functioning as HV blocking cascodes. When idling, the state of the level shifter is maintained with a small bias current, I_{BL}, to reduce quiescent current. During output or flying domain supply (V_{DDH}/V_{SSH}) transitions, the HC_PUL signal briefly pulses a high bias current, I_{BH}, to increase speed and provide high dV/dt immunity.

While C_2 does not require active voltage balancing since it is hard discharged to V_O each cycle, C_1 does when active and is susceptible to V_{C1} drift due to power stage timing and impedance mismatches. The balancer and V_O regulation implementation, shown in Fig. 11.5.3, utilizes a modified approach from [5] where the V_O loop sets the common mode of the error signals, BP and BM, which determines the duty cycles of the PWMA, PWMB, and switch control signals. The balancer loop then produces a small differential voltage between BP and BM to finely adjust the switch timing to regulate V_{C1} to $V_{IN}/2$. This allows the balancer and V_O loops to be independently compensated since the balancer compensation (Z_{C_B}) does not appear in the common mode path of the V_O loop. Figure 11.5.4 shows the measured performance of the balancer.

For modes that utilize the 1st stage, pre-charging (PC) is necessary during start up to ensure no switches are stressed as V_{IN} turns on and $V_{C1} = V_{IN}/2$ before PWM begins. The implementation of the 1st stage PC circuit is shown in Fig. 11.5.4. When PC is enabled (PC_EN = 1), switches S1, S4, and S_{PC} are on. This ensures V_{C1} tracks V_{IN} until it reaches $V_{IN}/2$. S1 is then turned off and V_{C1} is regulated to $V_{IN}/2$ by the comparator loop and the small switch S_{PC}. C_{B2} is also pre-charged to ensure that S2 remains off during start-up and its gate driver is properly powered before PWM begins. While S1 or S_{PC} can refresh C_{B2} when on, a current sink also produces a small bias current to ensure it remains charged regardless of the states of S1 and S_{PC} by drawing charge from C_1. The Zener diode ensures the voltage of C_{B2} remains near 5V. The PC functionality and start-up sequence are demonstrated in Fig. 11.5.4 where V_{C1} initially tracks V_{IN} until it reaches 10V. V_{IN} then continues to 20V while V_{C1} is regulated to 10V by the PC control loop. PWM is then enabled (PC_EN = 0) and the V_O regulation reference voltage, V_{REF}, is ramped up to its final value. The 2nd stage gradually enters normal operation as V_O ramps up.

As previously noted in Fig. 11.5.2, to extend the VCR range while minimizing R_0, Auto mode can be utilized to switch between LSP and LPS modes by detecting when D = 0.5 and inverting the 2nd stage operation from the previous mode. However, care must be taken during this transition since at D = 0.5 the I_L ripple of LPS mode is twice that of LSP mode. An example LSP-to-LPS transition is shown in Fig. 11.5.5. where a mode transition occurs synchronously but results in a large step change in the average value of I_L which could result in significant V_O perturbations. To minimize the magnitude of this step change, an active current shaping (ACS) technique shown in Fig. 11.5.5 is employed where I_L is gradually transitioned to the nominal peak value for the subsequent mode. The ACS implementation and relevant waveforms are shown in Fig. 11.5.5. A hysteretic comparator is used to detect when the V_O regulation error amplifier output, V_{REG}, is above or below V_{M_REF} which is equal to the average of the PWM oscillator waveform, V_{OSC} (i.e. the point of D = 0.5). The comparator output is gated by the RU (ramp-up) signal from the oscillator which forces the converter to remain in the previous mode for $T_S/8$ before transitioning to the next mode by asserting the PS2_INV signal, resulting in the inversion of the operation of the 2nd stage for the next mode. The measured Auto mode with ACS performance during a load step induced LSP-to-LPS transition is shown in Fig. 11.5.5, where I_L is properly shaped to the next mode. The V_O droop, which includes the combined effects of the load current and mode change, is limited to 200mV. The same test was repeated for the fixed LSP and LPS modes which resulted in 160mV of droop, indicating the Auto mode with ACS transition adds only 40mV of droop to the transient response. The same ACS method is applied for the LPS-to-LSP transition with similar results.

A prototype was fabricated in a 0.18µm BCD process with 9.4mm² die area (Fig. 11.5.7). The measured power efficiency vs. I_O plots across all modes with a 2.2µH (35mΩ DCR) inductor and f_S=600kHz (1.2MHz at inductor) in Fig. 11.5.6 show it achieves a peak efficiency of 94.8% and a peak output power of 21W while maintaining peak efficiencies >89.5% across all modes from a V_{IN} of 5V-24V. The LSP and LPS mode plots with V_{IN}=20V also illustrate the VCR extension provided by Auto mode. A comparison table is provided in Fig. 11.5.6. The prototype extends the V_{IN} range by >88% compared to [1] and achieves wider VCR ranges over [2–4] while reducing inductor conduction losses.

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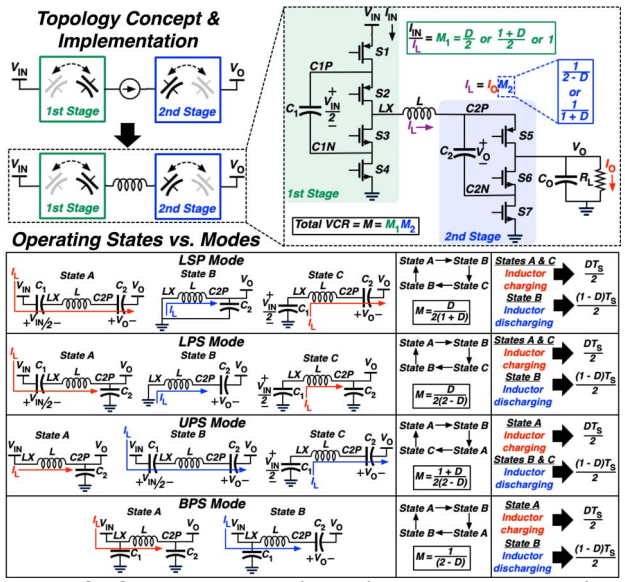


Figure 11.5.1: SIMS converter concept (top left), power stage topology (top right), and operating states versus modes (bottom).

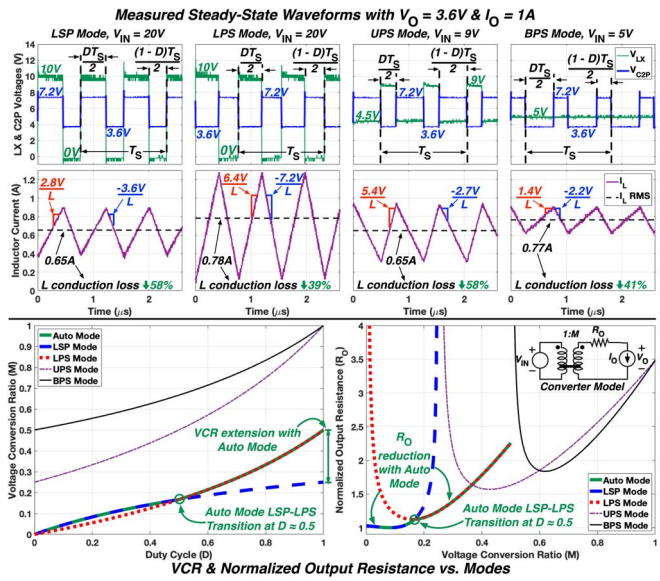


Figure 11.5.2: Measured steady-state operating waveforms (top), ideal VCRs vs. D (bottom left), and normalized output resistance versus VCR (bottom right).

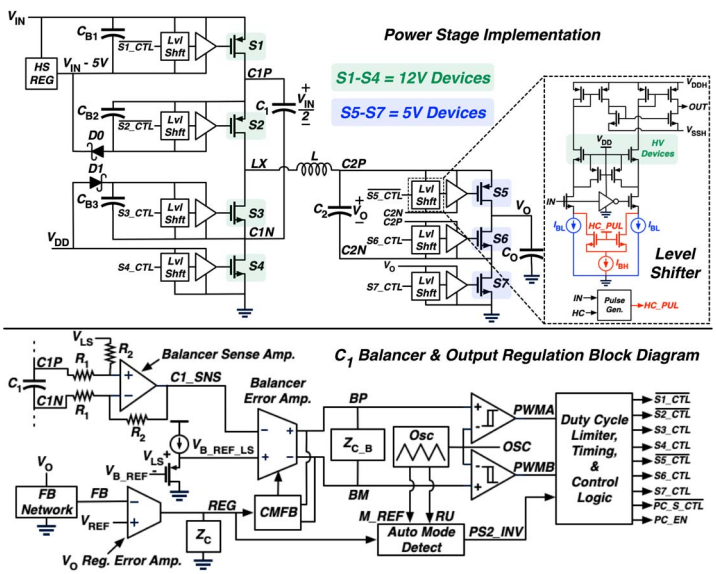


Figure 11.5.3: Power stage gate drive implementation (top left), level shifter circuit (top right), and C_1 balancer/V_O regulation control diagram (bottom).

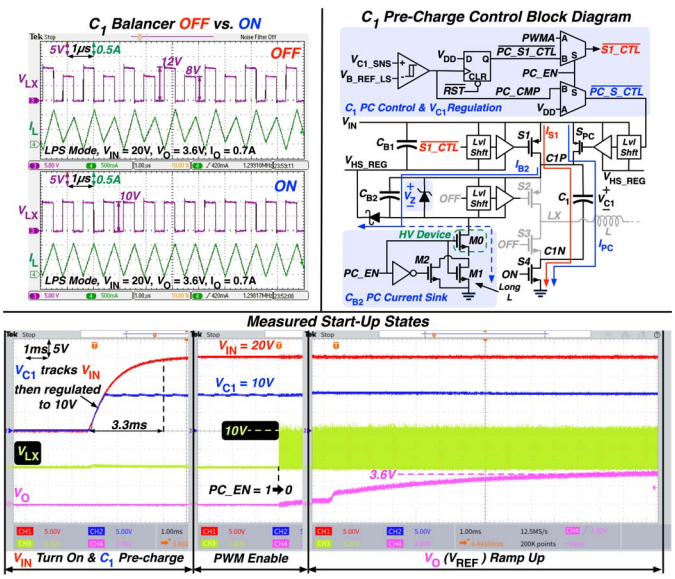


Figure 11.5.4: Measured C_1 balancer operation (top left), C_1 pre-charge control diagram (top right), and measured start-up waveforms for LPS mode (bottom).

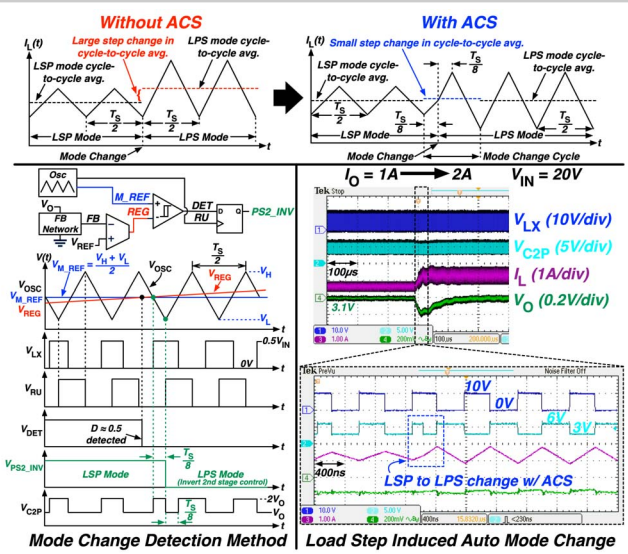
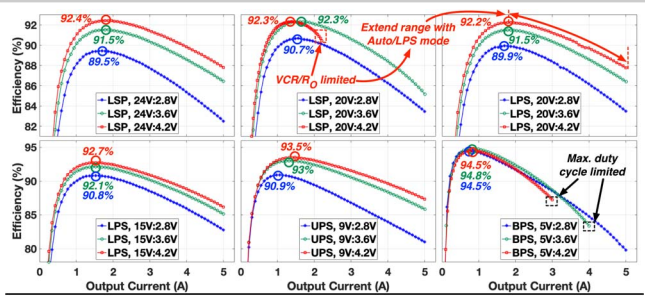


Figure 11.5.5: Auto mode ACS concept (top), duty cycle detection circuit & waveforms (bottom left), measured ACS during load transient induced mode change (bottom right).



	TI BQ25910 [1]	ISSCC '21 [2]	ISSCC '20 [3]	JSSC '19 [4]	This work
Topology	3-level Buck	Hyb. Casc. SC	Tri-State DSD	FIH	**Re-Cfg SIMS**
Technology	NR	180nm	180nm BCD	130nm BCD	**180nm BCD**
Inductor Location	Output	Output	Output	Input	**Middle**
V_{IN}/V_O Range	3.9-14V/2-4.8V	4-6V/0.4-1.2V	12-24V/1V	9V/3-4.2V†	**5-24V/2.8-4.2V**
Peak I_O/P_O	6A/22W^	1A/1.1W	3A/3W	3.4A/12.2W†	**5A/21W**
Pre-Charge?	Yes	Yes	Yes	No	**Yes**
Est. DC biased C_{FLY}	5.8µF^	3.2µF+6.4µF	1µF+1µF††	6.6µF+13µF	**5.8µF+10µF**
Inductor (DCR)	0.47µH (17mΩ)	0.24µH (NR)	2x560nH (NR)	1µH (5.5mΩ)†	**2.2µH (35mΩ)**
Max. Power Density*	1.64W/mm²^	0.1W/mm²	0.48W/mm²**	0.44W/mm²†^	**0.86W/mm²**
Max. Eff. (at VCR)	95.4% (0.76)	96.9% (0.24)	91.2% (0.08)	94.3% (0.4)†	**94.8% (0.72)**
Min. VCR (at Eff.)	0.14 (NR)^	0.08 (85.5%)	0.04 (88.3%)	0.33 (NR)	**0.12 (89.5%)**

^ Estimated from reported data. NR: Not reported
* Area counts flying caps., inductors, and die areas. † Reported V_{O1} performance with discrete inductor.
** Area counts die area only. †† Only nominal values reported.

Figure 11.5.6: Measured power efficiency versus I_O for different modes, and performance summary and comparison table.

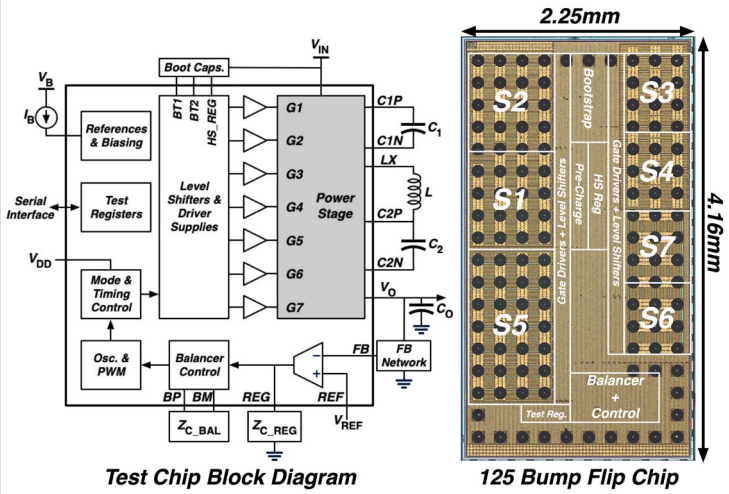


Figure 11.5.7: Test chip block diagram and die micrograph.

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