Total Ionizing Dose Effects on the Power-Up State of Static Random-Access Memory

Umeshwarnath Surendranathan, *Student Member, IEEE*, Horace Wilson, *Student Member, IEEE*, Maryla Wasiolek, Khalid Hattar, *Member, IEEE*, Aleksandar Milenkovic, *Senior Member, IEEE*, and Biswajit Ray, *Senior Member, IEEE*

***Abstract*— Power-up states of static random-access memory (SRAM) memories are often used for generating physical unclonable functions (PUFs) in a variety of integrated circuits. The integrity of PUFs derived from commercial SRAM memories in radiation-prone environments has been recently recognized as an important problem and it remains an open issue. We perform both experimental evaluation and simulation analysis to quantify the effects of irradiation on the power-up state of commercial SRAM chips. Our results show that SRAM-PUF is significantly altered after irradiation, thus limiting its use in radiation-prone environments. The SRAM-PUF bit error rate (BER) increases monotonically with an increase in the total ionizing dose (TID), exceeding 15% after 100 krad(Si). We observe small annealing effects over time, but the BER remains high even five months after irradiation.**

***Index Terms*— Ionizing radiation, physical unclonable function (PUF), static random-access memory (SRAM).**

I. Introduction

PHYSICAL unclonable function (PUF) is an important hardware security primitive that serves as a unique device identifier, a device-specific cryptographic key, or a device fingerprint. Semiconductor PUFs typically exploit manufacturing process variation in the CMOS circuits to generate a device-specific random signature that is robust and repeatable. The power-up state of static random-access memory (SRAM) was proposed for generating PUFs more than a decade ago [1], [2]. As SRAM memories are ubiquitous in a variety of electronic systems, SRAM-based PUFs have been widely adopted in commercial electronic systems [3], [4], [5], [6].

Radiation effects on PUFs have recently gained significant attention with the prospect of satellite Internet constellations that will require radiation-hardened hardware security primitives [7], [8], [9], [10]. In this context, evaluating radiation effects on SRAM PUFs is very important. Even though SRAM memory operations are quite robust against ionizing radiation effects, its power-up state (and hence PUF) might change significantly with irradiation [10], [11], [12], [13], [14]. For example, Su et al. analyzed the radiation effects on an SRAM-PUF built using the fully depleted silicon-on-insulator (FDSOI) process [11]. Their study shows an increased number of unstable PUF bits after irradiation. However, the study does not provide an analysis of the SRAM-PUF before and after irradiation, so the changes in the original PUF due to irradiation remain unclear. Similarly, Calienes et al. [15] studied the radiation tolerance difference for single-event effects between bulk and FDSOI SRAM devices. Interestingly, Zhang et al. [14] proposed irradiating chips as a means to improve the total ionizing dose (TID) response of SRAM-PUFs. Lawrence et al. [10] recently performed a detailed analysis of radiation effects on SRAM-PUFs derived from commercial off-the-shelf (COTS) SRAM chips. Our work builds on their study and expands it as follows: 1) we consider multiple COTS SRAM chips with a parallel memory interface rather than a single family of devices with a serial interface; 2) we use Co-60 gamma rays for irradiation experiements rather than X-rays and neutron irradiation; 3) since our chips remain responsive at higher doses, we report the chip performance up to 200 krad(Si); and 4) we elucidate the effects of irradiation using an HSPICE SRAM cell model.

In this article, we analyze and characterize the effects of ionizing radiation on SRAM-PUFs derived from power-up states of COTS SRAM chips from two different vendors. We quantify the effects of irradiation on SRAM-PUFs by measuring the Hamming distance (HD) between a GoldPUF and its corresponding authentication counterparts extracted before and after irradiation. We find that HD steadily increases with an increase in TID, indicating that SRAM-PUFs are not sufficiently robust in radiation-prone environments. To elucidate the effects of radiation on SRAM-PUF, we use an HSPICE model of SRAM cells. We simulate the transient current waveform during the power-up phase of an SRAM cell, which illustrates the mismatch effects between the cross-coupled inverters to determine the power-up state. We also explain the irradiation effects on SRAM-PUF by connecting the fundamental device physics of individual transistors under irradiation, such as oxide trapping

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Umeshwarnath Surendranathan, Horace Wilson, Aleksandar Milenkovic, and Biswajit Ray are with the Department of Electrical and Computer Engineering, The University of Alabama in Huntsville, Huntsville, AL 35899 USA (e-mail: us0003@uah.edu; hjw0011@uah.edu; milenka@uah.edu; biswajit.ray@uah.edu).

Maryla Wasiolek is with the Sandia National Laboratories, Albuquerque, NM 87185 USA.

Khalid Hattar is with the Department of Nuclear Engineering, University of Tennessee-Knoxville, Knoxville, TN 37902 USA.

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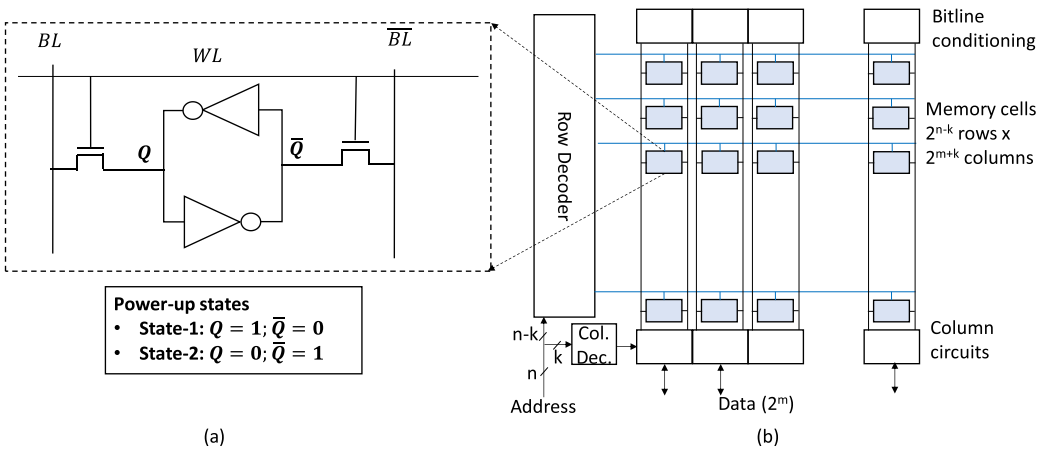

Fig. 1. (a) Schematic of a 6T SRAM cell. (b) SRAM array.

effects. We provide a simple classification method of PUF bits and explain how they get affected by irradiation.

The rest of this article is organized as follows. Section II provides a brief background of SRAM memory technology. Section III describes our experimental setup and experimental flow used in this research. Section IV presents the results of the experimental evaluation and discusses their implications. Finally, Section V concludes this article.

II. Background

A basic building block of an SRAM chip is an SRAM cell that holds 1 bit of information. The common SRAM cell known as the six-transistor (6T) cell consists of a cross-coupled CMOS inverter pair along with two access transistors, as shown in Fig. 1(a). The cross-coupled inverter pair has two stable states corresponding to logic 0 and 1, as shown in Fig. 1(a). After power-up, SRAM cells can end up in either state, depending on discrepancies in the size and drive strength of transistors in cross-coupled inverters. These discrepancies are an artifact of minuscule process variations that are unique for each chip [16], [17], [18], [19].

An SRAM chip contains an array of memory cells, as shown in Fig. 1(b). The chip with n address inputs and 2^m data lines is seen logically as an array of $2^n \times 2^m$ cells. For chip floor planning reasons, the array is physically organized into $2^{n-k} \times 2^{m+k}$ cells and an additional column decoder is used to select a word from the selected row. In addition to address and data pins, an SRAM chip has a control input for controlling read and write operations. To read from SRAM, bitlines are precharged and the selected wordline is turned on. One of the two column bitlines will be pulled down by the cell and that is sensed by the corresponding column circuitry. To write to SRAM, the bitlines are driven based on the content from data pins (e.g., BL $= 1$ and $\bar{BL} = 0$) and the word line is turned on. The bitlines overpower the selected cells, thus writing a new value.

The power-up state of the cells in the array is random and unique for each SRAM block. This power-up state can be used for generating SRAM-based PUFs or fingerprints. The power-up states, repeatedly captured on the same chip or an SRAM block, produce similar random sequences of bits, albeit not identical, as some memory cells change their power-up state due to electric noise. We generate five instances of the power-up state and perform a bit-by-bit comparison to create the reference GoldPUF. If there is a mismatch in any bit position of the five power-up states, we use the majority voting to decide the value of the GoldPUF bit. To quantify mismatches between the GoldPUF and any subsequent power-up state, we measure the intradie HD as follows:

$$\text{HD} = \frac{\#\text{ of set bits (GoldPUF XOR CurrentPUF)}}{\text{Total \# of PUF bits}}. \quad (1)$$

Hamming weight (HW) is another important metric that is computed as the percentage of cells with the power-up state at logic 1. Ideally, the HW of SRAM-PUFs is 50%.

TABLE I
Summary of Chip Specification

Manufacturer	IDT	Cypress
Part number	IDT71V416S	CY7C1041C
Capacity	4 Mbits	4 Mbits
Supply voltage	3.3 V	3.3 V
Word size	16 bits	16 bits
Tech. node	130 nm	150 nm
Timing	10 ns	10 ns

III. Experimental Setup and Flow

We use COTS SRAM chips from Integrated Device Technology, Inc. (IDT71V416S) and Cypress (CY7C1041C) for our tests. They are both 256k $\times$ 16-bits SRAM chips. Table I describes the main characteristics of both chips. They are functionally identical; the only difference is in the technology node used in fabrication.

In order to interface the SRAM chips, we use a custom-designed board with a TSOP-54 socket for holding SRAM chips [see Fig. 2(a)]. The socket is connected to an Arduino Due platform that acts as a controller responsible for reading SRAM power-up states. The Arduino Due is further connected

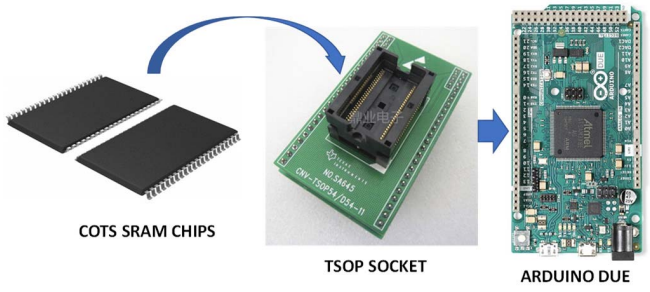

Fig. 2. Experimental setup.

via its native universal serial bus (USB) port to a workstation where data are further processed and analyzed.

The irradiation experiments are performed at the Sandia National Laboratories Gamma Irradiation Facility using a Co-60 source with a dose rate of 18.6 rad(Si)/s. Gamma irradiation was performed on the packaged TSOP (thin small outline package) devices with all the pins of the chip grounded. The direction of gamma rays during irradiation is perpendicular to the top surface of the chip.

The step-by-step experimental flow is given as follows. Before irradiating the chips, we precharacterize each chip to evaluate its baseline power-up states. We perform five consecutive power ON/OFF cycles and read each power-up state of the SRAM array. We read word-by-word the first 64k words of the SRAM array, resulting in a total of 1 Mbit (64k $\times$ 16) of the power-up state per one power-up cycle. We generate the GoldPUF by taking a majority vote from five power-up states of a fresh chip. We then expose the memory chips to gamma rays up to a certain dose level. We retrieve the power-up state of the irradiated chip within 45–60 min after irradiation. The PUF generated from the irradiated chip is called authentication PUF. We generate five authentication PUFs and they are individually compared with the GoldPUF to compute HD and the average is reported.

IV. Results and Discussion

A. Effects of Total Dose on SRAM-PUF

Fig. 3(a) and (b) shows the HD of SRAM-PUFs as a function of the total irradiation dose for IDT and Cypress chips, respectively. Fig. 3(a) and (b) shows the intradie HD values between the GoldPUF and the corresponding authentication PUFs, respectively. We find that intradie HD before irradiation is relatively small ($\sim$2%). Error-correction codes (ECCs) can be used to correct bit errors in the PUFs. However, we observe a monotonic increase in HD with an increase in the total dose with both vendors. We find that the HD exceeds 15% after TID = 100 krad(Si) for the IDT chip, and 9% for the Cypress chip. While the errors can be corrected using powerful ECCs, most ECC implementations require significant on-chip area and time overheads that scale up with the number of errors that need to be corrected. Furthermore, the ECCs require the generation and storage of helper data that are used later for error correction. The overhead due to helper data scales up exponentially with the bit error rate (BER). For example, correcting 6% of errors requires $\sim$3.68 bits per one valid PUF bit, whereas correcting 15% of errors requires $\sim$23.43 bits per one valid PUF bit [20]. In addition, helper data, typically stored in nonvolatile memory, can be a source of information leakage if not handled properly.

TABLE II
Summary of TID Effects on SRAM-PUFs

	IDT		CYPRESS	
TID (krad(Si)	HD(%)	HW(%)	HD(%)	HW(%)
0	1.45	44.75	2.38	50
30	6.11	45.05	4.29	49
100	16.71	44.90	9.01	49
200	25.69	45.62	13.11	50

For the reasons discussed above, we conclude that the SRAM PUFs may not be an ideal choice for encryption-key generation purposes that require zero BER after they are exposed to a moderate amount of irradiation [TID = 100 krad(Si)]. If they are used in radiation-prone environments, their implementations should involve powerful ECCs and provisions to prevent information leakage through helper data. However, SRAM PUFs may still be usable for device authentication applications. Since the interdie HD remains close to 50% even after irradiation, there exists a significant gap between intradie and interdie HD values. Hence, depending on the rejection thresholds, the PUF may still be used for authentication purposes, similar to what Lawrence et al. [10] concluded.

Fig. 3(c) shows the chip-to-chip variation in the HD values after irradiation. Four identical standalone SRAM chips from IDT and Cypress were used in this study. We find minimal variation across different chips within the same family of chips. Relatively high HDs are observed in all SRAM chips after irradiation. The IDT chips are seemingly more susceptible to power-up state degradation than the Cypress chips. This might be due to differences in the process technology between the two families of chips. Note that our goal in this article is not the comparison between two different SRAM chips, but to highlight the universality of SRAM PUF characteristics under irradiation. Table II summarizes the characterization results by reporting HD and HW as a function of TID. We do not find any significant changes in the HW due to irradiation. We tested the chips up to 100 krad(Si) as parts in a geosynchronous Earth orbit (GEO) satellite receive around 100 krad(Si) during their average lifetime of ten years [21]. Note that we have verified the basic functionality of the chip after irradiation by performing write and read operations with random data. We find that all the SRAM chips remain fully functional after irradiation.

B. Total Dose Induced Unstable Power-Up Bits

We perform a bit-by-bit analysis of total dose effects on SRAM PUF degradation. We classify SRAM-PUF bits into three categories as follows: strongly skewed to zero, strongly

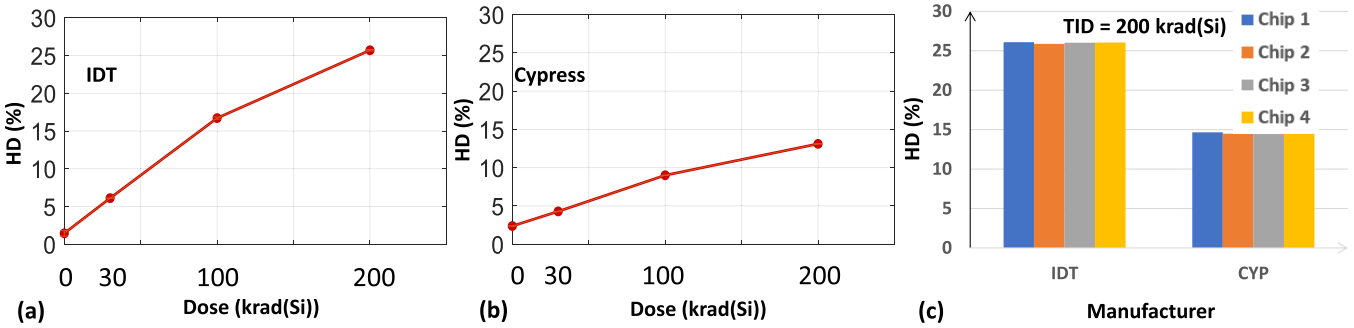

Fig. 3. HD of SRAM-PUF as a function of total dose for COTS memory chips from (a) IDT and (b) Cypress. (c) Chip-to-chip variation results of HD after irradiation [TID = 200 krad(Si)]. Four identical SRAM chips from IDT and Cypress are used.

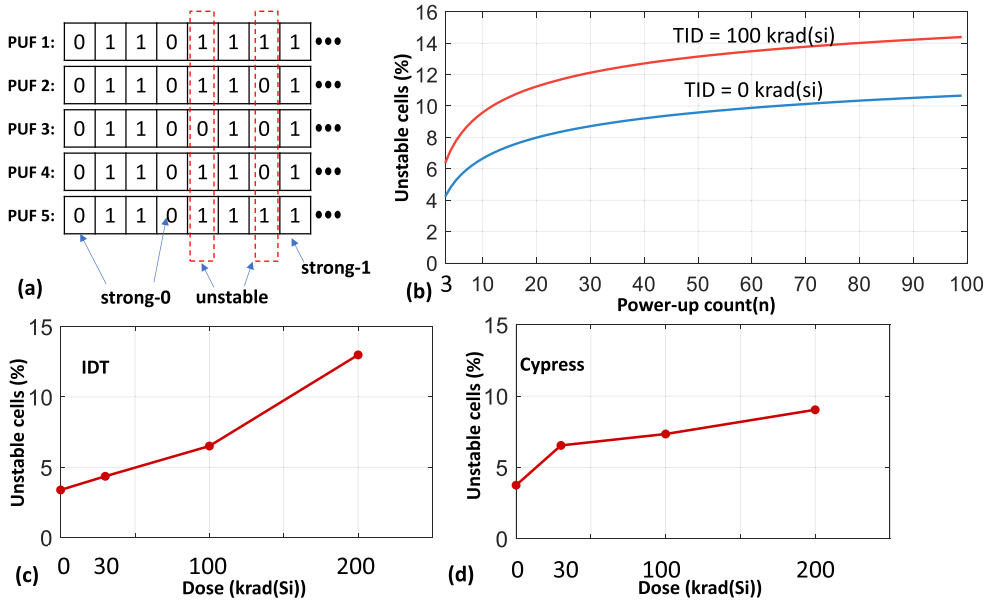

Fig. 4. (a) Classification of SRAM-PUF bits as strong-0, strong-1, and unstable bits. (b) Percentage of unstable PUF bits as a function of power-up read counts (n). Unstable PUF bits as a function of the total dose for COTS memory chips from (c) IDT and (d) Cypress.

skewed to one, and unstable bits [1]. Fig. 4(a) shows our classification method. We define unstable PUF bits as those bits that flip their state during consecutive PUF generation, whereas strongly skewed bits are those that retain their state (zero or one) during successive PUF generation. The strongly skewed bits are stable PUF bits because random electric noise is not sufficient to change their states on consecutive power-up read operations.

Fig. 4(b) shows the percentage of unstable bits in 1-Mb SRAM PUF as a function of the number of power-up read operations (n). The number of unstable PUF bits is increasing with an increase in the number of power-ups. However, only a tiny fraction of additional unstable bits is identified after a certain number of power-up operations ($n > 50$). Ideally, a larger number of power-up reads are necessary for accurately estimating the percentage of unstable PUF bits. Unfortunately, we have used only $n = 5$ power-up reads to estimate the number of unstable bits to minimize measurement time during irradiation experiments. Thus, the percentage of unstable bits we report here underestimates the actual percentage of unstable PUF bits. Nevertheless, our main focus here is the exploration of a relative trend in the percentage of unstable bits as a function of total dose and we believe that $n = 5$ is sufficient to capture this trend.

Fig. 4(c) and (d) shows the percentage of unstable PUF bits as a function of the total dose for IDT and Cypress chips, respectively. Chips from both vendors show a similar looking trend where the percentage of unstable bits gradually increases with an increase in the total irradiation dose. It is well known that ionizing radiation introduces defect states in the MOS structures, which increases the low-frequency or $1/f$ noise in semiconductor devices [22], [23], [24]. We believe that the effects of radiation-induced defects in the MOS structure are reflected in terms of an increased count of unstable PUF bits, which in turn increases the HD of the SRAM PUF after irradiation.

C. Root Cause Analysis

We first provide a conceptual framework to understand the power-up transients of SRAM cells and then provide an

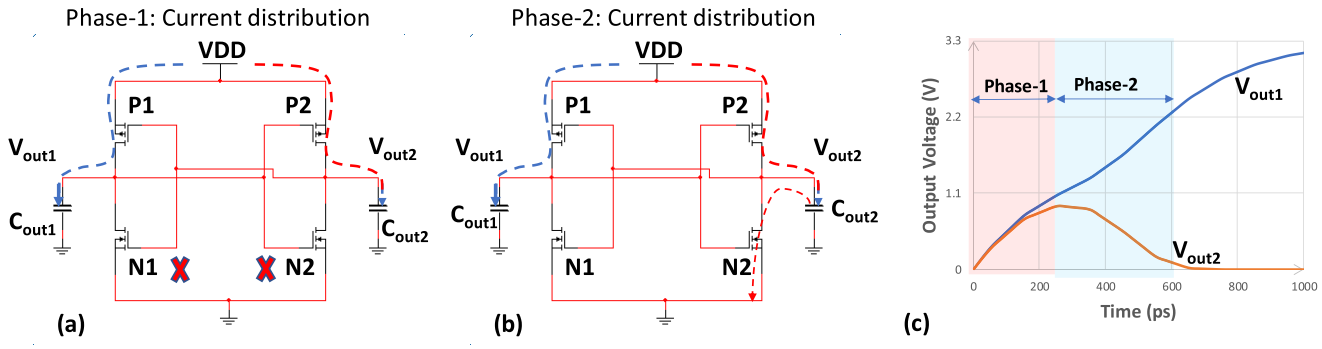

Fig. 5. (a) Schematic of an SRAM cell used for simulation. The current distribution corresponds to phase-1 of the power-up transient. (b) Current distribution during phase-2 of the power-up transient. (c) Transient power-up characteristics of the output nodes.

explanation of the effects of irradiation on it. During the first few picoseconds after power-up (phase-1 of transient behavior), the behavior of the cross-coupled CMOS inverters is critical in determining its steady-state power-up state. Fig. 5(a) shows the schematic of the SRAM cell with the ON/OFF conditions of the individual transistors during the initial phase (phase-1) of power-up. Note that all the nMOS transistors (two access transistors and two pull-down nMOS transistors) are turned off during the initial phase of power-up. The access transistors connected to the output nodes remain OFF throughout the power-up phase as word lines remain grounded. The nMOS transistors of the cross-coupled inverters remain OFF during the first few nanoseconds after power-up as output node voltages (V_{out1} and V_{out2}) take some time to reach a value greater than the threshold voltages of nMOS transistors. We use two equivalent output capacitors on the output nodes of the cross-coupled inverters to capture the total output capacitance, including the access transistors. Note that both the pMOS transistors are turned on initially and transient current flows through them charging the output nodes (V_{out1} and V_{out2}). If there is a mismatch in the pMOS transistors' current, one output node may charge faster than the other, which may eventually decide the steady power-up state of the cell. For example, if the current through the P1 transistor is higher than the current through P2, the output voltage V_{out1} will rise faster than V_{out2}. It will turn on the nMOS transistor N2 earlier than N1 causing faster discharge of the capacitor C_2. We illustrate the discharging event in Fig. 5(b) as the second phase of the power-up transient. Eventually, V_{out1} reaches V_{DD} and V_{out2} reaches ground potential, as shown in Fig. 5(c). We use the HSPICE simulation to generate Fig. 5(c). Simulation parameters are summarized in Table III. Note that we have chosen all device parameters for both inverters to be identical, except for the threshold voltage (V_t) magnitude, which is chosen slightly lower for the P1 transistor than P2. Such a small mismatch in V_t values eventually decides the power-up state of a cell, as shown in Fig. 5(c). There can be several process variables that can cause the mismatch between the transient current, deciding the ultimate power-up state. Thus, Fig. 5(c) needs to be treated as an illustrative example to understand the transient behaviors of the SRAM cell during the power-up phase.

TABLE III
HSPICE SIMULATION PARAMETERS

Parameters	Value
Sizing of pull-up PMOS	W=200 nm, L=100 nm
Sizing of pull-down NMOS	W=600 nm, L=100 nm
Output capacitor	10 pF

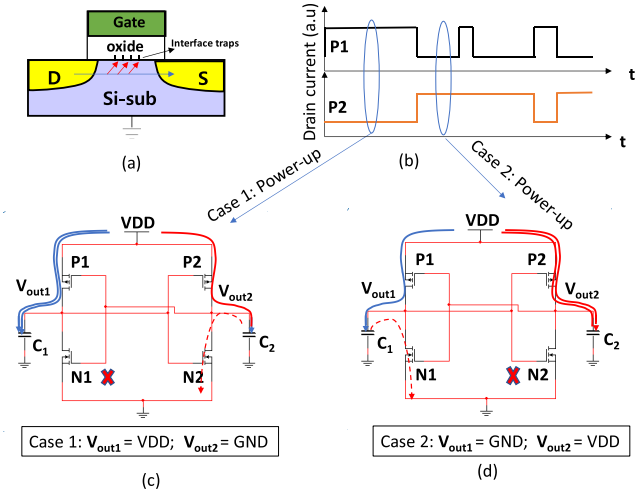

Fig. 6. (a) Schematic of a transistor with interface defect. (b) Current fluctuation caused by low-frequency noise. (c) and (d) Current transient leading to two different power-up states corresponding to different drain current values during power-up.

Ionizing radiation significantly changes the power-up transient current of the SRAM cell due to the following reasons: 1) irradiation introduces defects in the MOS structure causing random current fluctuations and 2) irradiation causes charge trapping in the oxide layer altering the threshold voltage of transistor [22], [23], [24]. Based on these two effects, we illustrate the PUF degradation with the total dose in the following paragraphs.

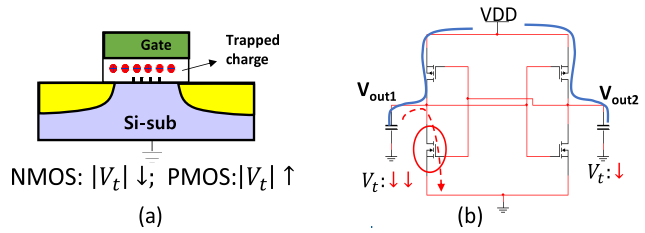

Fig. 7. Radiation-induced charge trapping effect in (a) oxide and (b) corresponding current transients during the power-up phase.

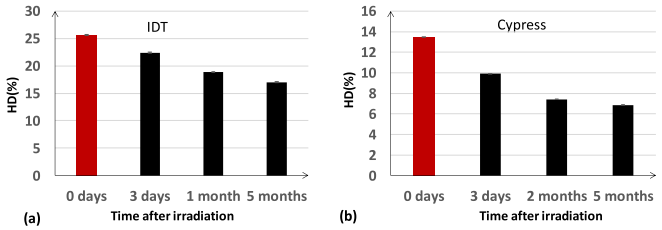

Fig. 8. Relaxation effects for (a) IDT (b) Cypress chip.

1) Effect of Irradiation-Induced Defects: Fig. 6 shows the effects of interface defects during the power-up transient. Defects near the oxide–Si interface in the MOS structure [see Fig. 6(a)] cause fluctuation in current conduction characterized by low-frequency noise [22], [23], [24]. Fig. 6(b) shows a sketch for random current fluctuation through the pMOS transistors affected by noise. If the current fluctuation is significant during the power-up transient (phase-1), unstable power-up states will be observed. For example, Fig. 6(c) and (d) shows two cases where current fluctuation during phase-1 of the power-up transient forces a cell to either of the two power-up states. Since noise amplitude increases after irradiation, such unstable behavior is expected to increase on the irradiated chip as confirmed by our experimental evaluation in Fig. 4.

2) Effect of Charge Trapping in Oxide: Ionizing radiation causes charge trapping in the oxide layer (mainly holes) causing an increase in threshold voltage magnitude for pMOS and a decrease in threshold voltage magnitude for nMOS [see Fig 7(a)]. If the radiation-induced V_t shift of one of the pMOS transistors of a single memory cell is considerably higher than the other, then the output node corresponding to that pMOS transistor will have a lower charging current, forcing that node to settle at the ground state irrespective of its power-up state before irradiation. Similarly, if one of the nMOS transistor's V_t gets significantly lower compared to the other nMOS, then the output node corresponding to the low-V_t nMOS will end up at the ground state [see Fig. 7(b)]. In other words, a PUF bit that remains in the "1" state during several subsequent power-on states (strong-1) may get converted to a PUF bit that remains in the "0" state during several subsequent power-on states (strong-0) after irradiation and vice versa, due to significant and unequal shifts of threshold voltages of the individual transistors.

D. Room Temperature Annealing Effects on Irradiated Chips

In this section, we analyze the room temperature annealing effects on irradiated SRAM chips. The irradiated chips were kept at room temperature with all pins floating. We measure the power-up state and compute the PUF HD following the same procedure described by (1). Fig. 8(a) and (b) shows the results for the IDT and Cypress chip, respectively. The chips are allowed to anneal at room temperature for over five months. We observe a consistent trend of decreasing HD over time from both vendors. A significant decrease in HD seems to happen in the first few days after irradiation. However, even after five months of room temperature annealing period, more than 60% of the erroneous PUF-bits remained in the erroneous state. We know that trapped holes in the oxide layers anneal through thermal or tunnel annealing [25] and also neutralize through hydrogen diffusion [26]. This possibly causes the transistor's threshold voltage to partially regress to its initial state. Lawrence et al. [10] observed a small increase in HD in a 24-h annealing period. In general, the post-irradiation annealing response of SRAM cells depends on several factors, including bias conditions during irradiation and annealing, anneal duration, total dose during irradiation, and device layout [27].

V. Conclusion

In summary, we conclude that the power-up states of SRAM cells in commercial SRAM chips are significantly altered by ionizing radiation. The intradie HD of PUFs drastically increases with an increase in the total irradiation dose exceeding more than 15% after 100 krad(Si) for a family of chips. Thus, SRAM PUFs are not suitable for encryption key generation purposes after a moderate amount of irradiation [TID = 100 krad(Si)] unless they are accompanied by strong ECCs. However, depending on the selection of rejection thresholds, the SRAM PUF may still be used for authentication purposes. We observe small annealing effects over time, but the HD remains high even five months after irradiation.

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