Towards Improving Ionizing Radiation Tolerance of 3-D NAND Flash Memory

Biswajit Ray
Electrical and Computer Engineering
The University of Alabama in Huntsville
Huntsville, AL, USA
biswajit.025@gmail.com

Matchima Buddhanoy
Electrical and Computer Engineering
The University of Alabama in Huntsville
Huntsville, AL, USA
mb0194@uah.edu

Mondol Anik Kumar
Electrical and Computer Engineering
The University of Alabama in Huntsville
Huntsville, AL, USA
mk0144@uah.edu

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***Abstract*—In this paper we present characterization results of total ionizing dose (TID) effects on commercial 3-D NAND memory. We show the TID induced threshold voltage shift and bit error rate of the memory array. Based on the characterization results we present four system-level techniques that can mitigate TID effects of the commercial 3-D NAND memory.**

Keywords—Total ionizing dose, 3-D NAND flash, reliability

I. Introduction

Total ionizing dose effects on 3-D NAND flash memory technology is a topic of great interest for space and defense applications. Even though NAND flash memory is the work-horse of the storage industry for high density, non-volatile data storage applications, it has several reliability concerns under ionizing radiation environment. Ionizing radiation lowers the threshold voltage of programmed memory cells causing bit-flip events and data corruption [1]–[3]. In addition, radiation effects introduce defect states in the oxide layers of the memory cells which degrades cell reliability such as endurance and data-retention [4]–[6]. Thus, it is important to implement radiation effects mitigation strategies before deploying flash storage in the radiation prone environments.

Even though TID effects on 2-D NAND flash technology is a well-researched topic, only a limited number of studies on the irradiation effects on 3-D NAND are available in the published literature [1]–[3]. In this paper, we provide experimental characterization results of TID effects on the state-of-the-art 3-D NAND flash memory. We include both charge trap and floating gate based commercial-off-the-shelf (COTS) 3-D NAND memory chips in our study. Based on the characterization results we propose a number of system-level techniques that can be used to enhance TID tolerance of commercial 3-D NAND memory.

II. Background

The schematic of the 3-D flash memory array is shown in Fig. 1(a). The green layers are the word lines (WLs) of the memory array while the purple pillars are the poly-silicon channel. The blue bottom layer is the silicon substrate, and the red lines at the top are the bit lines (BLs). The yellow bars on the substrate represent the select gate (SG) transistors. Similar SG transistors are also present at the top near the bit lines. Fig. 1(b) shows the circuit diagram of a NAND flash memory structure. A 3-D NAND flash memory chip typically contains thousands of flash blocks while each flash block consists of a fixed number of logical pages. Each logical page contains multiple flash cells. A 3-D NAND flash memory cell, as shown in Fig. 1(c), is essentially a gate-all-around (GAA) metal-oxide-semiconductor field-effect transistor (MOSFET) with a floating gate (FG) or charge-trap (CT) layer. Traditional flash memory cells store one bit of information and are known as SLC (Single-Level Cell). In SLC storage, a flash cell is in the programmed state (logic 0) when electrons are stored on the FG/CT layer, whereas it is in the erase state (logic 1) when there are no electrons on the FG/CT layer. However, modern flash memories store 2 bits (MLC – Multi-Level Cell), 3 bits (Triple-Level Cell), and 4 bits (QLC – Quad-Level Cell) in one cell.

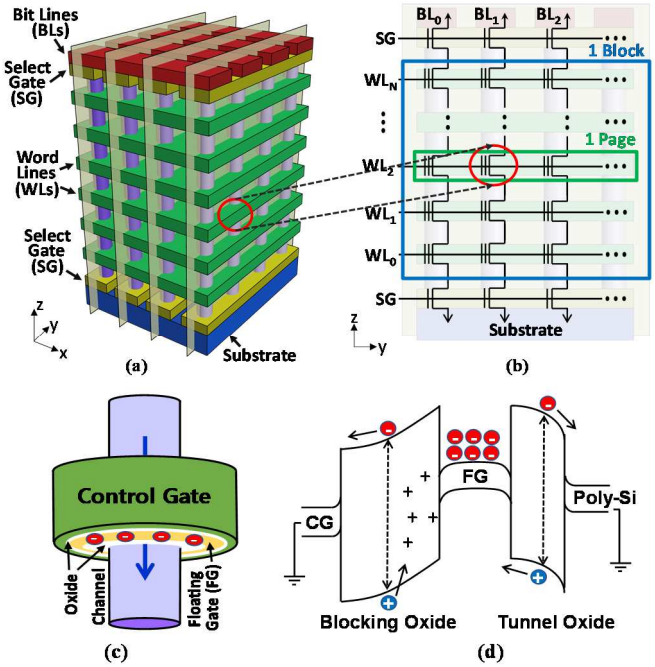

Fig. 1. (a) Schematic of a 3-D NAND flash memory block and (b) the corresponding circuit diagram. (c) Structure of a single flash memory cell with GAA geometry. (d) Energy band diagram of a programmed flash cell during radiation exposure with all pins grounded.

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Fig. 1(d) shows the energy band diagram of a programmed flash memory cell with all its terminals are grounded. Ionizing radiation creates electron-hole pairs in the insulating oxide layers. Radiation-induced electrons that escape recombination are swept off the oxide layers through the substrate or control-gate due to electric field of the oxide layers. Holes are usually trapped in the oxide layer or get recombined with stored electrons, eventually creating a net positive charge yield. As a result, threshold voltage of the programmed memory cells is lowered leading to 0→1-bit flips. In addition, ionizing radiation permanently damages the oxide layers by creating defect or trap states which degrades long-term data retention characteristics of the memory bits [6].

III. Radiation Effects Characterization Results

In this section, we discuss the experimental set-up and irradiation conditions. We also present the radiation effects characterization results of 3-D NAND flash memories.

A. Experimental set-up and irradiation conditions

The experimental evaluation is performed on multiple COTS 3-D NAND flash memory chips with FG/CT storage layers. To interface the raw NAND chip with the computer, we use a custom-designed hardware board, as shown in Fig. 2. We follow the command sets defined by the Open NAND Flash Interface (ONFI) to perform basic memory operations such as read, write, erase and read-retry [7]. The hardware setup allows us to access the raw memory bits without any error correction.

To evaluate the ionizing radiation effects on 3-D NAND flash memories, we expose the chips to radiation at the Ohio State University's Nuclear Reactor Facility using a Co-60 source at a dose rate of 18.6 rad(Si)/s. Gamma irradiation is performed on packaged devices with all pins grounded. The direction of gamma rays during irradiation was perpendicular to the top surface of the chip. Note that we only expose raw NAND flash chips to Gamma irradiation while the hardware setup does not get exposed to irradiation.

B. Radiation effects on V_t distribution

Fig. 3 shows V_t distributions for the highest programmed state (L_7) in 3-D TLC FG NAND flash memory at different TID values [2]. The symbols represent the measured data while the solid lines represent the fitted Gaussian distribution. The distribution in black color represents pre-irradiation data obtained just after program operation. We find that the mean V_t value is lowered and the standard deviation of V_t distribution is increased with TID [2]. Similar behavior is observed in all remaining programmed states ($L_1 - L_6$) of the flash memory page. Fig. 3(b) summarises the V_t- shift (ΔV_t) values for each programmed state of the TLC memory. We find that higher the V_t state before irradiation, higher its mean ΔV_t magnitude is. This behavior is expected due to more charge yield in the oxide layers of higher V_t cells after irradiation caused by stronger electric-field magnitude.

C. Layer-dependent bit error rate

The V_t downshift causes bit error in the logical memory pages [3]. Fig. 4 shows the bit error rate (BER) of flash memory pages across different vertical layers before irradiation (blue) and after 10 krad(Si) irradiation (red). The BER values in all

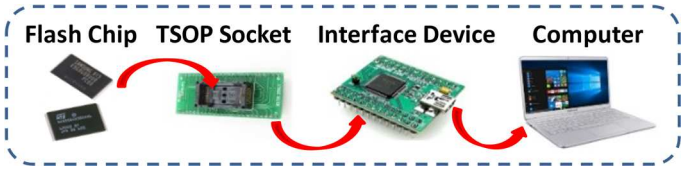

Fig. 2. Experimental set-up.

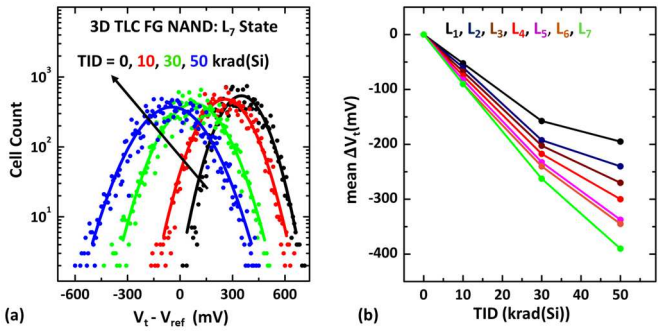

Fig. 3. (a) V_t distributions for the highest programmed state (L_7) in 3-D TLC FG NAND flash memory measured for different TID values. (b) Mean V_t shift for each programmed state is plotted as a function of TID values.

layers is very low before irradiation. However, after irradiation, the BER rises significantly in all layers. Average BER value from all the memory pages in a given 3-D layer of a memory block is plotted in Fig. 4. Default read reference method is used for reading the memory pages. For the charge trap memory we found that the bottom layers are more affected after irradiation. This might be due to the narrower diameter of the memory cells at the bottom of the 3-D stack due to the inefficient reactive ion eatching process typically used during fabrication of the 3-D NAND stacks. However, 64-layer FG 3-D NAND memory shows a different layer dependent BER pattern. So, we conclude that there is no fixed pattern for the layer-dependent BER response for all the 3-D NAND technology. However, for a given process we find that the layer dependent BER pattern remains the same [3].

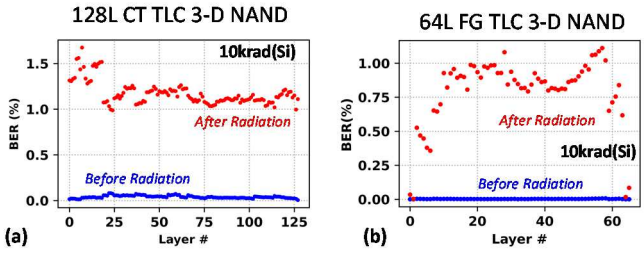

Fig. 4. Layer dependent BER after irradiation with TID = 10 krad(Si) for two different 3-D NAND memory chips with (a) 128-layer CT and (b) 64-layer FG technology. Average BER value is plotted for all the pages in a given layer.

IV. Approaches for Radiation Tolerance

In this section, we present four different approaches to enhance radiation tolerance of 3-D NAND flash memories.

A. *Layer-dependent error mitigation*

The layer dependence of the radiation-induced BER can be utilized by the memory controller to mitigate data corruption [3]. For example, error-correcting codes (ECCs) are typically used by the standard memory controller to detect and correct the errors present in the stored data. Since the pages located in the edge layers of the 3-D stack are more vulnerable to ionizing radiation damage, it may be necessary for the controller to implement stronger ECC (or more ECC bits) for data stored in these pages. Another important technique for ensuring data integrity is called data refresh, where memory controller periodically performs error correction of stored data and re-writes them on a new location. The refresh frequency of memory pages can be made layer dependent based on pre-characterization results. Additionally, a flash memory based on-chip dosimeter, originally proposed by Kumari et. al [8], can be utilized by the memory controller in order to determine the absorbed dose to trigger refresh operation.

B. *Defect engineering to achieve radiation-tolerance*

Defect states in the tunnel oxide of a flash memory cell play a significant role to determine its electrostatics. For example, if a flash cell has pre-existing defects in tunnel-oxide and Poly-Si interface, a fraction of the electrons gets trapped at the interface states during program operation, requiring fewer electrons on FG as illustrated in Fig. 5(a) and (b). The presence of this interface trapped electrons will create a rather localized electric field in the interface causing sharp band bending (Fig 5(b)). Consequently, the blocking oxide field will be weaker for an interface-trap dominated cell. Weaker field will lead to recombination of radiation induced electron-hole pairs reducing the net positive charge yield during irradiation. Since blocking oxide is thicker than the tunnel oxide, lower charge yield in the blocking oxide will reduce the TID effects significantly. Fig. 5(c) shows measured V_t -loss data as a function of TID from a commercial 3-D NAND memory chip. Interestingly, we find that a group of memory cells (blue) are not much affected by irradiation in comparison with other memory cells. We believe that the blue cells are interface-trap dominant cells. However, interface traps will reduce the long-term data retention of memory cells (see Fig. 5(d)) and hence defect engineering will offer a trade-off between TID tolerance and long-term data retention.

C. *Watermark storage*

In order to ensure long-term data integrity of flash storage under radiation environment, we proposed a novel non-charge based data storage technique called *Watermark* [9]. Watermark stores data in the form of analog property of memory cells, such as intrinsic cell V_t, which is altered through repeated program-erase (PE) cycles. PE cycles introduces defect states in the oxide layer of selected memory cells by soft-breakdown. These defect states change analog cell properties permanently; and hence, the proposed technique resembles as one-time-programmable memories.

The Watermark imprinting technique is illustrated in Fig. 6(a) using the binary representation of the year 2021. The imprinting process involves repeated erasing and programming of Watermark data until there are sufficient differences in physical properties between "good" and "bad" bits shown in Fig. 6(a). The retrieval of Watermark will be performed by partial-erase operation. As illustrated in Fig. 6(b), if a partial-erase operation is performed on the imprinted page written with traditional charge-based data (all-zero), the "good" bits will flip to logic-1 whereas the "bad" bits will remain in logic-0. In this way, the imprinted information can be retrieved using standard system commands. Fig. 6(c) compares TID effects on Watermark and traditional charge-based SLC storage. Clearly, TID-induced degradation rate of Watermark storage is significantly lower than the SLC storage [9].

D. *Electrostatic shielding from ionizing radiation*

Ionizing radiation not only lowers the cell V_t but also causes permanent damage to the oxide layers by creating trap states [4]–[6]. Damaged oxide layers degrade data retention characteristic of memory cell [6] and make them vulnerable to noise effects [5]. To protect the oxide layers from ionizing radiation damage, especially when the flash cell is not holding any useful data, we suggest pre-programming the memory module before deploying it to the radiation environment. This technique is called *"Electrostatic Shielding"* since it is found that the stored charge at the FG/CT layer shields the oxide-channel interface from radiation-induced permanent damage.

To evaluate the effectiveness of this technique, we perform the data retention test on two groups of memory blocks from an irradiated chip. The first group of memory blocks was in the programmed state whereas the second group of blocks was in the erased state during irradiation. After irradiation, we freshly

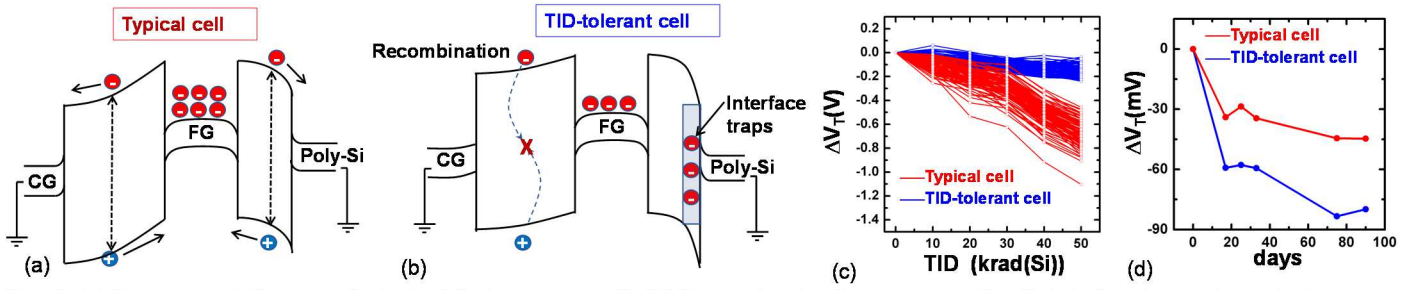

Fig. 5. (a) Energy band diagram of a typical flash memory cell. (b) Energy bands of a memory cell with interface traps where electrons are trapped during program operation. This type of cell is expected to be TID-tolerant due to weaker field in the blocking oxide. (c) Measured cell by cell V_t-loss data with TID from a commercial memory chip. (d) Average V_t-loss at room temperature of typical and TID-tolerant cells after irradiation.

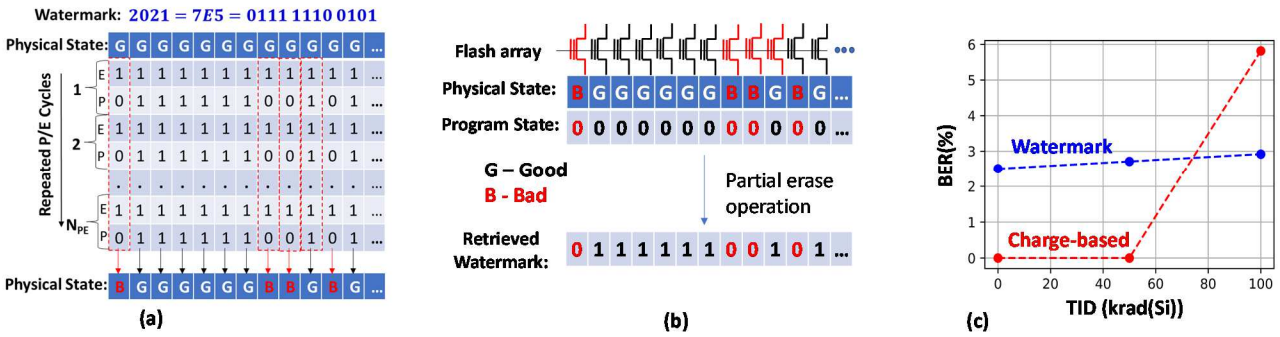

Fig. 6. (a) Watermark imprinting technique. (b) Watermark retrieval technique. (c) Comparison of BER of Watermark storage and charge based SLC storage under irradiation.

write new data on both groups of memory blocks and compare the retention error in Fig. 7(a)-(b). We find that memory blocks that were in the programmed state during irradiation (green line) perform better in terms of data retention properties compared to the blocks that were in the erased state during irradiation (red line). We find that electrostatic shielding concept holds in both FG and CT 3-D NAND flash memory.

We explain the physics behind our technique by using the energy band diagram illustrated in Fig. 7(c)-(d). Note that Fig. 7(c)-(d) represents the simplified energy band diagram of an erased and a programmed flash cell with all terminals grounded. Due to the opposite field direction in the tunnel oxide of a programmed and erased cell, the trapped hole and defect location in the tunnel oxide are different as shown in the figure. In general, trap states located near the oxide-channel interface are more harmful compared to the trap states close to FG/CT interface. As a result, the erased memory cells suffer more TID-induced degradation compared to programmed memory cells.

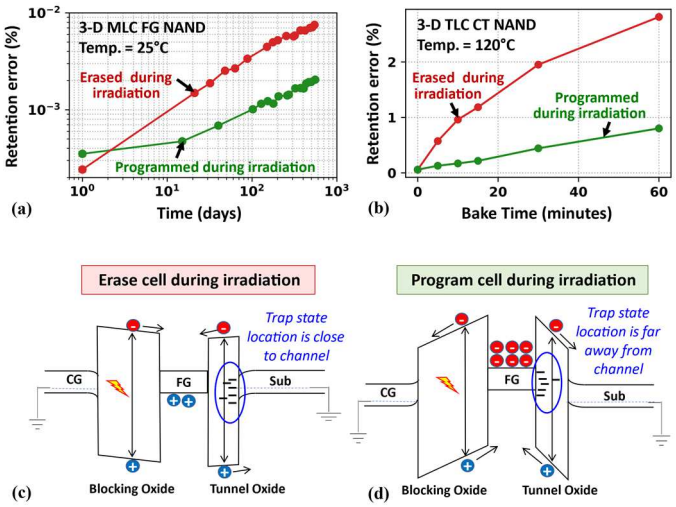

Fig. 7. Plot of retention error vs. time for (a) 3-D MLC FG NAND and (b) 3-D TLC CT NAND. Energy band diagram of an (c) erased cell and (d) programmed during irradiation.

V. Conclusion

In summary, we have presented characterization results of ionizing radiation effects on commercial 3-D NAND flash memory. In addition, we have discussed four different techniques that can be useful to increase radiation tolerance of commercial NAND flash memory technology in radiation-prone environment. In this work, we have focused our analysis on memory cell reliability, even though failure of peripheral circuits, such as decoder and charge-pumps, is an important concern for high dose of irradiation (TID > 50 krad(Si)).

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