Approximated Fractional-Order Capacitor "Seed" Impedance Characterization to Support Fully-Controllable Immittance Converters

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***Abstract*—One recent method to approximate and physically implement fractional-order elements utilizes a fully-controllable immittance converter (FGIC). With this approach, external components are used with the FGIC to implement a target floating immittance value. This immittance can be fractional-order if at least one of the external components is a fractional-order element. Here, a fractional-order capacitor is approximated for use as the fractional-order element using an RC-network; designed specifically to meet the usable bandwidth (10 kHz to 1 MHz) of an FGIC44 (an integrated circuit realization of a floating immittance converter using operational-transconductance amplifiers).**

I. Introduction

The field of fractional-order circuits refers to electrical circuits that utilize concepts from fractional calculus in their design and realization [1]. Fractional calculus is the branch of mathematics concerning the differentiation and integration of functions to non-integer order [2]. As an example, the Grunwald-Letnikov definition of a fractional-order derivative, with non-integer order α, is given by [3]:

$$ {}_aD^{\alpha}f(x) = \lim_{h\to 0}\frac{1}{h^{\alpha}}\sum_{m=0}^{\left[\frac{x-a}{h}\right]}(-1)^m\frac{\Gamma(\alpha+1)}{m!\Gamma(\alpha-m+1)}f(x-mh) \tag{1}$$

where $\Gamma(\cdot)$ is the gamma function and $n-1 \leq \alpha \leq n$. The integration of these concepts into circuits and systems has yielded fractional-order impedances [4], fractional-order control systems [5], [6], and fractional-order oscillators [7] to name a few recent advances.

Focusing on fractional-order circuits and system in the analog domain, the ideal realization of this class of circuits requires a fractional-order element (FOE). This terminology refers to an electrical component with voltage/current relationship defined by a fractional-order differential equation. This generalization to the fractional-order domain realizes voltage/current characteristics between the traditional resistors, indicators, and capacitors. As an example, a fractional-order capacitor has the voltage/current relationship given by:

$$ i = C_{\alpha}\frac{\mathrm{d}^{\alpha}v}{\mathrm{d}t^{\alpha}} \tag{2}$$

where $0 \leq \alpha \leq 1$ is the fractional-order and C_{α} is the pseudo-capacitance with units F/sec$^{1-\alpha}$. When $\alpha = 1$ this component is a traditional (integer order) capacitor and when $\alpha = 0$ it is a resistor. Applying the Laplace transform (with zero initial conditions) to (2), the expression can be rearranged to yield the electrical impedance of the fractional-order capacitor (FOC)

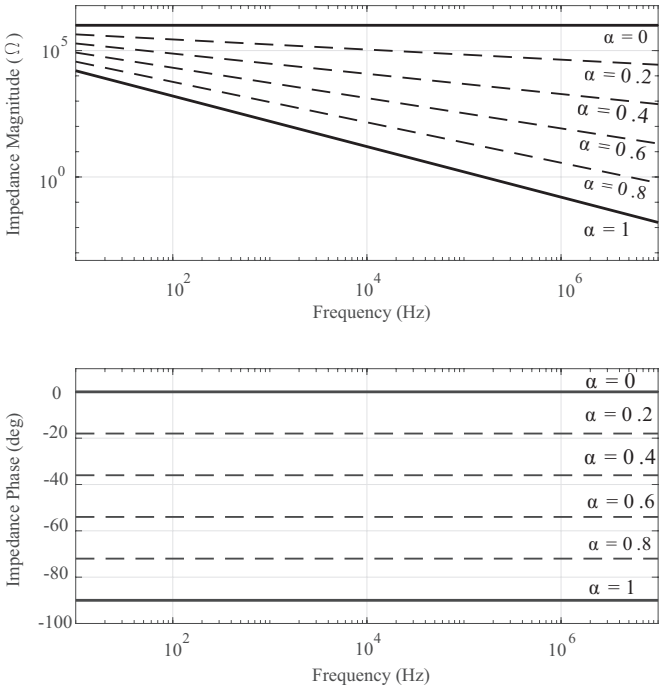

Fig. 1. Impedance (a) magnitude and (b) phase of ideal 1 μF/sec$^{1-\alpha}$ fractional-order capacitors with $\alpha = 0.2$ to 0.8 in steps of 0.2 from 10 Hz to 10 MHz.

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TABLE I
FGIC44 FRACTIONAL-ORDER ADMITTANCE USING ONE SEED FOE WITH $\alpha = 0.205$

α_1	α_2	α_3	α_4	α
1	0	1	1	-2
1	0	0.205	0	-1.205
0	0	1	0	-1
0	0.205	1	0	-0.795
0.205	0	0	0	-0.205
0	0	0	0	0
0	0.205	0	0	0.205
0	1	0.205	0	0.795
0	1	0	0	1
0	1	0	0.205	1.205
0	1	0	1	2

given by:

$$Z(s) = \frac{V(s)}{I(s)} = \frac{1}{C_\alpha s^\alpha} \tag{3}$$

where $s = \mathrm{j}\omega$. To illustrate the fractional-order properties of ideal FOEs, the impedance magnitude and phase from 1 Hz to 10 MHz for a 1 μF/sec$^{1-\alpha}$ component with $\alpha = 0.2$ to 0.8 in steps of 0.2 are shown in Fig. 1. To highlight the fractional-order steps, the ideal values of a resistor ($\alpha = 0$) and traditional capacitor ($\alpha = 1$) are provided for reference. Both the magnitude and phase of the FOE impedance are dependent on the order (α). In the context of the magnitude, the fractional-order impacts the slope as the magnitude decreases with increasing frequency. For phase, which is constant with frequency, the fractional-order affects the value such that $\varphi_\alpha = -90\alpha^\circ$. While fractional-order components (e.g. fractional-order capacitors and inductors) are not commercially available progress has been made regarding both their realization [8] and methods to approximate them using traditional (and commercially available) components [9].

One recent method to approximate and physically implement FOEs utilizes a fully-controllable immittance converter (FGIC) [10] with fractional-order "seeds" [11], [12]. With this approach, external components are used with the FGIC to implement a target floating immittance value. This immittance can be fractional-order if at least one of external components is a FOE and both the immittance and order can be tuned through the targeted use of other component values. For example, Koton *et al.* [11], [12] presented that the use of a single "seed" admittance with $\alpha = 0.2$ could approximate fractional-orders from -2 to 2 in steps of 0.2 [11]. This provides a method to realize a wide range of FOEs when only a limited number of "seeds" are available. To validate this approach, fractional-order seeds were approximated using both 5-th order [11] and 7-th order RC networks [12]. Generally, as the order of an approximation is increased the frequency band that it approximates and the error in that frequency band (compared to the ideal case) decreases. While the earlier 5-th order and 7-th order approximations validated the operation of the FGIC there has been limited efforts in evaluating what order of "seed" is necessary to realize a FOE across the operational bandwidth of the FGIC (which motivates this work).

In this work, an analysis of the FOE characteristics (bandwidth, peak error, RMS error) when 5-th, 7-th, and 8-th order approximations are utilized is outlined. From this analysis recommendations on the approximation order for FGIC designs will be presented with simulations and experimental results of the FOE characteristics provided to support.

II. FGIC44 OPERATION AND PERFORMANCE SUMMARY

The FGIC44 is an integrated circuit realization of a floating immittance converter using operational-transconductance amplifiers (OTAs) [10], [12]. The input admittance of this design is given by:

$$\left[\mathrm{Y_{IN}}\right] = \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \frac{\mathrm{Y_2 Y_4}}{\mathrm{Y_1 Y_3}} \frac{g_{m1} g_{m2} g_{m3} g_{m4}}{g_{m5} g_{m6} g_{m7}} \tag{4}$$

where $Y_{1,2,3,4}$ are the admittances of the external components and g_{m1-7} are the transconductances of the internal OTAs. This design realizes an admittance with fractional-order given by:

$$\alpha = \alpha_2 + \alpha_4 - \alpha_1 - \alpha_3 \tag{5}$$

where α_{1-4} are the orders of the externally connected admittances Y_{1-4}, respectively. Complete details of the design and characterization are provided by Koton *et al.* [11] and Dvorak *et al.* [10] for interested readers. The values given in Table I highlight how a range of overall fractional-orders (from -2 to 2) can be realized using only one "seed" element. From the experimental characterization by Dvorak *et al.* of the realized FGIC44 designs using the 0.18 μm TSMC CMOS technology process, the internal OTAs had magnitude and phase responses that were constant from 1 Hz to 1 MHz (magnitude) and 100 kHz (phase) [10]. Therefore, the FOE components used as "seeds" with the FGIC should also have bandwidths that match these ranges for magnitude and phase.

III. APPROXIMATION OF FRACTIONAL ORDER CAPACITOR

Approximating a fractional-order capacitor requires the design and realization of an electric network with magnitude and phase characteristics similar to the theoretical FOC impedance over a frequency band of interest. One approach designs a rational approximation for s^α that is used in (3), generating an integer-order function that can be implemented using traditional (i.e. integer order) electric network synthesis techniques. Towards this process, an n-th order approximation (where n is an integer) of s^α is given by:

$$s^\alpha \cong \omega_0^\alpha \cdot \frac{a_n s^n + a_{n-1}\omega_0 s^{n-1} + ... + a_1 \omega_0^{n-1} s + a_0 \omega_0^n}{b_n s^n + b_{n-1}\omega_0 s^{n-1} + ... + b_1 \omega_0^{n-1} s + b_0 \omega_0^n} \tag{6}$$

where a_0 to a_n are the numerator coefficients, b_0 to b_n are the denominator coefficients, and ω_0 is the center frequency of the approximation. The next steps are generating the appropriate capacitance value for the integer-order realization. A FOC and traditional capacitor do not share the same units but can be related to each other at a specific frequency (ω_0, in rad/s) given by:

$$C = \frac{C_a}{\omega_0^{1-\alpha}} \tag{7}$$

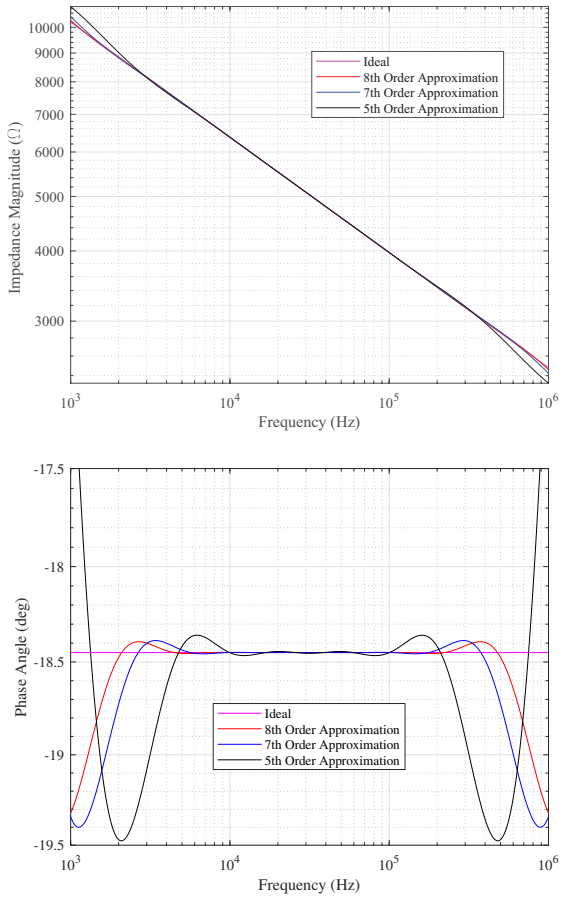

Fig. 2. Impedance (a) magnitude and (b) phase of 5-th, 7-th, and 8-th order approximations of $s^{0.205}$ compared to ideal case.

where C is the integer order capacitor (with units of F) and C_α is the pseudo-capacitance (with units F/sec$^{1-\alpha}$) [13]. This expression supports the design of a FOC approximation through the calculation of the equivalent integer-order capacitance to represent the target C at a particular frequency of interest.

To realize an approximated FOC with $C = 1$ nF and $\alpha = 0.205$ with a center frequency of 31.7 kHz (selected as a logarithmic midpont between 10 kHz and 1 MHz), the value of C_α using (7) is 16.3 μF/sec$^{1-\alpha}$. Substituting both (6) and (7) into (3), the approximated fractional order impedance (and its inverse, admittance) are given by:

$$Z(s) \approx \frac{1}{C\omega_0} \cdot \frac{b_n s^n + b_{n-1}\omega_0 s^{n-1} + ... + b_1\omega_0^{n-1}s + b_0\omega_0^n}{a_n s^n + a_{n-1}\omega_0 s^{n-1} + ... + a_1\omega_0^{n-1}s + a_0\omega_0^n} \tag{8}$$

$$Y(s) \approx C\omega_0 \cdot \frac{a_n s^n + a_{n-1}\omega_0 s^{n-1} + ... + a_1\omega_0^{n-1}s + a_0\omega_0^n}{b_n s^n + b_{n-1}\omega_0 s^{n-1} + ... + b_1\omega_0^{n-1}s + b_0\omega_0^n} \tag{9}$$

Note that the a and b coefficients in (6) are dependent on the value of α. Their value as a function of α can be generated using the general form for continued fraction expansion to $(1+x)^\alpha$, given by [14]:

$$(1+x)^\alpha = \frac{1}{1-}\frac{\alpha x}{1+}...\frac{(n+\alpha)x}{2+}\frac{(n-\alpha)x}{(2n+1)+}... \tag{10}$$

in which the substitution $x = s - 1$ is made. From this form, using the approach presented by Tsirimokou *et al.* [13], the a and b coefficient values for the 8-th order approximation of s^α are given in Table II.

A. Impedance Characteristics

As noted previously, FOE approximations can be improved by increasing their order, that is the number of elements in the realization. This improvement is observed as an increase of the approximated frequency band and/or decrease of approximation error.

Previously, 5-th and 7-th order approximations of s^α have been utilized in the approximation of a FOC when the FGIC44 has been utilized [10], [12]. To visualize the improvements increasing approximation order yields, the magnitude and phase of 5-th and 7-th order approximations of $C_\alpha = 16.3$ μF/sec$^{1-\alpha}$, $\alpha = 0.205$, and center frequency of 31.7 kHz are given in Fig. 2. For comparison, the ideal magnitude and phase ($\varphi_{0.205} = -18.45°$) are also provided. The impedance magnitude of the approximations in Fig. 2(a) show very good visual agreement with the ideal case over the shown frequency band (1 kHz to 1 MHz). From 2(a), it was discovered that the frequency ranges of the 5-th and 7-th orders with less than 1% deviation from the ideal is 2.39 kHz to 1 MHz and 1 kHz to 1 MHz, respectively. Focusing on the phase in Fig. 2(b), the 5-th order approximation has less than 1% error for a frequency range of 1.20 kHz to 1 MHz with an increase to 1.02 kHz to 1 MHz for the 7-th order approximation of the impedance phase angle.

To increase the approximated frequency band of the FOC for future use with an FGIC44 an 8-th order approximation is selected (increasing beyond the 5-th and 7-th previously utilized). The necessary polynomials for this approximation for a FOC with $C_\alpha = 16.3$ μF/sec$^{1-\alpha}$, $\alpha = 0.205$, and center frequency of 31.7 kHz were generated in MATLAB using (6), (10), and (8). The magnitude and phase characteristics of this approximation are also given in Fig. 2 to visualize the improvements.

While the bandwidths of the previous approximations highlight the increased frequency range that increasing order yielded, this metric does not reflect the overall change in accuracy across the entire frequency band. For this comparison, the root mean square (RMS) error was calculated for both magnitude and phase for each approximation (when $\alpha = 0.2$, 0.5, and 0.8) over the bandwidth in which its error was $< 1\%$. These values and are given in Table III). This RMS value was calculated by:

$$x_{\text{RMS}} = \sqrt{\frac{1}{N}\sum_{n=1}^{N}|x_n|^2} \tag{11}$$

TABLE II
8-TH ORDER APPROXIMATION COEFFICIENTS AS A FUNCTION OF FRACTIONAL ORDER (α)

Coefficient	Coefficient Polynomial
$a_8 = b_0$	α^8 + 36α^7 + 546α^6 + 4536α^5 + 22449α_4 + 67284α_3 + 118124α^2 + 109584α + 40320
$a_7 = b_1$	ω_0(-8α^8 - 216α^7 - 1848α^6 + 504α^5 + 110208α^4 + 788256α^3 + 2572928α^2 + 4110336α + 2580480)
$a_6 = b_2$	ω_0^2(28α^8 + 504α^7 + 168α^6 - 47376α^5 - 278628α^4 + 498456α^3 + 9310112α^2 + 30030336α + 31610880)
$a_5 = b_3$	ω_0^3(-56α^8 - 504α^7 + 7224α^6 + 75096α^5 - 236544α^4 - 3630816α^3 - 1746304α^2 + 56899584α + 126443520)
$a_4 = b_4$	ω_0^4(70α^8 - 12180α^6 + 765030α^4 - 20509720α^2 + 197568000)
$a_3 = b_5$	ω_0^5(-56α^8 + 504α^7 + 7224α^6 - 75096α^5 - 236544α^4 + 3630816α^3 - 1746304α^2 - 56899584α + 126443520)
$a_2 = b_6$	ω_0^6(28α^8 - 504α^7 + 168α^6 + 47376α^5 - 278628α^4 - 498456α^3 + 9310112α^2 - 30030336α + 31610880)
$a_1 = b_7$	ω_0^7(-8α^8 + 216α^7 - 1848α^6 - 504α^5 + 110208α^4 - 788256α^3 + 2572928α^2 - 4110336α + 2580480)
$a_0 = b_8$	ω_0^8(α^8 - 36α^7 + 546α^6 - 4536α^5 + 22449α^4 - 67284α^3 + 118124α^2 - 109584α+ 40320)

TABLE III
ROOT MEAN SQUARE ERROR FOR 5-TH, 7-TH, AND 8-TH ORDER APPROXIMATIONS OF s^α

α	5-th Order Phase	5-th Order Impedance	7-th Order Phase	7-th Order Impedance	8-th Order Phase	8-th Order Impedance
0.2	2.78	2.02	1.85	0.44	1.23	0.16
0.5	1.91	3.72	1.35	0.73	0.87	0.28
0.8	0.81	2.43	0.56	0.42	0.34	0.18

where N is the total datapoints in the bandwidth of comparison and x_n is the difference between the ideal magnitude or phase and the approximation. For the purpose of results summarized in Table III, the assumed bandwidth was 10 kHz to 1 MHz and $N = 1001$ datapoints that were logaritmically distributed inside the frequency range. The RMS values decrease with increasing approximation order for all values of α in Table III for both magnitude and phase. This supports that the error of the higher-order approximations decreases across the entire frequency band of interest.

B. RC Ladder (Foster I) Realization

For use with an FGIC44, the approximation must be realized as a physical circuit. One realization method uses an RC-ladder structure such as the Foster I network shown in Fig. 3. This network uses parallel resistor/capacitor pairs (R_i, C_i where $i = 1, 2, ...n$) in series with each other and a single resistor (R_0). The impedance expression, $Z(s)$, of the Foster I network is given by:

$$Z(s) = R_0 + \sum_{i=1}^{n} \frac{\frac{1}{C_i}}{s + \frac{1}{R_i C_i}} \tag{12}$$

The values of the passive elements of the Foster I network can be calculated by equating the coefficients of (8) with those derived from the partial fraction expansion of the $Z(s)$ found in Table II given by:

$$Z(s) = k + \sum_{i=1}^{n} \frac{r_i}{s - p_i} \tag{13}$$

where k, r_i, and p_i are constants, residues, and poles of the impedance, respectively. From equating terms in (12) and (13), the values of resistors and capacitors in the network are given by:

$$R_0 = k \tag{14}$$

$$C_i = \frac{1}{r_i}(i = 1...n) \tag{15}$$

$$R_i = \frac{1}{C_i|p_i|} \tag{16}$$

Using (14)-(16) and the coefficients in Table II, the ideal component values for the 8-th order approximation of $C_\alpha = 16.3$ μF/sec$^{1-\alpha}$, $\alpha = 0.205$ and center frequency 31.7 kHz are given in Table IV. Values of E96 resistor and E24 capacitor series closest to the ideal were selected to realize the RC network. These nominal values are also given in Table IV. Note that to achieve target capacitance values, parallel capacitors were implemented for C_1, C_2, C_3, C_6, C_7, and C_8. In these cases, the two nominal values of these parallel capacitors are listed in Table IV.

IV. EXPERIMENTAL VALIDATION

The 8-th order approximation of the FOC using the Foster-I network was physically implemented using a printed circuit board design populated with the discrete E96 resistors and E24 capacitors with values from Table IV. To validate that the constructed network yielded the expected impedance, measurements of the electrical impedance were collected using a Agilent 4294A impedance analyzer in a bipolar (two-wire) measurement configuration. Measurements were collected from 1 kHz to 1 MHz and the values saved for transfer to a computer for further processing.

The experimental magnitude and phase data compared to both ideal and LTSpice simulations (of the RC ladder) are given in Figs. 4(a) and 5(a). Both experimental and LTSpice simulated impedance magnitude show very good agreement with the ideal values from 10 kHz to 1 MHz and the phase shows very good agreement from approximately 20 kHz to

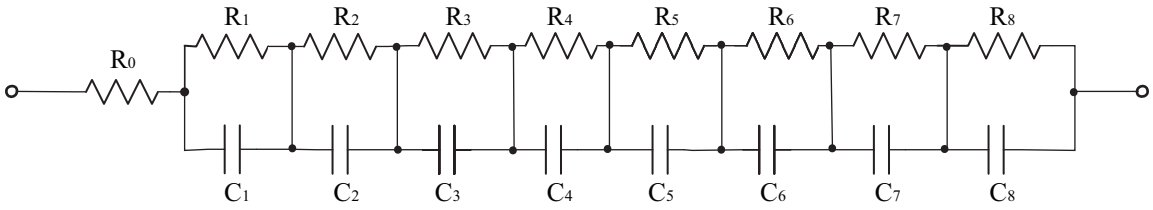

Fig. 3. Foster I topology of RC ladder network to realize 8-th order approximation of FOC.

TABLE IV
IDEAL AND NOMINAL ELEMENT VALUES FOR FOSTER I RC NETWORK FOC REALIZATION

Element	Ideal Resistance (Ω)	Nominal Resistance (Ω)	Element	Ideal Capacitance (F)	Nominal Capacitance (F)
R_1	1.06k	1.10k	C_1	123p	120p ‖ 3.30p
R_2	733	740	C_2	877p	820p ‖ 51.0p
R_3	654	647	C_3	2.61n	2.0n ‖ 0.68n
R_4	676	677	C_4	5.54n	5.6n
R_5	798	784	C_5	9.88n	10.0n
R_6	1.11k	1.096k	C_6	16n	15n ‖ 1.0n
R_7	1.98k	1.955k	C_7	25.5n	22n ‖ 3.30n
R_8	6.8k	6.81k	C_8	49n	47n ‖ 2.20n
R_0	1.6k	1.603k			

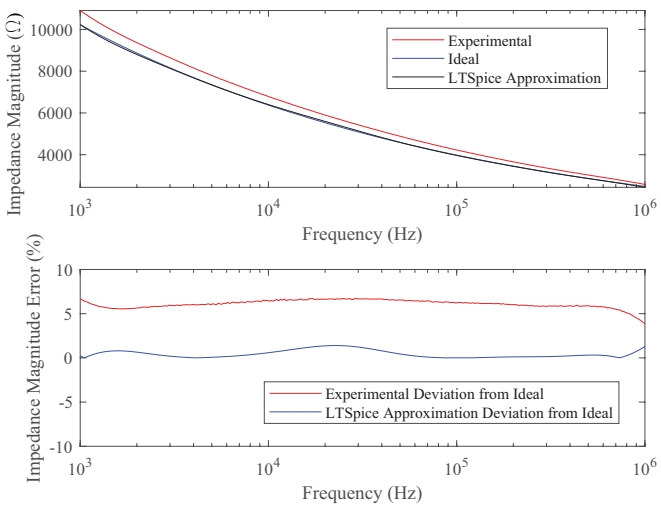

Fig. 4. Experimental and Ideal Impedance Magnitude Data Comparison for $\alpha = 0.205$

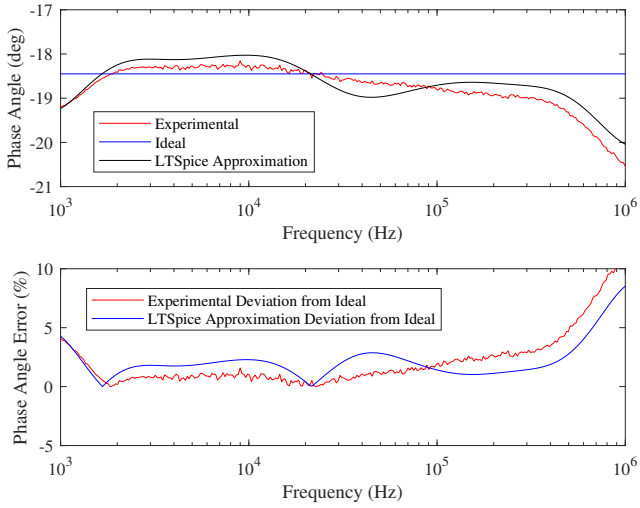

Fig. 5. Experimental and Ideal Phase Angle Data Comparison for $\alpha = 0.205$

500 kHz. To quantify the difference, the deviation of the experimental from the ideal values for magnitude and phase are shown in Fig. 4(b) and 5(b). The magnitude and phase have less than 6.8% and 5% deviation across the previously noted frequency bands of good visual agreement. The deviation of the experimental impedance magnitude/phase from the LTSpice simulations is attributed to deviations of the components from the nominal values due to their tolerances and also the introduction of parasitics from the PCB implementation.

V. CONCLUSION AND NEXT STEPS

The 8-th order approximation of the fractional-order capacitor in this work achieved the study requirements of magnitude/phase performance across three frequency decades (10 kHz - 1 MHz). This support the future use of this approximation with FGIC44 devices to realize immittances

with adjustable fractional-order (examples of the range of orders with this device are given in Table I).

While this work has designed and fabricated the necessary FOC approximation, further work is required to i) experimentally validate the fractional-order immittance realized when this design is used with the FGIC44 and ii) design further unity "seed" elements to increase the range of fractional-order immittances that can be realized and how the use of two seed approximations may impact the overall performance.

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