Rapid Inverse Design of GaN-on-GaN Diode with Guard Ring Termination for BV and $(V_FQ)^{-1}$ Co-Optimization

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***Abstract*—GaN-on-GaN vertical diode is a promising device for next-generation power electronics. Its breakdown voltage (BV) is limited by edge termination designs such as guard rings. The design space of guard rings is huge and it is difficult to optimize manually. In this paper, we propose an effective inverse design strategy to co-optimize BV and $(V_FQ)^{-1}$, where BV, V_F, and Q are the breakdown voltage, forward voltage, and reserve capacitive charge of the diode, respectively. Using rapid Technology Computer-Aided-Design (TCAD) simulations, neural network (NN), and Pareto front generation, a GaN-on-GaN diode is optimized within 24 hours. We can obtain structures with 200V higher BV at medium $(V_FQ)^{-1}$ or find a nearly ideal BV structure with 25% higher BV^2/R_{on} compared to the best randomly generated TCAD data.**

Keywords—Breakdown Voltage, Gallium Nitride (GaN), Machine Learning, Technology Computer-Aided Design (TCAD), Pareto Front

I. Introduction

GaN vertical diode is a promising device for next-generation power electronics applications [1]-[3]. GaN vertical diode can be formed on Ga-on-Sapphire (or other foreign substrates) wafers or GaN-on-GaN wafers. The former has a lower cost but has a larger leakage current due to threading dislocations [4]-[6]. Therefore, the GaN-on-GaN diode is preferred and chosen in this study.

While GaN has a much larger breakdown field than Silicon due to its large bandgap [7], the breakdown voltage of a GaN vertical diode is limited by the edge termination design [8] such as guard rings (Fig. 1) and junction termination extension (JTE) [9]. Guard-ring designs can have superior tolerance of process variability as compared to JTE, as they are less sensitive to the implant dose and depth. However, the design space of guard rings is huge because it depends on the ring's spacing (S), width (W), number (N), and junction gradient (σ). The design space explodes when the diode's capacitive charge (Q) and forward voltage (V_F) are considered which depend on the p-GaN thickness (D) and doping concentration in the anode and the guard rings. Currently, the GaN diode is designed based on human expertise assisted by simulations. Machine learning was recently used to optimize the static metrics of GaN HEMT [10]. However, there is no effective inverse design strategy to co-optimize BV and $(V_FQ)^{-1}$ with V_FQ as a switching Figure-Of-Merit (FOM) of power diodes.

In Ref. [11], TCAD, machine learning, and an optimizer are used to perform inverse design to optimize the breakdown voltage (BV) of a GaN-on-GaN vertical diode. In this paper, for the first time, we demonstrate a rapid inverse design strategy (~24 hours) on a GaN-on-GaN diode using TCAD, neural network (NN), and Pareto front generation to perform

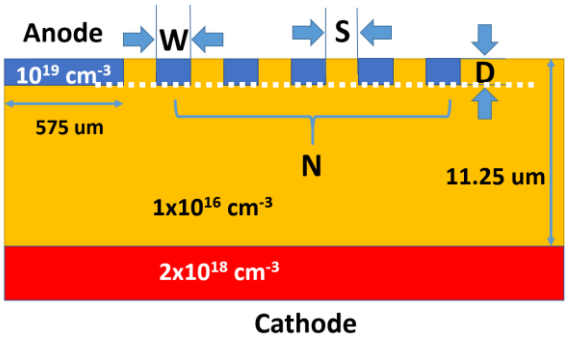

Fig. 1. GaN-on-GaN diode used in this study (not in scale for clarity). S, W, D, N, and σ (junction gradient, not shown) are varied in the TCAD structure generation with $S \in [0.25,5]$, $W \in [0.25,5]$, $D \in [0.01,1]$, $N \in [0,32]$, and $\sigma \in [0.01,0.1]$ (units all in μm except for N which is unitless). 266 structures are generated and simulated. Cylindrical coordinates are used and thus this is equivalent to a 3D simulation. The white dashed line shows the cutline in Fig. 10.

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N. Yee and A. Lu have equal contributions.

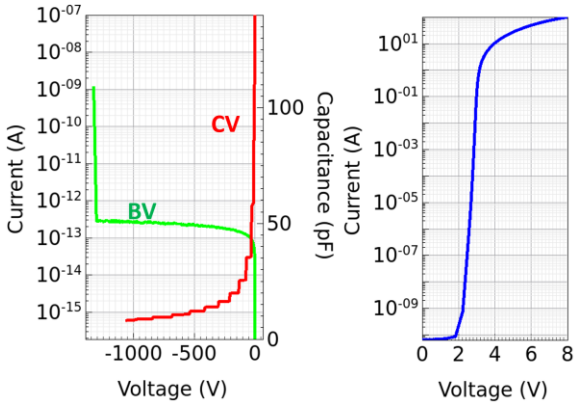

Fig. 2. The BV (left), CV (left), and pulsed-IV (right) of the random rapid-TCAD generated structure with the largest rapid-TCAD BV (-1770V). The curves shown are simulated using full TCAD models and the BV is about -1305V instead of -1770V rapid-TCAD BV (See also Fig. 7).

BV and $(V_F Q)^{-1}$ co-optimization, which allows the finding of optimized structures by training a neural network on sub-optimal TCAD structures (easy to obtain by randomly assigning S, W, D, N, and σ).

II. Simulation Setup

TCAD Sentaurus is used to generate and simulate vertical GaN-on-GaN diode [12]. The setup is based on Ref. [13] and the know-how in Refs. [6] and [14]. The structure is shown in Fig. 1 with guard rings added next to the anode for edge termination. The n-type drift region is 11.25µm and is doped with 10^{16}cm^{-3} Silicon. The anode and the guard rings are p-type and doped with 10^{19} cm^{-3} magnesium. Fermi-Dirac statistics, incomplete ionization, high-field mobility saturation, and impact ionization are turned on. Model parameters in Ref. [13] are used. The device has an anode radius of 575µm. To speed up the simulation, the substrate thickness is set to 3.25µm. This increases the forward current compared to a substrate with a normal thickness (e.g. 350µm) but can be calibrated by adding external resistance with mixed-mode simulation if needed.

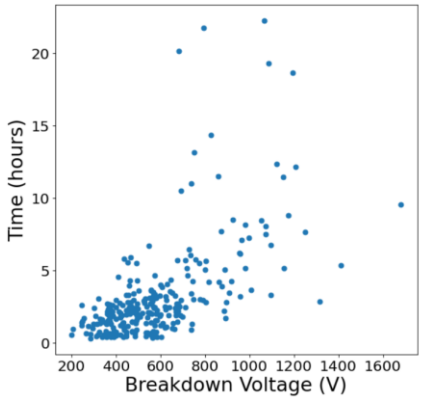

Fig. 3. Rapid-TCAD BV+CV simulation time distributions of the 266 structures using the rapid-TCAD simulation approach. High BV structures take longer simulation time and are rarer. Therefore, it is impossible to rely on random generation to achieve optimal structures. Some structures take more than 10 hours and thus it is important to use multiple cores. With 50 cores, all simulations finished in 24 hours.

III. Rapid TCAD Simulation

BV simulation is known to be time-consuming. The rapid-BV simulation method in [11] that provides ~5X speed up in BV simulations is used. In this method, impact ionization is removed and the peak electric field is monitored until it reaches 3.3MV/cm (GaN critical field). This allows rapid search for high BV devices which can then be verified using full TCAD simulation or experiment, if necessary.

266 structures have been randomly generated by randomly varying S, W, D, N, and σ (Fig. 1) and BV, pulsed-IV, and CV are simulated with a total simulation time of about 24 hours using 50 cores. Fig. 2 shows the TCAD results of the structure with the highest BV. V_F is defined when the forward current is 20A and Q is the integrated charge in the CV curve when the reverse bias reaches 60% of the BV. Fig. 3 shows the simulation time distribution of 266 structures as a function of BV.

IV. Neural Network And Pareto Front

Using the 266 rapid-TCAD data, an NN (Fig. 4) is trained to predict BV, R_{ON}, V_F, and Q as surrogate models with *S*, *W*,

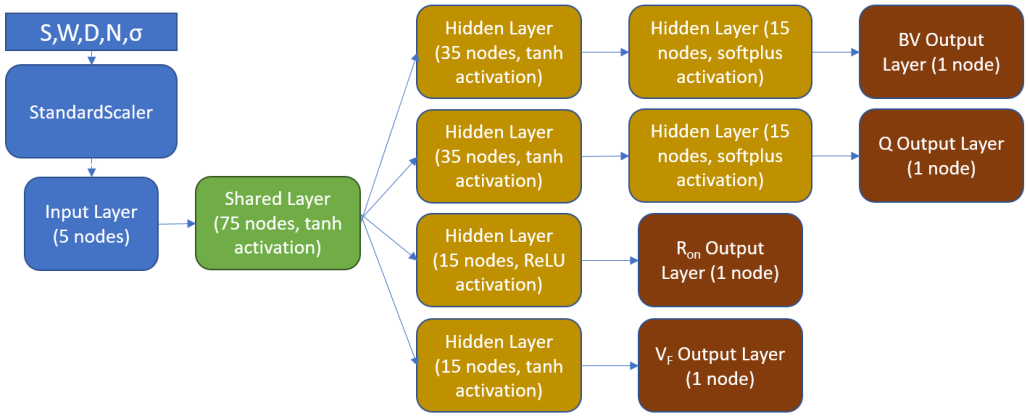

Fig. 4. The neural network built to predict BV, R_{ON}, V_F, and Q (reverse charge) with diode structure parameters as inputs.

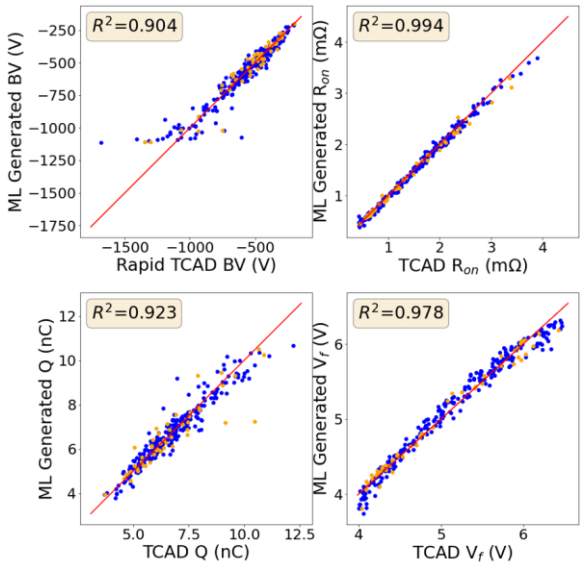

Fig. 5. Training (blue, 266 samples) and validation (orange, additionally 50 new samples) performance of the NN. Ideal prediction is shown in red lines where x = y. The R^2 of the training data are shown.

D, *N*, and σ as inputs. Fig. 5 shows the training and validation results. It can be seen that the model can predict the training and validation data well except for a saturation in the prediction of the BV at the high BV region due to the lack of high BV samples in the training data. However, this is proven not to be an issue in inverse design.

This NN is then used as a surrogate model to co-optimize the BV and $(V_FQ)^{-1}$ using the NSGA-II algorithm [15] as a multi-objective optimization problem to establish a Pareto front by maximizing both BV and $(V_FQ)^{-1}$ (Fig. 6). 150 generations are used to construct the Pareto front.

Fig. 7 shows the rapid TCAD simulation training data distribution and the Pareto front generated. For $(V_FQ)^{-1}$ in the $0.03V^{-1}(nC)^{-1}$ to $0.04\ V^{-1}(nC)^{-1}$ range, the BV is increased by up to 250V in the Pareto front prediction. For low $(V_FQ)^{-1}$,

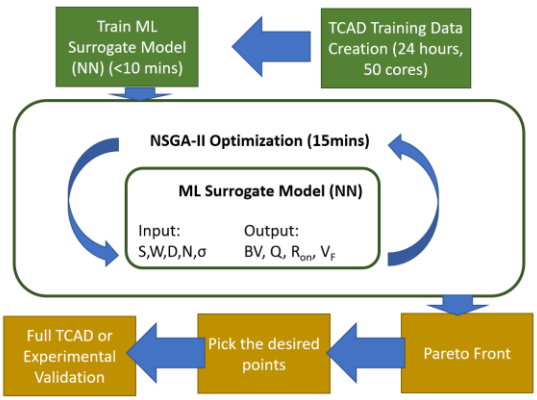

Fig. 6. The rapid inverse design framework. Rapid-TCAD is used to easily and randomly generate 266 sub-optimal structures. They are used to train a NN as the surrogated model, which will be used to find the Pareto front to discover structures with more superior performance without human expertise. The time used in each step is shown. Due to the rapid BV simulation and the use of Pareto front, inverse design and optimization can be finished in 24 hours.

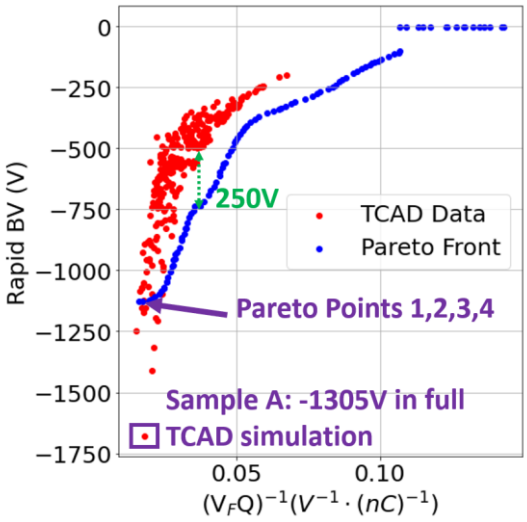

Fig. 7. Distribution of the rapid-TCAD training data and the optimized Pareto front in a BV vs. $(V_FQ)^{-1}$ plot. Note that the BV are obtained in rapid-TCAD simulation. The maximum BV obtained is only -1305V when the structure is simulated in full-TCAD simulation in Sample A.

there is a saturation in the BV prediction due to the saturation in the NN prediction in Fig. 5. Four points with the highest BV in the Pareto front were selected to be verified using full TCAD simulations. Their BV curves are shown in Fig. 8 and BV, R_{ON}, V_F, and Q are shown in Fig. 9. It can be seen that BV as large as -1995V is achieved which is almost 95% of the ideal 1-D parallel-plate limit (Fig. 8) and 25% higher BV^2/R_{on} compared to the best randomly generated TCAD data (Fig. 9).

Fig. 10 plots the E-field distribution of the structures with the highest BV discovered by the optimization process and by random TCAD generation using full-TCAD simulations. It can be seen that the designs discovered by the optimization

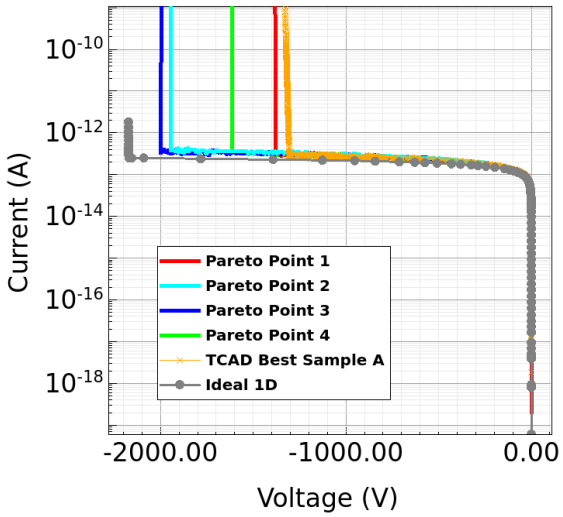

Fig. 8. BV plots of the 4 Pareto points with the highest BV, TCAD Best Sample A (see Fig. 7 and Fig. 9) and 1D ideal structure (parallel-plate limit).

	Structure Parameters					Figures of Merit (FOM)					
Pareto Points	G (μm)	W (μm)	N	σ (μm)	D (μm)	R_{on} (mΩ)	V_F (V)	Q (nC)	BV (V)	Normalized BV^2/R_{on}	Normalized $(V_FQ)^{-1}$
1	1.40	4.26	25	0.097	0.32	1.3	4.7	10.8	1383	0.79	1.1
2	1.39	4.91	32	0.100	0.70	2.8	5.7	13.9	1944	0.72	0.71
3	1.12	2.90	29	0.095	0.51	1.7	5.1	14.4	1995	1.25	0.76
4	1.37	5.00	32	0.097	0.41	1.8	4.9	11.8	1615	0.77	0.97
TCAD Best	1.13	3.11	9	0.094	0.30	0.91	4.6	12.2	1305	1	1

Fig. 9. The FOM and structures of the 4 best BV structures predicted by the Pareto front in Fig. 7. The structure and FOM of the training data from TCAD with the highest BV are also shown (Sample A in Fig. 7). All the data shown are simulated with full TCAD models. The pink boxes highlight the superior performance of the Pareto front structures compared to the training data.

process have successfully smoothed out the electric field to increase the breakdown voltage using the guard rings.

It should also be noted that the designs predicted by the Pareto front from $(V_FQ)^{-1} = 0.03V^{-1}(nC)^{-1}$ to $0.04\ V^{-1}(nC)^{-1}$ do not perform as well as the front indicates in the full-TCAD simulation. However, most of them still demonstrate an improvement in BV compared to the rapid-TCAD data with one of them as much as 200V.

V. Conclusion

Using a novel inverse design strategy, we can obtain GaN diode structures with 200V higher BV at medium $(V_FQ)^{-1}$ or find a nearly ideal BV structure with 25% higher BV^2/R_{on} compared to the best randomly generated TCAD data. This approach shows great potential to accelerate power device optimization using the data of low-cost sub-optimal devices.

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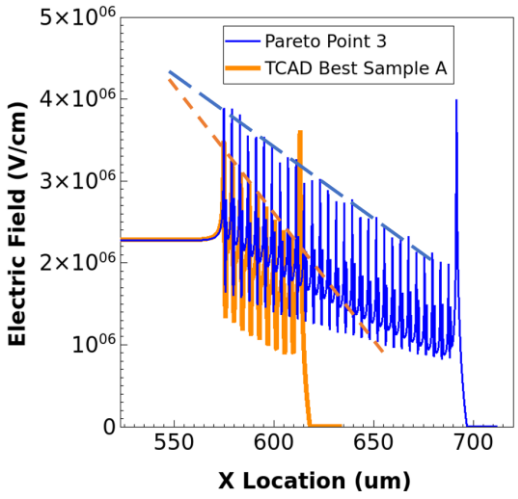

Fig. 10. Electric field distribution cutting at the junction along the white dashed line in Fig. 1 at breakdown for the TCAD Best Sample A (BV ~ -1350V) and Pareto Point 3 (BV ~ -1995V). Dashed lines are guidance to show that the Pareto Point 3 is more effective in smoothing the E-field.

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