A Wideband Low RMS Phase/Gain Error mm-Wave Phase Shifter in 22-nm CMOS FDSOI

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***Abstract*— A 5-bit low-power and compact active mm-wave phase shifter (PS) with low rms phase/gain error is implemented in 22-nm CMOS fully depleted silicon on insulator (FDSOI) technology for 5G multi-input multi-output (MIMO) phased arrays. The proposed phase shifter uses a gain-boosted two-stage *RC* poly-phase filter (PPF), which maintains reasonable phase accuracy features while compensating for the gain response. The system uses a reactance invariant cascode vector modulator (VM), which results in constant loading effect for quadrature network, therefore improving rms phase/gain error. The phase shifter shows measured rms phase error of <4° at 24–36 GHz. The measured mean gain is from −8.2 to −5 dB at 24–36 GHz, and the rms gain error is <0.6 dB at 24–36 GHz. The total power consumption of the proposed phase shifter is 7.2 mW, and the chip area is 612 × 953 μm including pads.**

***Index Terms*— 5G, active phase shifter (PS), fully depleted silicon on insulator (FDSOI) technology, in-phase and quadrature (IQ) network, mm-wave, *RC* poly-phase filter (PPF), vector modulator (VM), wideband phase shifter.**

I. Introduction

PHASE shifters (PSs) are one the most important elements in a phased array system. Phase shifters are realizable in either passive or active versions. Passive ones can be implemented in different ways, such as LC-network [1], [2], [3], reflection-type [4], [5], [6], and loaded line phase shifters [7], [8]. Passive phase shifters have the advantage of providing very good linearity and consuming very low to zero dc power. However, they suffer from high insertion loss (IL).

Active phase shifters are mainly based on a vector summing technique, and any phase or amplitude mismatch directly degrades the accuracy of the phase shifter. Having an accurate quadrature generator, high linearity, and low power consumption are the main challenges in designing an active phase shifter. In [9], a differential quadrature all pass filter (QAF) is presented. The major drawback of this circuit is its sensitivity to capacitive loading effect. In [10], an improved version of QAF is presented to compensate its sensitivity to the capacitive load while maintaining good phase accuracy but at the cost of 6-dB loss in addition to [9]. In [11], a g_m-C poly phase filter (PPF) quadrature network is presented to compensate the gain response of the conventional RC PPF quadrature network at the cost of increasing the power consumption, dramatically. In [12], a conventional two-stage RC PPF is presented, which has the best phase accuracy but suffers from having very high loss (around 11 dB). In [13], a novel two-stage RC PPF quadrature network is presented, whose inductors are used instead of capacitors in the second stage to achieve gain boosting, but the 20-25 GHz phase shifter uses four 700 pH, and due to lower SRF of inductors to make them more compact, the frequency of operation is limited. In [14], a two-stage RC PPF with power splitting is used to increase the gain response of the quadrature network, but due to using the power splitting circuit and the fact that the value of resistors and capacitors in the first and second stages of RC PPF are the same, the structure suffers from low phase accuracy over wide bandwidth. In this article, a 5-bit active mm-wave phase shifter is presented with wide bandwidth (12 GHz), small rms phase and gain error (4°, 0.6 dB), low-power consumption (7.2 mW), and small size (0.6 mm^2). Two major modifications to enhance the accuracy and the gain response of the quadrature network are as follows: 1) employing a loss-compensated two-stage RC PPF to compensate for high IL while maintaining the phase accuracy and 2) using a reactance invariant cascode vector modulator (VM) to have constant loading effect seen by quadrature network, therefore improving rms phase/gain error.

II. System-Level Architecture

The block diagram of the proposed phase shifter is shown in Fig. 1. The input (output) is a single-ended signal matched to 50 Ω. Therefore, a single-ended to differential (differential to single-ended) matching network is used. A two-stage RC PPF circuit with two shunt inductors at its output is used to maintain properties of a conventional PPF, including low phase error and at the same time increasing the voltage gain by 5.5 dB at mid-band compared with its conventional counterpart. Next, capacitor banks are placed in parallel with the inputs of VM to provide constant reactance at the input and are controlled by a digital unit. Then, quadrature signals are generated and fed into the VM. The VM input voltage signals are converted to currents through the phase-invariant amplifier (PGA) and are added together with adjusted amplitudes using a 5-bit DAC.

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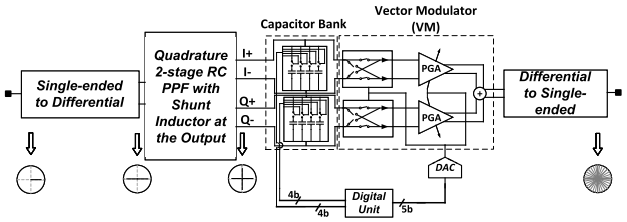


Fig. 1. Block diagram of the proposed phase shifter.

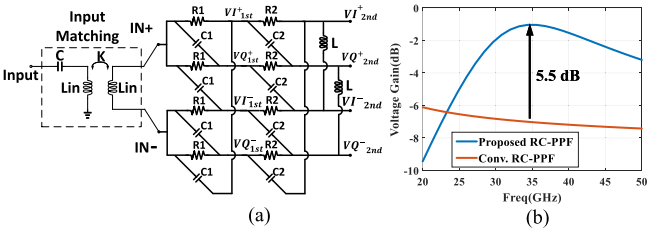
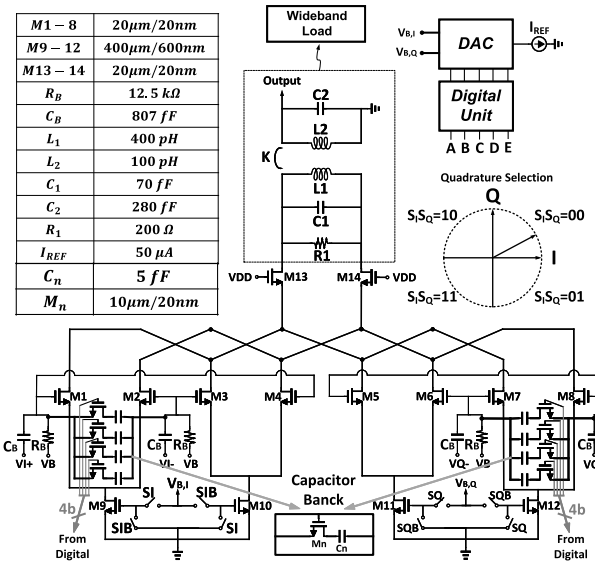


Fig. 2. Proposed two-stage RC PPF. (a) Schematic. (b) Voltage gain frequency response comparison with conventional counterpart. ($C = 101$ fF, $K = 0.5$, $L_{\text{in}} = 500$ pH, $R_1 = 100\ \Omega$, $C_1 = 64$ fF, $R_2 = 100\ \Omega$, $C_2 = 43$ fF, $L = 350$ pH, and $Q = 20.5$ at 40 GHz.)



$M1-8$	$20\mu m/20nm$
$M9-12$	$400\mu m/600nm$
$M13-14$	$20\mu m/20nm$
R_B	$12.5\ k\Omega$
C_B	$807\ fF$
L_1	$400\ pH$
L_2	$100\ pH$
C_1	$70\ fF$
C_2	$280\ fF$
R_1	$200\ \Omega$
I_{REF}	$50\ \mu A$
C_n	$5\ fF$
M_n	$10\mu m/20nm$

Fig. 3. Circuit schematic of the proposed wideband VM.

III. Circuit Design

A. In-phase and quadrature (IQ) Network

To alleviate the relatively high IL of the conventional RC PPF, the structure shown in Fig. 2(a) is proposed where only two inductors are added to the output of the circuit. To show the effect of this modification, for simplicity, the voltage gain transfer function of a one-stage RC PPF with two shunt inductor can be written as follows:

$$\frac{VI+}{V_{\text{IN,diff}}} = \frac{Ls(1 - R_1C_1s)}{LC_1R_1s^2 + Ls + 2R_1}. \tag{1}$$

As shown in (1), this transfer function has gain boosting compared with its conventional counterpart with a voltage gain of 0 dB due to the presence of the second-order polynomial in its denominator. Fig. 2(b) shows the post-layout simulation of the proposed two-stage RC PPF with shunt inductor EM simulated using SONNET [15] and the conventional two-stage RC PPF with 5.5 dB voltage gain boosting. To investigate the phase behavior of the proposed two-stage PPF, the output voltage of the VI^+_{2nd} and VQ^+_{2nd} can be driven as follows:

$$\frac{VI^+_{\text{2nd}}}{VQ^+_{\text{2nd}}} = \frac{\left(\frac{VI^+_{\text{1st}}}{VQ^+_{\text{1st}}}\right) - R_2C_2s}{1 + \left(\frac{VI^+_{\text{1st}}}{VQ^+_{\text{1st}}}\right) \times R_2C_2s} \tag{2}$$

which shows that the phase response of the proposed two-stage RC PPF is exactly identical to its conventional counterpart [12].

B. Reactance Invariant VM

Fig. 3 shows the VM circuit schematic. It is composed of S_I and S_Q switches along with PGAs. The quadrature signals generated in the two-stage RC PPF are applied to the input of the VM. The VM performs two tasks on these quadrature signals to be able to create 0°–360° phase shifting: 1) by using switches S_I and S_Q, the sign of each I and Q signal is changed accordingly and 2) by changing the dc currents of the current-source (CS) transistors of the VM (M9–M12) using a DAC, the ac currents of the VM input transistors (M1–M4 in I path and M5–M6 in Q path) and, hence, their quadrature addition are adjusted [12]. The implemented VM takes advantage of using the cascode structure (M13 and M14) to better isolate summing part from output matching section, which results in more constant gain with respect to different phase shifting steps.

One of main advantages of RC-PPF type quadrature network is that, with the same loading effect from VM, the phase accuracy and amplitude imbalance of I and Q sections are not affected. Since dc currents of the VM for I and Q sections are not the same for different phase steps, their loading effect is different, which degrades the phase/gain accuracy of the quadrature network, and the worst case scenarios occur for phase shiftings of 0°/90°/180°/270°. For example, in 0° (digital input = "00000") phase state, the I section of the VM is completely "ON" and the Q section is "OFF," and this causes the capacitance value difference in the I and Q sections of the VM (the load of the quadrature network) and results in gain/phase mismatch. To compensate for this mismatch, two sets of capacitor banks each including four parallel capacitors with series switches, as shown in Fig. 3, are placed in shunt with the I/Q sections of the VM input. Since the difference between capacitance values of two sections is deterministic, a digital circuit is designed that turns the switch of the capacitor banks "ON" and "OFF" based on the digital input. Each unit achieves an ON capacitor of 10 fF and an OFF capacitor of 5 fF. The values of these capacitors are determined based on the code in the digital unit, which results in constant loading effect for each phase step. The comparison of capacitance variation between the I and Q sections of VM when calibration is ON and OFF is shown in Fig. 4(a), where in the proposed approach, the capacitance variation is limited to 5 fF.

IV. Fabrication and Measurement Results

The phase shifter is implemented using 22-nm FDSOI CMOS technology and occupies an area of 953 μm × 612 μm (including pads). The die photograph is shown in Fig. 4(b). The chip is measured using ON-chip ground-signal-ground (GSG) probing and short-open-load-through (SOLT) calibration. Using a supply voltage of 1.2 V, a power consumption

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART PSs

Ref.	Frequency [GHz]	No. of bits	RMS Phase Error [°]	RMS Gain Error [dB]	Gain [dB]	Power [mW]	Area [mm^2]	IP1dB [dBm]	Technology
This work	**24 - 36**	**5**	**< 4**	**< 0.6**	**-8.2 ∼ -5**	**7.2**	**0.6**	**< 4**	**22-nm FDSOI**
[16]	29.5 - 33.5	4	< 4.9	< 0.4	-2.8	18	0.21	-	65-nm CMOS
[10]	60 - 80	4	< 9.1	< 1.3	11 - 14.7	108	1.058	-27	0.13-μm SiGe BiCMOS
[13]	20.8 - 25	7	< 1.17	< 0.13	-3.5	6.6	0.134	-	65-nm RF CMOS
[5] & [17]	27 - 29	5	< 4.3	-	9.5	10	0.32	-22	65-nm CMOS
[18]	8 - 12	5	< 4.6	0.6	-1.25 ∼ -1.75	73.92	0.6	-	0.18-μm SiGe BiCMOS

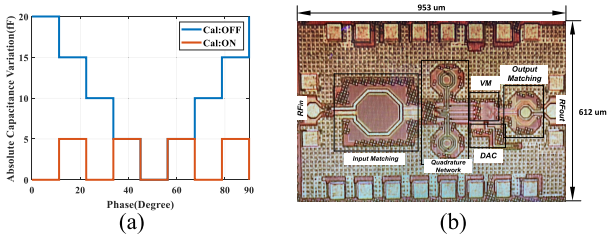


Fig. 4. (a) Absolute value of input capacitance variation between I and Q paths in the VM. (b) Chip photograph of the proposed 5-bit phase shifter.

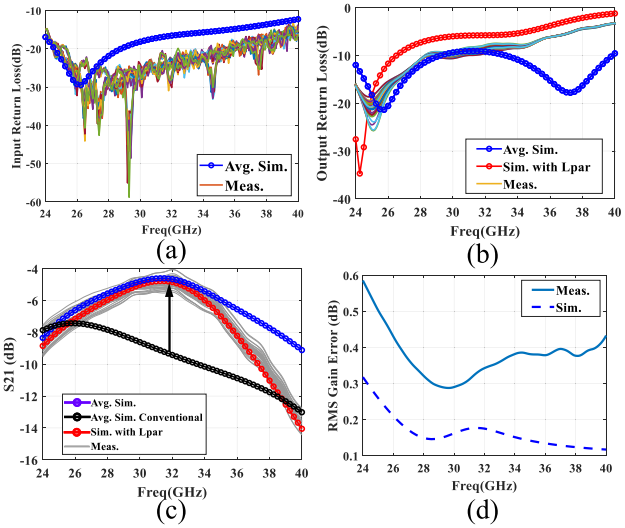


Fig. 5. Measured and simulated S-parameters for 32 phase steps. (a) Input return loss. (b) Output return loss. (c) $S21$. (d) RMS gain error.

of 7.2 mW is measured. Fig. 5(a) and (b) shows the input and output return loss ($S11$ and $S22$) of the fabricated PS for 32 phase steps. These results show that $S11$ and $S22$ are not sensitive to different phase states. The lower band response of the measured output return loss is well matched to the average simulation result, but there is a difference in higher band frequencies, which is most probably due to two reasons: 1) the parasitic inductance (Lpar = 25 pH) that is series with $C2$ in Fig. 3 which Fig. 5(c) shows that with considering EM simulated Lpar the results are close to measurements and 2) the custom filling cells for inductors and the fact that their behavior cannot be predicted using SONNET EM simulation. Fig. 5(c) shows the IL ($S21$) of the PS for 32 different

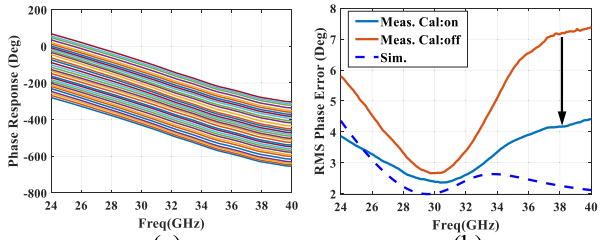


Fig. 6. (a) Measured phase response of the PS for 32 different phase steps. (b) Measured and simulated rms phase error.

phase states. The measured $S21$ very well follows the average simulation result for 24–36 GHz, but at higher frequencies (36–40 GHz), there is a discrepancy due to the same reason. Also, $S21$ of a conventional two-stage RC PPF is compared with the proposed RC PPF in Fig. 5(c), which shows the gain improvement. Fig. 5(d) shows the measured rms gain error of the PS is less than 0.6 dB at 24–40 GHz. Fig. 6(a) shows the measured phase response of the PS for 32 different phase steps. Fig. 6(b) shows that the measured rms phase error of the PS is less than 4.3° at 24–40 GHz with calibration. With calibration on, the result is better at least by 1° especially at higher frequency where the loading is more sever. Also, the measured rms phase error versus input power shows 0.65° variation from −30- to 10-dBm input power. The chip performance and comparison with the state of the art are summarized in Table I.

V. CONCLUSION

A 5-bit mm-wave active phase shifter with low rms phase and gain errors is presented in this article. The measurement results show an rms phase error of <4° at 24–36 GHz, a measured mean gain ranging from −8.2 to −5 dB at 24–36 GHz, and an rms gain error of <0.6 dB at 24–36 GHz. The total power consumption is around 7.2 mW, while the measured input referred P1dB is <4 dBm over the entire frequency band of interest.

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