

A 27.5–46.2-GHz Broadband Low Noise Amplifier With IP₃ Enhancement

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Abstract—This letter presents a 27.5–46.2-GHz broadband low-noise amplifier (LNA) featuring IP₃ enhancement. The LNA bandwidth (BW) is extended by implementing dual-resonant input matching and a broadband output network. The LNA IP₃ is enhanced by incorporating parallel PMOS and NMOS paths in the second stage, with their output currents combined through a three-winding transformer. Implemented using the GlobalFoundries 45-nm CMOS silicon-on-insulator (SOI) process, the LNA demonstrates 27.5–46.2 GHz effective BW, 2.1 dB minimum noise figure (NF), and 19.8 dB peak gain. The measured IIP₃ is –3.6 dBm at 34 GHz under 25.5 mW DC power consumption. Compared to recently reported broadband LNAs with a similar frequency range, this design achieves the state-of-the-art NF, IIP₃, and figure-of-merit (FoM).

Index Terms—5G, bandwidth (BW), broadband, CMOS, IP₃, linearity, linearization, low noise amplifier (LNA), millimeter-wave (mmWave), three-winding transformer.

I. INTRODUCTION

THE past few years have seen a growing interest in the development of instantaneously broadband transceivers, aiming to cover multiple mmWave 5G bands simultaneously [1], [2]. For such applications, in addition to having wide bandwidth (BW), high gain, and low noise figure (NF), the low-noise amplifier (LNA) also needs to present high linearity to suppress interference and maintain high sensitivity [3]. Despite recent advances in broadband mmWave LNAs [4], [5], [6], [7], [8], [9], achieving high IP₃ with a low NF is still challenging.

Recently, we report a systematic design methodology for expanding the BW of mmWave LNAs in [9]. It is based on the classic cascode common-source (CS) with inductive degeneration topology and can turn an existing narrowband LNA design into a broadband implementation by only updating component values, thereby incurring minimal area overhead and NF degradation. Due to space constraints, readers interested in the detailed design guidelines and design equations for enhancing the input matching BW and gain BW are encouraged to refer to [9].

The work presented in this letter builds upon our prior work [9] with an emphasis on improving linearity. It is achieved by incorporating a pair of PMOS and NMOS paths

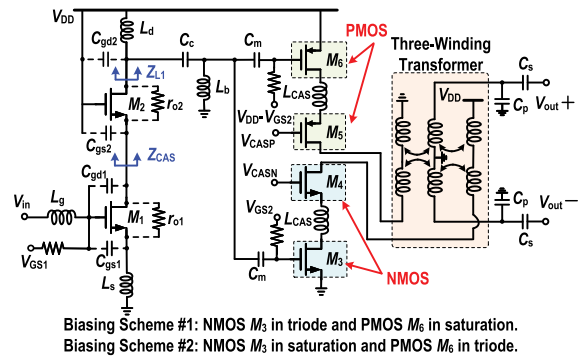


Fig. 1. Schematic of the proposed broadband LNA with IP₃ enhancement.

in the second stage, with their output currents combined through a three-winding transformer (see Fig. 1). The combined PMOS and NMOS output current presents a close-to-zero net third-order nonlinearity coefficient g_{m3} when one of the CS transistors operates in triode and the other in saturation. Additionally, the use of the three-winding transformer enhances the magnetic coupling of the output network while separating the DC currents of the PMOS and NMOS paths.

This letter is organized as follows. Section II elaborates on the LNA implementation details, including the IP₃ enhancement using parallel PMOS and NMOS paths, and the broadband output network design. Section III presents the measurement results. Section IV concludes this letter and presents a performance comparison with state of the art.

II. LNA IMPLEMENTATION

A. Linearity Enhancement Using Parallel PMOS and NMOS Paths in the Second Stage

In multistage amplifiers, linearity is usually limited by the latter stages [10]. Therefore, we choose to embed the IP₃ enhancement circuit into the second stage of our LNA design.

The nonlinearity of the amplifier output current can be modeled using a polynomial, as follows:

$$i_{\text{out}} = g_{m1}v_{\text{in}} + g_{m2}v_{\text{in}}^2 + g_{m3}v_{\text{in}}^3 \quad (1)$$

where $g_{m1,2,3}$ represent the linear transconductance and second-/third-order nonlinearity coefficients, respectively. A common technique for improving the LNA IP₃ is the derivative superposition (DS) [3], a.k.a., multiple gated transistors (MGTR). It combines the output currents of a main transistor, biased in the strong inversion region, and multiple auxiliary transistors, biased in the weak inversion region, to realize a close-to-zero net g_{m3} . Note that the conventional DS technique only

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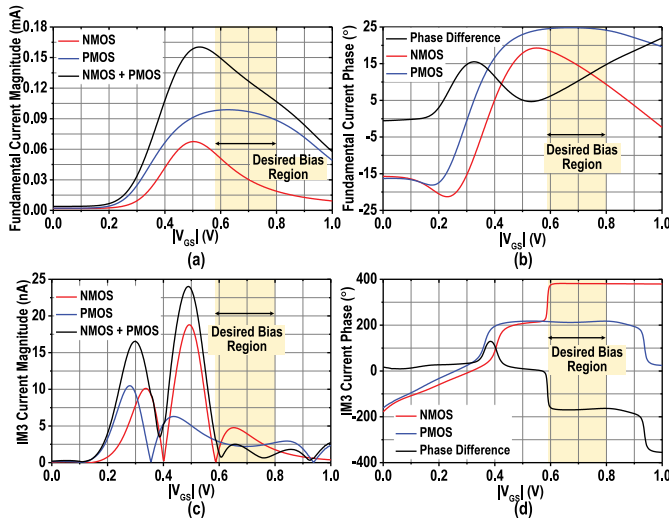


Fig. 2. (a)–(d) Simulated output current amplitudes and phases of the fundamental and IM3 tones. When $|V_{GS}|$ is ~ 0.6 V, the NMOS M_3 is biased in triode and the PMOS M_6 is biased in saturation.

incorporates NMOS transistors, often resulting in a degraded IP_2 because the g_{m2} of the main and auxiliary NMOS transistors have the same sign. This issue can be mitigated by the complementary DS technique [3], which employs a pair of NMOS and PMOS transistors. As $g_{m2,P}$ and $g_{m2,N}$ exhibit opposite signs, their combined g_{m2} can still remain small.

However, the complementary DS technique becomes less effective at mmWave frequencies. This is because the device sizes of the strong-inversion and weak-inversion transistors are quite different, leading to distinct parasitic capacitances at their outputs, which in turn, results in a substantial phase mismatch between the output currents of the NMOS and PMOS paths at high frequencies.

To address this challenge, we propose a new biasing scheme for the complementary DS technique. The device sizes of the NMOS CS transistor M_3 and the PMOS CS transistor M_6 are set to be identical, with the same $|V_{GS}|$ (see Fig. 1). Then, one of them is biased in the saturation region with a higher $|V_{DS}|$, while the other is biased in the triode region with a lower $|V_{DS}|$. The transistor operating in triode exhibits a different g_{m3} nonlinearity compared to the transistor in saturation due to the mobility degradation effect [11], which is leveraged for IP_3 enhancement in this work. Specifically, we set the PMOS cascode biasing V_{CASp} to 0.1 V and the NMOS cascode biasing V_{CASn} to 0.5 V, respectively. This results in M_6 being biased in saturation and M_3 being biased in triode when $|V_{GS}|$ is ~ 0.6 V (Fig. 1). We then simulate the output current amplitudes and phases of the fundamental and IM3 tones of the PMOS and NMOS paths with a two-tone input at 38 and 38.1 GHz. As shown in Fig. 2, when $|V_{GS}|$ is ~ 0.6 V, the IM3 current magnitudes of the PMOS and NMOS paths are nearly equal, with a close-to- 180° phase difference between them. As a result, the simulated net IM3 output current is almost zero, leading to a high IP_3 .

It is worth noting that the simulated phase mismatch of the fundamental output currents between the PMOS and NMOS paths is very small [Fig. 2(b)], which is fundamentally different than the conventional complementary

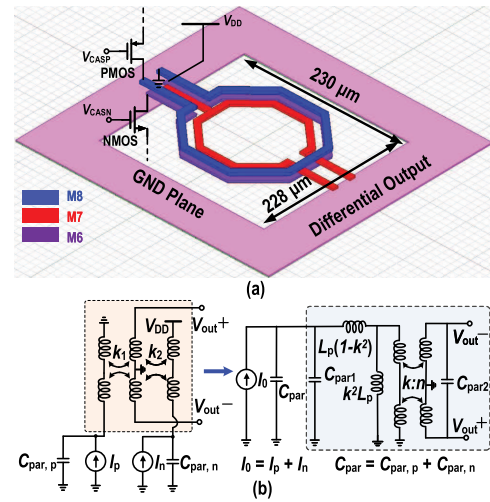


Fig. 3. (a) Three-dimensional EM model of the output three-winding transformer. (b) Its equivalent circuit model.

DS technique with distinct transistor sizes for NMOS and PMOS. This ensures that the proposed transistor sizing and biasing scheme can enhance the IP_3 and fundamental output current simultaneously. From Monte Carlo simulations, the average phase difference between the PMOS and NMOS IM3 currents is 168.5° , with a standard deviation of 2.0° . At the same time, the average phase difference between the PMOS and NMOS fundamental currents is 7.3° , with a standard deviation of 1.0° . These simulations indicate the robustness of the proposed method in achieving reduced IM3 and enhanced fundamental output simultaneously.

Similarly, we can bias the NMOS M_3 in saturation and the PMOS M_6 in triode by setting V_{CASp} to 0.8 V, V_{CASn} to 1.2 V, and $|V_{GS}|$ to ~ 0.6 V. This configuration can also achieve in-phase fundamental output current combining and near-zero IM3 output in the simulation.

B. Transformer-Based Broadband Output Network

To combine the output currents of the PMOS and NMOS paths, we adopt a three-winding transformer as the output network (see Fig. 3). The primary coil on M_6 is connected between the NMOS output and V_{DD} , the primary coil on M_8 is connected between the PMOS output and ground (GND), and the secondary coil on M_7 is connected to the differential output. This sandwich structure enhances the magnetic coupling between the PMOS/NMOS primary coils and the output coil, thereby reducing the passive loss. Additionally, the differential output facilitates the integration of the LNA into the receiver chain. In Fig. 3(b), k_1 models the magnetic coupling coefficient between the M_8 coil and the M_7 output coil, and k_2 models the magnetic coupling coefficient between the M_6 coil and the M_7 output coil. Since $k_1 \approx k_2 \approx k = 0.43$, we can directly combine the PMOS and NMOS output currents, yielding a typical two-port transformer model [12], [13] to facilitate the network design, as in Fig. 3(b). The transformer parameters (i.e., L_p , k , and n) and the capacitors C_p and C_s are chosen to realize broadband transimpedance gain from the current source to the load while absorbing the transistor parasitic capacitance. Detailed design guidelines and equations for the transformer parameters can be found in our prior work [9].

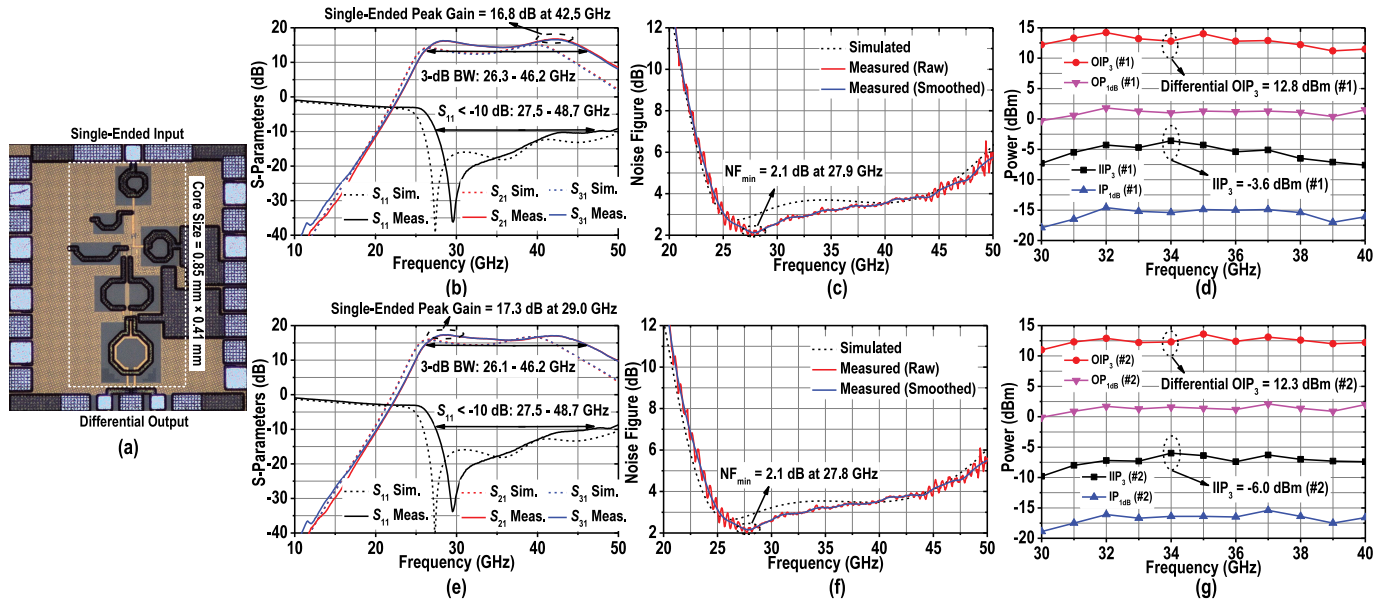


Fig. 4. (a) Chip micrograph. (b)–(d) Measured S-Parameters, NF, IP₃, and P_{1dB} for the biasing scheme #1 (NMOS M_3 in triode and PMOS M_6 in saturation). (e)–(g) Measured S-Parameters, NF, IP₃, and P_{1dB} for the biasing scheme #2 (NMOS M_3 in saturation and PMOS M_6 in triode).

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART BROADBAND MMWAVE LNAs

Reference	BW* (GHz)	3-dB BW (GHz)	Peak Gain (dB)	NF (dB)	IIP ₃ (dBm)	IP _{1dB} (dBm)	P _{DC} (mW)	Core Size (mm ²)	FoM**	Technology
This Work	27.5–46.2	26.3–46.2 ^a 26.1–46.2 ^b	19.8 ^a 20.3 ^b	2.1–4.4	-3.6 ^a -6.0 ^b	-14.6 ^a -15.4 ^b	25.5 ^a 27.4 ^b	0.35	1380 ^a 828 ^b	45-nm CMOS SOI
TCAS-I 2020 [5]	26.3–47	22–47	22.2	3.0–4.3	-13.8	-22.6	9.5	0.13	430	0.13- μ m SiGe
JSSC 2021 [6]	22.9–38.2	22.9–38.2	14.5	2.6–4.6	-3.6	-13.2	18.9	0.16	400	28-nm CMOS
MWCL 2022 [7]	20–44	18–44	19.5	2.6–3.5	-8.9 ^{††}	-18.5	17	0.16	667	65-nm CMOS
MWCL 2022 [8]	21.4–41.1	21.3–41.1	20.3	2.9–3.6	-6.1 ^{††}	-15.7	27.5	0.13	669	28-nm FDSOI
TCAS-I 2023 [9]	27–46	25.5–50	21.2	2.4–4.2	-9.5	-17.4	25.5	0.38	424	45-nm CMOS SOI

* Intersection of 3-dB gain BW and 10-dB return loss BW.

^a PMOS M_6 in saturation and NMOS M_3 in triode.

^{††} Estimated using IP_{1dB} + 9.6 dB.

^b PMOS M_6 in triode and NMOS M_3 in saturation.

** $FoM = \frac{10^3 \times Gain[\frac{W}{W}] \times BW_{eff}[GHz] \times IIP_3[mW]}{P_{DC}[mW] \times (NF[linear]-1) \times f_c[GHz]}$, f_c is the geometric mean, peak gain and minimum NF are taken in FoM calculation.

III. MEASUREMENT RESULTS

The high-linearity broadband LNA prototype is fabricated using the GlobalFoundries 45-nm CMOS silicon-on-insulator (SOI) process. The chip micrograph is shown in Fig. 4(a).

When the NMOS M_3 is biased in triode and the PMOS M_6 is biased in saturation (the biasing scheme #1), the measured DC current is 19.6 mA. Its measured S-Parameters, NF, IP₃, and P_{1dB} are summarized in Fig. 4(b)–(d). Here, we define the effective LNA BW as the intersection of the 3-dB BW and 10-dB return loss BW [4]. The measured effective LNA BW is 27.5–46.2 GHz. The single-ended peak gain is 16.8 dB at 42.5 GHz, resulting in a differential peak gain of 19.8 dB. The differential outputs are well-balanced across the effective BW. The measured in-band gain ripple is 2.5 dB, and the measured group delay remains between 45 and 70 ps from 30 to 47 GHz. For the NF measurement, the minimum NF is 2.1 dB at 27.9 GHz, and the NF remains < 4.4 dB within the effective BW. The measured best IIP₃ is -3.6 dBm at 34 GHz. The measured IIP₃ remains higher than -7.6 dBm and the measured IP_{1dB} remains higher than -18.0 dBm from 30 to 40 GHz. Compared to our prior work [9], which has the same first stage as this design but

an NMOS-only second stage that is biased in saturation, this work achieves ~6 dB IP₃ improvement with very similar gain, NF, and power consumption.

Similar LNA performance is measured when the NMOS M_3 is biased in saturation and the PMOS M_6 is biased in triode (the biasing scheme #2), as shown in Fig. 4(e)–(g). This configuration achieves 0.5 dB higher gain but 2.4 dB lower IP₃ at 34 GHz with 21.1 mA DC current.

IV. CONCLUSION

This letter presents a 27.5–46.2-GHz broadband LNA with IP₃ enhancement. The IP₃ enhancement is enabled by combining the output currents of parallel PMOS and NMOS paths in the second stage through a three-winding transformer. For the PMOS and NMOS CS transistors, they are implemented using the same size, with one transistor biased in saturation and the other biased in triode. This new biasing scheme ensures an in-phase combining of the fundamental currents with a near-zero net g_{m3} . A performance comparison table with recently reported broadband LNAs operating in a similar frequency range is shown in Table I. This design achieves the state-of-the-art NF, IIP₃, and figure-of-merit (FoM).

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