Vacuum annealed β-Ga_2O_3 recess channel MOSFETs with 8.56 kV Breakdown Voltage

Shivam Sharma, Lingyu Meng, A F M Anhar Uddin Bhuiyan, Zixuan Feng, David Eason[1], Hongping Zhao, *Senior Member, IEEE* and Uttam Singisetti, *Senior Member, IEEE*

***Abstract*— This letter reports vacuum annealing of late--ral field-plated β-Ga_2O_3 MOSFETs with significant current recovery and improvement in the on-state resistance, R_{on}, after Reactive Ion Etching (RIE) induced damage. We fabricate and characterize MOSFETs based on Molecular Beam Epitaxy (MBE) and Metal-Organic Chemical Vapor Deposition (MOCVD) grown β-Ga_2O_3 wafers to better understand the effects of vacuum annealing. We see a clear trend of vacuum annealed devices showing no reduction in breakdown voltages, V_{br}, as compared to polymer passivated MOSFETs. This trend holds for identical gate-drain separation, L_{gd}, varying from 20 µm to 60 µm. Devices show up to 10 times reduction in R_{on} as compared to previously reported R_{on} for SU-8 passivated devices. For MBE sample, V_{br} of 7.16 kV for a L_{gd} = 40 µm device, with an average field strength of 1.79 MVcm^{-1} and peak drain current density of 40 mA/mm, is reported. R_{on} is 897 Ω·mm, giving Baliga's Figure of Merit (BFOM) as 5.71 MWcm^{-2}. For a L_{gd} = 60 µm device, we report record high breakdown of 8.56 kV with BFoM of 4.9 MWcm^{-2}. For MOCVD grown sample, a L_{gd} = 60 µm device has V_{br} of 6.11 kV, R_{on} of 1.98 kΩ·mm and corresponding BFoM of 1.88 MWcm^{-2}. Transfer Length Method (TLM) analysis indicates incomplete post etch current recovery after vacuum annealing.**

***Index Terms*— Gallium oxide, field-plate, MOSFET, vacuum annealing, breakdown voltage, electron device.**

I. Introduction

β-GALLIUM oxide (Ga_2O_3) has emerged as an excellent material for efficient power devices and RF electronics due to its exceptional electronic properties[1-3]; giving high Baliga's Figure of Merit (BFOM). Tremendous progress has been made in Ga_2O_3 devices in terms of breakdown voltages, average field strengths and power device figures of merit [4-8]. Kilovolt (kV) class breakdown voltages, V_{br}, have been reported in Schottky barrier diodes [9-15] and MOSFETs[4, 5, 7, 16-21]. Recently, lateral field-plated and SiN_x/SiO_2 passivated MESFETs on Metal-Organic Chemical Vapor Deposition (MOCVD) grown Ga_2O_3 were demonstrated with record kV rating and high BFOM [4, 7]. These devices used regrowth of the source/drain layers to form low resistance contacts. However, the devices have not yet approached the theoretical limits as predicted by the BFOM.

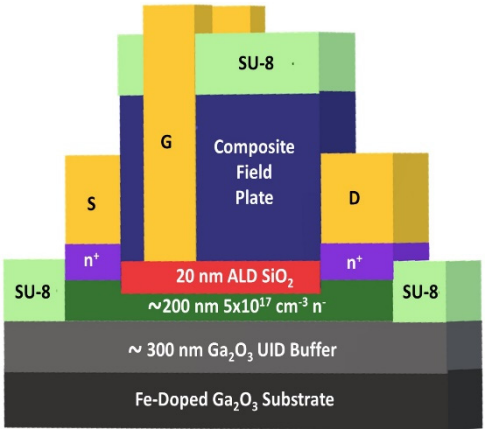

Fig. 1. Device Schematic.

In contrast to source/drain (S/D) regrowth process, the recess channel MOSFET process, where the n^{++} layers are selectively removed from channel region, in principle, offer less complexity hence more manufacturability. However, research has shown that reactive ion etching (RIE) reduces the charge carrier density in the channel access region [19, 23]. This has been attributed to the physical damage to the surface and subsequent creation of vacancies, traps and defects. This has an overall degrading effect on current carrying capacity and increases on-resistance although the breakdown is high [19]. RIE induced defects could also increase gate leakage current. Several methods have been explored to mitigate the RIE damage. Vacuum annealing has been demonstrated as an efficient mechanism to recover the lost current in MODFETs [22].

In this letter, we incorporate vacuum annealing to lateral field-plated recess channel Ga_2O_3 MOSFETs in both Molecular Beam Epitaxy (MBE) and MOCVD grown materials. We hypothesize that the RIE process leads to damage to the surface crystal structure which introduces trap states. Moreover, the stoichiometry of the surface layer could also be changed. These

This work was supported by the Air Force Office of Scientific Research (Program Manager: Ali Sayir) under Award FA9550-18-1-0479 and in part by NSF (Program Officer: Dr. Vikram Dalal) under Awards ECCS-2019749, ECCS-2019753 and in part by a sub-contract on NASA SBIR award (80NSSC21C0162, Program Officer: Dr. Max Yang, Prime: CFD Research Corporation).

Shivam Sharma, David Eason[1] and Uttam Singisetti are affiliated with the Department of Electrical Engineering, University at Buffalo, Buffalo, NY 14260 USA. (e-mail: uttamsin@buffalo.edu).

Lingyu Meng, A F M Anhar Uddin Bhuiyan, Zixuan Feng and Hongping Zhao are affiliated with the Department of Electrical and Computer Engineering, Ohio State University, Columbus, OH 43210 USA.

[1] Dr. David Eason passed away on 01/20/2022.

effects lead to a depletion of carriers. High temperature vacuum annealing process recovers these surface damages similar to the annealing of ion-implanted samples. High vacuum annealing is preferred to minimize the likelihood of oxidation of the ohmic metal stack. We demonstrate that vacuum annealing does not have any negative impact on breakdown characteristics of MOSFETs; at the same time increasing the on currents by more than an order. For MBE grown wafer, we report a L_{gd} = 60 µm device with record high V_{br} value of 8.56 kV, while at L_{gd} = 40 µm, we report a high breakdown of over 7 kV. Similar kV rating is also reported for MOCVD grown wafers. These values are the highest ever reported breakdown voltages for MBE and MOCVD grown β-Ga_2O_3 based lateral field-plated MOSFETs [4, 19]. For simplicity, we will explicitly mention/label samples as MBE or MOCVD.

II. Fabrication and Measurements

Device schematic of a fabricated MOSFET is shown in Fig. 1. Device structure and fabrication process are similar to our previous reports [18-20, 23]. For MBE sample, epitaxial layers were grown by Novel Crystal Technology (NCT), Inc., Japan, on 500 µm thick Fe-doped (010) Ga_2O_3 substrate. The 200 nm thick channel layer has Si dopant concentration of ~ 6.0 x 10^{17} cm^{-3} while the top 50 nm thick ohmic layer has targeted Si dopant concentration of ~ 2.2 x 10^{19} cm^{-3}. For MOCVD sample [24, 25], wafer structure is same except for Si doping in the channel is ~ 5 x 10^{17} cm^{-3}. The top-most ohmic layer is 50 nm thick with Si dopant density of ~ 1 x 10^{20} cm^{-3}. Epilayers for MOCVD sample were grown by MOCVD at 880 °C.

For both the samples, fabrication process was identical. Device fabrication started with the definition of 275 nm thick (100 nm Ti/ 100 nm Au/ 75 nm Ni) source/drain (S/D) pads. A 1-minute Rapid Thermal Annealing (RTA) at 470 °C was done in N_2 ambient to make the contacts ohmic. Device mesa isolation was done in a timed BCl_3/Ar RIE to achieve an etch depth of 625 nm. A second timed BCl_3/Ar self-aligned RIE was done to achieve channel thickness of 185 nm after removal of 50 nm of n^+ and 15 nm of n^- layers, which was verified by Atomic Force Microscopy (AFM). Devices were annealed at 600 °C under high vacuum (~ 1 x 10^{-8} Torr) for 1 hour for post-etch current recovery. An MBE chamber was used for vacuum annealing with liquid N_2 flowing in between the chamber walls. At the beginning of the anneal, the pressure was 3 × 10^{-9} Torr which increased to a maximum of 2 × 10^{-8} Torr as the temperature ramped-up to 600 °C. Temperature ramp-up rate was 30 °C/minute. Composite field-plate oxide deposition followed by trench etch and gate patterning was identical to our previous reports [18-20, 23]. This included a 1-minute RTA at 470°C to densify the FP oxide after trench etch and before gate patterning. Subsequent processing was done to improve the device isolation by further etching Ga_2O_3 substrate another 125 nm. SU-8 passivation concluded the device fabrication process [19, 26, 27]. The gate lengths, L_g, of all devices reported here are 2 µm.

DC input and output characterization of devices was done using HP 4155B Semiconductor Parameter Analyzer. Breakdown voltage measurements were done using Keysight B1505A Power Device Analyzer in conjunction with Keysight N1272A Device Capacitance Selector (can apply up to 3 kV of drain voltages). For V_{br} measurements greater than 3 kV, we used Keysight N1268A Ultra High Voltage Expander along with Keysight B1505A. All V_{br} measurements were done in Fluorinert FC-40 ambient to prevent air-arcing.

III. Results and Discussion

The S/D contacts show ohmic characteristics after RTA. For MBE sample after RTA, sheet resistance, R_{sh}, and contact resistance ρ_c, were calculated as 371 Ω/□ and 1.34 × 10^{-5} Ω-cm^2 respectively. However, after RIE of n^{++} layer, the contacts showed significant current degradation. After vacuum anneal, ohmic I-Vs for d = 10 µm TLM device for MBE sample showed the improvement in current to mA range from µA range as shown in Fig. 2 (a). Fig. 2 (b) shows the comparison of 4-probe resistance, R_{4p}, of TLM structures of MBE and previously reported [19] samples. It is clear that the vacuum annealed devices have more than one order of magnitude lower resistances as compared to [19]. Similar trend was observed for MOCVD sample. We noticed hardening of the ohmic metals after vacuum annealing which could possibly be due to alloying at 600 °C. It is noted that the high temperature annealing could have a negative impact on the contact resistance.

The measured R_{sh} and ρ_c after RIE and vacuum annealing were 1.12 x 10^4 Ω/□ and 6.06 x 10^{-4} Ω-cm^2 respectively for MBE sample. Similar trend was observed for MOCVD sample, with lower contact resistance (2.34 x 10^{-7} Ω-cm^2) that is attributed to higher doping in the n^{++} layer. Theoretically, assuming the mobility as 100 $cm^2V^{-1}s^{-1}$ and given the carrier concentration and the thickness of n^- layer as ~ 6.0 x 10^{17} cm^{-3} and 185 nm respectively, the calculated R_{sh} value comes out to be 5.63 x 10^3 Ω/□. For both samples, higher experimental v-

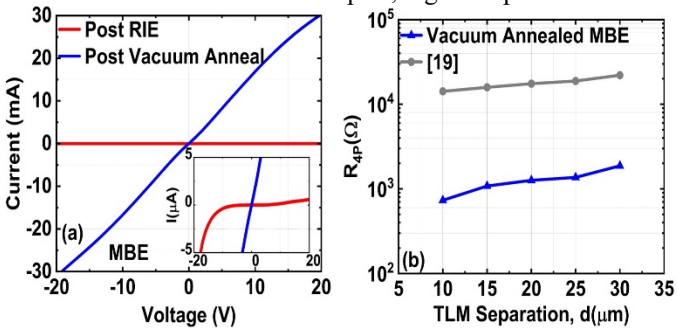

Fig. 2. (a) Effect of vacuum anneal on Ohmic I-Vs of MBE sample's TLM structure with separation, d =10 µm. Inset: non-linear µA range current after RIE. (b) Comparison of 4-Probe Resistance, R_{4p}, of TLMs of MBE and [19] samples.

-alues of R_{sh} as compared to theoretical values suggest an incomplete recovery of depleted carriers in the channel access region. Further anneal optimization (temperature-time) could improve the recovery. Having demonstrated the current recovery, we discuss the device results next.

Fig. 3. (a) shows the output characteristics of MBE sample with lower on-resistance (897 Ω·mm) compared to previous reports; both the on current density and on resistance improved by more than an order. Fig. 3 (b) shows the comparison between R_{on} values of vacuum annealed MBE sample with previous report [19] with L_{gd} ranging from 20 µm to 60 µm. It is evident that vacuum annealing is instrumental in lowering R_{on} by up to 10 times as compared to [19]. Figs. 3. (c) and 3. (d) show input and transconductance characteristics, respectively, of MBE L_{gd}

= 40 µm device. We report a good ON-OFF ratio of 10^9 with a threshold voltage, V_{th}, of –20 V.

Fig. 4. (a) shows DC output characteristics of an MOCVD device with L_{gd} = 40 µm. R_{on} of 1.04 kΩ·mm is about 10 times lower than [19]. Fig. 4. (b) shows that vacuum annealed MOSFETs of MOCVD wafer have up to an order of magnitu-de lower R_{on} as compared to [19]; spanning L_{gd} from 20 µm to 60 µm. This further demonstrates vacuum annealing as an efficient technique for post-RIE current recovery.

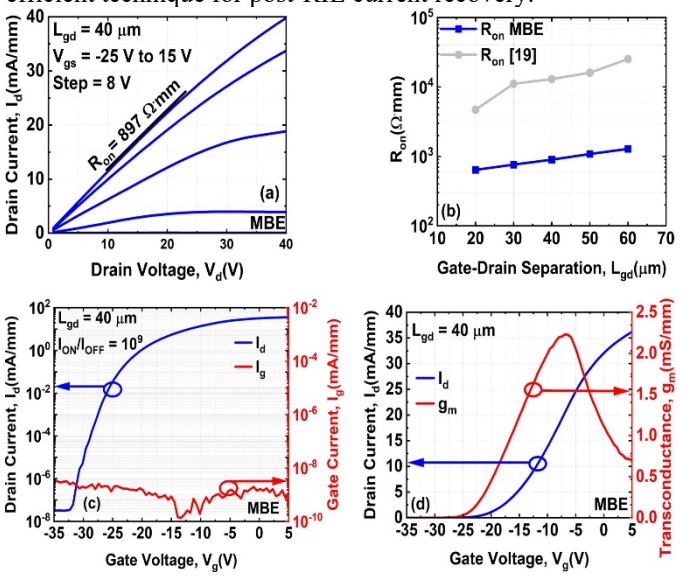

Fig. 3 (a) DC output characteristics. (b) Comparison of R_{on} between MBE sample and [19]. (c) DC input characteristics (log scale). (d) DC input characteristics with transconductance of L_{gd} = 40 µm device of MBE sample. L_g = 2 µm.

As seen in Figs. 3 (b) and 4 (b), both MBE and MOCVD samples show the effectiveness of vacuum annealing. However, the on-resistance is higher than recently reported MESFETs [4, 7] and other reports [21, 28]. This can be attributed to the partial recovery; a full recovery can reduce the resistance by about 46.5%. Additionally, the gate-source separation (5-8 µm) is higher than those reported in [4, 7].

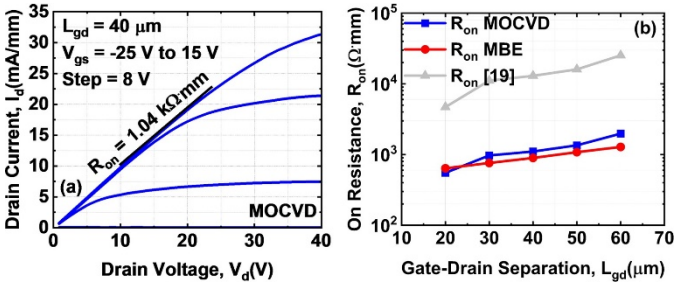

Fig. 4. (a) DC output characteristics of L_{gd} = 40 µm device of MOCVD sample. Fig. 4. (b) Comparison of R_{on} among MBE, MOCVD and [19] samples. L_g = 2 µm.

Breakdown voltage, V_{br}, plots of L_{gd} = 60 µm devices for both MBE and MOCVD samples, are shown in Fig. 5 (a). Also appended are V_{br} plots for MBE devices with 30 µm and 40 µm L_{gd}. After vacuum annealing, MBE and MOCVD devices with L_{gd} = 60 µm show breakdown values of 8.56 kV and 6.11 kV respectively with corresponding average field strengths, E_{br}, of 1.43 MVcm^{-1} and 1.02 MVcm^{-1}. V_{br} values are either higher or comparable with the reported V_{br} value of 6.81 kV for 60 µm device in [19]. We observe similar trend for L_{gd} = 40 µm device. Vacuum annealed MBE device gives a V_{br} of 7.16 kV (E_{br} = 1.78 MVcm^{-1}) which is comparable to 6.72 kV V_{br} reported in [19]. MOCVD L_{gd} = 60 µm device does not show a very sharp breakdown. Instead, current starts increasing at about 5.5 kV until a hard breakdown occurs at 6.11 kV. This soft breakdown characteristics could potentially be attributed to the interfacial conduction between epitaxial layer and substrate.

Fig. 5 (b) shows the trend of V_{br} values of vacuum annealed MBE and MOCVD devices in comparison with those of SU-8 passivated devices without vacuum annealing in [19]. The plot is suggestive that vacuum annealing does not negatively impact the V_{br} of devices. Across L_{gd}, ranging from 20 µm to 60 µm, we see that vacuum annealed devices have improved or comparable V_{br} against [19].

IV. Conclusion

In this letter, we studied the effect of vacuum annealing on lateral, field-plated β-Ga_2O_3 based MOSFETs fabricated on two differently grown wafers, one by MBE and the other by MOCVD. We report upto 10 times reduction in R_{on} as compared to previous report from our group. TLM analysis shows partial current recovery from RIE-induced carrier depletion. We also show that vacuum annealing is not detrimental to V_{br}. V_{br} of 8.56 kV is reported for L_{gd} = 60 µm device for MBE wafer. This is the highest V_{br} ever reported for MBE or MOCVD grown β-Ga_2O_3 based lateral field-plated MOSFETs. Regrowth of S/D contacts and further optimization of vacuum annealing can give better on currents and further reduce R_{on}.

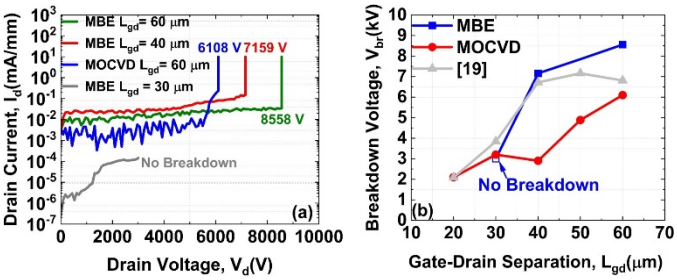

Fig. 5. (a) V_{br} Characteristics of MBE and MOCVD devices with L_{gd} = 60 µm. Also shown are V_{br} plots for MBE devices with L_{gd} of 30 µm (no breakdown) and 40 µm. L_{gd} = 30 µm device was measured using Keysight N1272A which has lower noise floor. Fig. 5 (b). Comparison among V_{br} values of vacuum annealed devices and [19].

REFERENCES

[1] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Gallium oxide (Ga2O3) metal-semiconductor

field-effect transistors on single-crystal β-Ga2O3 (010) substrates," *Applied Physics Letters,* vol. 100, no. 1, p. 013504, 2012, doi: 10.1063/1.3674287.

[2] M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Development of gallium oxide power devices," *physica status solidi (a),* vol. 211, no. 1, pp. 21-26, 2014.

[3] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Field-plated Ga 2 O 3 MOSFETs with a breakdown voltage of over 750 V," *IEEE Electron Device Letters,* vol. 37, no. 2, pp. 212-215, 2015.

[4] A. Bhattacharyya *et al.*, "4.4 kV β-Ga2O3 MESFETs with power figure of merit exceeding 100 MW cm− 2," *Applied Physics Express,* vol. 15, no. 6, p. 061001, 2022.

[5] K. Tetzner *et al.*, "Lateral 1.8 kV $\beta $-Ga 2 O 3 MOSFET With 155 MW/cm 2 Power Figure of Merit," *IEEE Electron Device Letters,* vol. 40, no. 9, pp. 1503-1506, 2019.

[6] Y. Lv *et al.*, "Lateral β-Ga2O3 MOSFETs With High Power Figure of Merit of 277 MW/cm2," *IEEE Electron Device Letters,* vol. 41, no. 4, pp. 537-540, 2020, doi: 10.1109/LED.2020.2974515.

[7] A. Bhattacharyya *et al.*, "Multi-kV Class <italic>β</italic>-Ga_2O_3 MESFETs With a Lateral Figure of Merit Up to 355 MW/cm^2," *IEEE Electron Device Letters,* vol. 42, no. 9, pp. 1272-1275, 2021, doi: 10.1109/LED.2021.3100802.

[8] Y. Lv *et al.*, "Source-Field-Plated $\beta $-Ga 2 O 3 MOSFET With Record Power Figure of Merit of 50.4 MW/cm 2," *IEEE Electron Device Letters,* vol. 40, no. 1, pp. 83-86, 2018.

[9] P. Dong *et al.*, "6 kV/3.4 mΩ·cm<sup>2</sup > Vertical β-Ga2O;3 Schottky Barrier Diode With BV2;/Ron,sp Performance Exceeding 1-D Unipolar Limit of GaN and SiC," *IEEE Electron Device Letters,* vol. 43, no. 5, pp. 765-768, 2022, doi: 10.1109/LED.2022.3160366.

[10] K. Konishi *et al.*, "1-kV vertical Ga2O3 field-plated Schottky barrier diodes," *Applied Physics Letters,* vol. 110, no. 10, p. 103506, 2017, doi: 10.1063/1.4977857.

[11] W. Li *et al.*, "2.44 kV Ga2O3 vertical trench Schottky barrier diodes with very low reverse leakage current," in *2018 IEEE International Electron Devices Meeting (IEDM)*, 1-5 Dec. 2018 2018, pp. 8.5.1-8.5.4, doi: 10.1109/IEDM.2018.8614693.

[12] W. Li *et al.*, "1230 V β-Ga2O3 trench Schottky barrier diodes with an ultra-low leakage current of <1 μA/cm2," *Applied Physics Letters,* vol. 113, no. 20, p. 202101, 2018, doi: 10.1063/1.5052368.

[13] W. Li *et al.*, "1.5 kV Vertical Ga2O3 Trench-MIS Schottky Barrier Diodes," in *2018 76th Device Research Conference (DRC)*, 24-27 June 2018 2018, pp. 1-2, doi: 10.1109/DRC.2018.8442245.

[14] S. Roy, A. Bhattacharyya, P. Ranga, H. Splawn, J. Leach, and S. Krishnamoorthy, "High-k Oxide Field-Plated Vertical (001) β-Ga₂O₃ Schottky Barrier Diode With Baliga's Figure of Merit Over 1 GW/cm²," *IEEE Electron Device Letters,* vol. 42, no. 8, pp. 1140-1143, 2021, doi: 10.1109/LED.2021.3089945.

[15] J. Yang, F. Ren, M. Tadjer, S. J. Pearton, and A. Kuramata, "2.3 kV Field-Plated Vertical Ga2O3 Schottky Rectifiers and 1 a Forward Current with 650 V Reverse Breakdown Ga2O3 Field-Plated Schottky Barrier Diodes," in *2018 76th Device Research Conference (DRC)*, 24-27 June 2018 2018, pp. 1-2, doi: 10.1109/DRC.2018.8442188.

[16] Z. Hu *et al.*, "Enhancement-Mode Ga2O3 Vertical Transistors With Breakdown Voltage >1 kV," *IEEE Electron Device Letters,* vol. 39, no. 6, pp. 869-872, 2018, doi: 10.1109/LED.2018.2830184.

[17] J. K. Mun, K. Cho, W. Chang, H.-W. Jung, and J. Do, "Editors' Choice—2.32 kV Breakdown Voltage Lateral β-Ga2O3 MOSFETs with Source-Connected Field Plate," *ECS Journal of Solid State Science and Technology,* vol. 8, no. 7, pp. Q3079-Q3082, 2019. [Online]. Available: http://jss.ecsdl.org/content/8/7/Q3079.abstract.

[18] K. Zeng, A. Vaidya, and U. Singisetti, "1.85 kV Breakdown Voltage in Lateral Field-Plated Ga2O3 MOSFETs," *IEEE Electron Device Letters,* vol. 39, no. 9, pp. 1385-1388, 2018, doi: 10.1109/LED.2018.2859049.

[19] S. Sharma, K. Zeng, S. Saha, and U. Singisetti, "Field-Plated Lateral Ga 2 O 3 MOSFETs With Polymer Passivation and 8.03 kV Breakdown Voltage," *IEEE Electron Device Letters,* vol. 41, no. 6, pp. 836-839, 2020.

[20] K. Zeng, A. Vaidya, and U. Singisetti, "A field-plated Ga2O3 MOSFET with near 2-kV breakdown voltage and 520 mΩ · cm2 on-resistance," *Applied Physics Express,* vol. 12, no. 8, p. 081003, 2019/07/12 2019, doi: 10.7567/1882-0786/ab2e86.

[21] Y. Lv *et al.*, "Lateral source field-plated β-Ga2O3 MOSFET with recorded breakdown voltage of 2360 v and low specific on-resistance of 560 mΩ cm2," *Semiconductor Science and Technology,* vol. 34, no. 11, p. 11LT02, 2019.

[22] C. Joishi *et al.*, "Breakdown Characteristics of β -(Al0.22Ga0.78)2O3/Ga2O3 Field-Plated Modulation-Doped Field-Effect Transistors," *IEEE Electron Device Letters,* vol. 40, no. 8, pp. 1241-1244, 2019, doi: 10.1109/LED.2019.2921116.

[23] K. Zeng, A. Vaidya, and U. Singisetti, "710 V Breakdown Voltage in Field Plated Ga203 MOSFET," in *2018 76th Device Research Conference (DRC)*, 24-27 June 2018 2018, pp. 1-2, doi: 10.1109/DRC.2018.8442222.

[24] Z. Feng, A. Anhar Uddin Bhuiyan, M. R. Karim, and H. Zhao, "MOCVD homoepitaxy of Si-doped (010) β-Ga2O3 thin films with superior transport properties," *Applied Physics Letters,* vol. 114, no. 25, p. 250601, 2019.

[25] Z. Feng *et al.*, "Probing Charge Transport and Background Doping in Metal-Organic Chemical Vapor Deposition-Grown (010) β-Ga2O3," *physica status solidi (RRL)–Rapid Research Letters,* vol. 14, no. 8, p. 2000145, 2020.

[26] A. Olziersky *et al.*, "Insight on the SU-8 resist as passivation layer for transparent Ga2O3–In2O3–ZnO thin-film transistors," *Journal of Applied Physics,* vol. 108, no. 6, p. 064505, 2010, doi: 10.1063/1.3477192.

[27] J. Melai, C. Salm, S. Smits, J. Visschers, and J. Schmitz, "The electrical conduction and dielectric strength of SU-8," *Journal of Micromechanics and Microengineering,* vol. 19, no. 6, p. 065012, 2009/05/20 2009, doi: 10.1088/0960-1317/19/6/065012.

[28] A. Bhattacharyya *et al.*, "130 mA mm− 1 β-Ga2O3 metal semiconductor field effect transistor with low-temperature metalorganic vapor phase epitaxy-regrown ohmic contacts," *Applied Physics Express,* vol. 14, no. 7, p. 076502, 2021.