Applied Physics Express

LETTER

4.4 kV β-Ga_2O_3 MESFETs with power figure of merit exceeding 100 MW cm^{-2}

To cite this article: Arkka Bhattacharyya *et al* 2022 *Appl. Phys. Express* **15** 061001

Applied Physics Express 15, 061001 (2022) LETTER
https://doi.org/10.35848/1882-0786/ac6729

4.4 kV β-Ga_2O_3 MESFETs with power figure of merit exceeding 100 MW cm^{-2}

Arkka Bhattacharyya[1*], Shivam Sharma[2], Fikadu Alema[3], Praneeth Ranga[1], Saurav Roy[4], Carl Peterson[4], Geroge Seryogin[3], Andrei Osinsky[3], Uttam Singisetti[2], and Sriram Krishnamoorthy[4*]

[1]Department of Electrical and Computer Engineering, University of Utah, Salt Lake City Utah 84112 United States of America
[2]Electrical Engineering Department, University at Buffalo, Buffalo, NY 14260 United States of America
[3]Agnitron Technology Incorporated, Chanhassen, Minnesota 55317, United States of America
[4]Materials Department, University of California, Santa Barbara, California 93106, United States of America

*E-mail: a.bhattacharyya@utah.edu; sriramkrishnamoorthy@ucsb.edu

Received February 10, 2022; revised April 9, 2022; accepted April 12, 2022; published online May 16, 2022

β-Ga_2O_3 metal–semiconductor field-effect transistors are realized with superior reverse breakdown voltages (V_{BR}) and ON currents (I_{DMAX}). A sandwiched SiN_x dielectric field plate design is utilized that prevents etching-related damage in the active region and a deep mesa-etching was used to reduce reverse leakage. The device with $L_{GD} = 34.5$ μm exhibits an I_{DMAX} of 56 mA mm^{-1}, a high I_{ON}/I_{OFF} ratio $>10^8$ and a very low reverse leakage until catastrophic breakdown at ~4.4 kV. A power figure of merit (PFOM) of 132 MW cm^{-2} was calculated for a V_{BR} of ~4.4 kV. The reported results are the first >4 kV class Ga_2O_3 transistors to surpass the theoretical unipolar FOM of silicon.

β-Ga_2O_3, a unipolar ultra-wide bandgap (UWBG) semiconductor ($E_g = 4.6$–4.9 eV), has gained increasing importance as a material with tremendous promise to enable power-efficient next generation high voltage power devices. In the last decade of research, β-Ga_2O_3 material system has witnessed several milestones in bulk and epitaxial single crystal growth, doping, device design, and processing.[1–11] β-Ga_2O_3-based devices with breakdown voltage up to 8 kV and critical breakdown fields exceeding the theoretical limits of SiC and GaN have been demonstrated.[7,12,13] While substantial progress has been made in β-Ga_2O_3 devices, understanding of its material and device performance to take full advantage of its intrinsic properties is still far from mature.

Several field management techniques have been demonstrated in β-Ga_2O_3 devices to enhance the average breakdown fields and blocking voltages—the most popular technique being the field-plate (FP) design. But most of these devices suffer from either high reverse leakage that leads to a premature breakdown or low ON currents (and high R_{ON}) due to the non-ideal FP process flow involving etching in the gate region.[7,8] In this letter, we demonstrate over 4 kV class all-metalorganic vapor phase epitaxy (MOVPE)-grown β-Ga_2O_3 lateral metal–semiconductor field-effect transistor (MESFETs) with a gate FP design using SiN_x FP/passivation dielectric that achieves high ON currents, low reverse leakage, and power figure of merit (PFOM) exceeding 100 MW cm^{-2}, simultaneously. We address the critical metrics of V_{BR} (breakdown voltage), $R_{on,sp}$ (specific on-resistance), and ON current (I_{DMAX}) at the same time—with significant improvement over the state-of-the-art reports.[7,8,12,14,15]

Growth of β-Ga_2O_3 channel (230 nm thick Si-doped ~ 3.6×10^{17} cm^{-3}) on an Fe-doped (010) bulk substrate was performed by using Agnitron Technology's Agilis 700 MOVPE reactor with TEGa, O_2, and silane (SiH_4) as precursors and argon as carrier gas. The 10 × 15 mm^2 (010) bulk substrate (Novel Crystal Technology, Japan) was cleaned using hydrofluoric acid (HF) for 30 min prior to epilayer growth. SF_6/Ar inductively coupled plasma-reactive ion (ICP-RIE) dry etching was utilized for mesa and contact region recessing. The mesa etching was intentionally extended deeper into the substrate, and the total mesa etch height was measured to be ~500 nm. The device mesa isolation and the source/drain MOVPE-regrown ohmic contacts fabrication details can be found elsewhere.[16–20] Ti/Au/Ni (20 nm/100 nm/30 nm) was evaporated on the regrown n^+ contact regions followed by a 450 °C anneal in N_2 for 1.5 min. For the Schottky gate, Ni/Au/Ni (30 nm/100 nm/30 nm) metal stack was evaporated to complete the MESFET structure.

The gate FP design involved a sandwiched dielectric structure as shown in Fig. 1. A 170 nm thick SiN_x film was sandwiched between the gate metal and the FP metal [evaporated Ti (10 nm)/Au (150 nm)/Ni (50 nm)] using sequential metal evaporation and plasma-enhanced chemical vapor deposition (PECVD) SiN_x deposition steps. The FP metal was shorted to the gate pad placed away from the device mesa (in the third dimension shown in Fig. 1). This FP design avoids dry etching plasma-related damage in the active region. The device dimensions were later verified by top-view SEM imaging and the FP extensions (L_{FP}) were 3.2 and 3.5 μm for devices with gate-to-drain length (L_{GD}) of 34.5 and 44.5 μm, respectively. All the devices had a fixed L_{GS} ~1 μm and L_G ~2.4 μm. The device mesa was fully passivated using a (50 nm) SiN_x/(50 nm) SiO_2 bilayer passivation.

From Hall measurement, the channel charge and mobility were measured to be 5.7×10^{12} cm^{-2} and 95 cm^2 V^{-1} s^{-1} respectively ($R_{sh,ch} = 11.7$ kΩ/□). From transfer length measurements (TLM), the channel $R_{sh,ch}$ was 11.5 kΩ/□ and the total contact resistance to the channel was $R_C = 1.4$ Ω.mm. The metal to regrown contact layer (R_{sh,n^+} ~130 Ω/□) specific contact resistance was of the order ~10^{-6} Ω cm^2. Figures 2(a) and 2(b) show the DC output and transfer curves for a MESFET with dimensions $L_{GS}/L_G/L_{GD} = 1.0/2.4/34.5$ μm, measured using Keithley 4200 SCS. The maximum ON current (I_{DMAX}) and ON-resistance (R_{ON}) measured were ~56 mA mm^{-1} and 385 Ω.mm at a gate bias (V_{GS}) of 2 V as shown in Fig. 2(a). The contact resistance to the channel, R_C, was a negligible part of the total device R_{ON}. The devices show sharp pinch-off at a $V_{GS} = -13$ V and low reverse leakage ($I_{ON}/I_{OFF} > 10^8$ and negligible gate leakage). A maximum transconductance and sub-threshold swing of 6.2 mS mm^{-1} and 186 mV dec^{-1} was extracted respectively. The low gate and source-drain leakage indicated minimal surface and bulk-related leakage in these devices.

The breakdown measurements were performed with the wafer submerged in FC-40 Fluorinert dielectric liquid using a

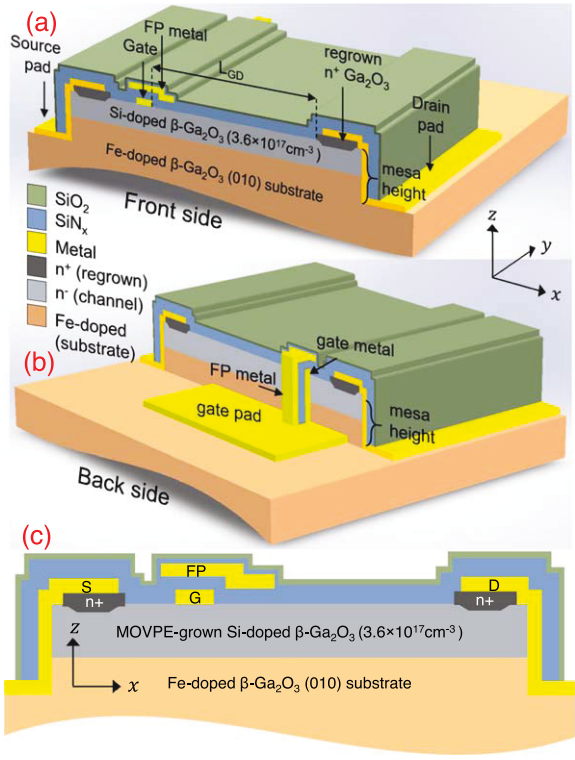

Fig. 1. (Color online) (a) 3D cross-section schematic of the β-Ga_2O_3 MESFET showing the FP design. (b) Gate FP metal is electrically connected to the gate pad outside the mesa (inset: coordinate planes/axes) and (c) 2D cross-section schematic of the device along the x–z plane.

Keysight B1505 power device analyzer with N1268A ultra-high voltage (UHV) expander. Figure 3(a) shows the three-terminal breakdown characteristics (at $V_{GS} = -20$ V) of the MESFET device with L_{GD} of 34.5 μm. A breakdown voltage V_{BR} ($= V_{DS} - V_{GS}$) of 4415 V was measured. The device with L_{GD} of 44.5 μm exhibited a V_{BR} of 4567 V (not shown). All the devices exhibited very low leakage of 10–100 nA mm^{-1} until catastrophic breakdown was observed. The measured reverse leakage currents in Fig. 3(a) was limited by the noise floor of the N1268A UHV measurement set-up. Minimizing the reverse leakage was key to achieving the high V_{BR} values and improved L_{GD}–V_{BR} linearity. Firstly, the long HF substrate cleaning before the epilayer growth helped in suppressing the parasitic channel at the epilayer/substrate interface that is believed to come from residual Si impurities from the substrate polishing or ambient exposure. As shown from capacitance–voltage (C–V) measurements in Fig. 3(b), the channel charge profile showed sharp decay near the substrate, indicating the absence of any active parasitic channel. A backside depletion of the channel ~50 nm from the substrate was observed which is consistent with the E_f pinning at the Fe trap level ($E_C - E_{Fe} \sim 0.8$ eV) in the substrate.[21] We hypothesize that the deeper mesa etching was important to eliminate any fringing leakage paths around the device mesa. The low reverse leakage and identical pinch-off voltage values from CV and FET transfer characteristics indicate that these two design steps were very effective in suppressing parasitic channel/charge conduction.

Figure 4(a) shows the variation of V_{BR} and I_{DMAX} as a function of L_{GD}. The breakdown voltage values exhibit a very linear increase up to $L_{GD} = 10$ μm (V_{BR} ~2.5 kV) and the devices were able to exhibit 2.5 MV cm^{-1} average breakdown field (V_{BR}/L_{GD}). Beyond L_{GD} of 10 μm, the breakdown voltage starts to enter a saturation region and the V_{BR} saturates at around ~4.5 kV and does not increase much from L_{GD} of 34.5–44.5 μm. From Sentaurus TCAD simulations, it was estimated that all the devices with $L_{GD} \leqslant 10$ μm had a punch-through (PT) field profile i.e. electric field does not go to zero at the drain contact, at their respective breakdown voltages whereas devices with $L_{GD} > 10$ μm had non-punchthrough (NPT) field profile at breakdown. Figures 4(c), 4(d) and Figs. 4(e), 4(f) shows the 2D E-field contour and profiles for the PT ($L_{GD} = 10$ μm) and NPT ($L_{GD} = 34.5$ μm) devices at their respective breakdown voltages. It can also be seen that the NPT devices ($L_{GD} > 10$ μm) show larger device-to-device variation in V_{BR} compared to the PT devices ($L_{GD} \leqslant 10$ μm). Figure 4(b) shows the variation of I_{DMAX} with L_{GD} and shows almost a linear change. It is to be noticed that I_{DMAX} values show very little device-to-device variation unlike the V_{BR} values. This observation indicates that apart from the spatial variation of bulk-related leakage paths, the device fabrication process variation over the 10×15 mm^2 sample could also lead to the spread in the V_{BR} values. The low device-to-device variation in ON currents also indicate that the epi-film

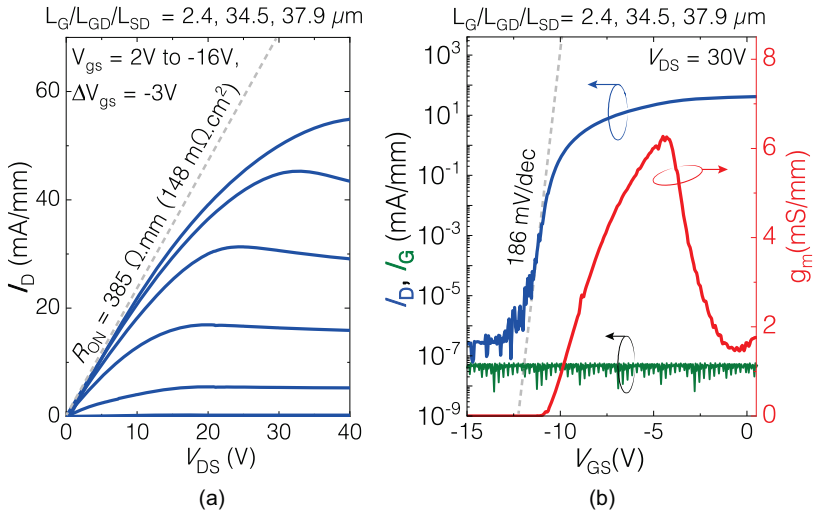

Fig. 2. (Color online) (a) Output and (b) transfer curves for the β-Ga_2O_3 MESFETs with $L_{GD} = 34.5$ μm.

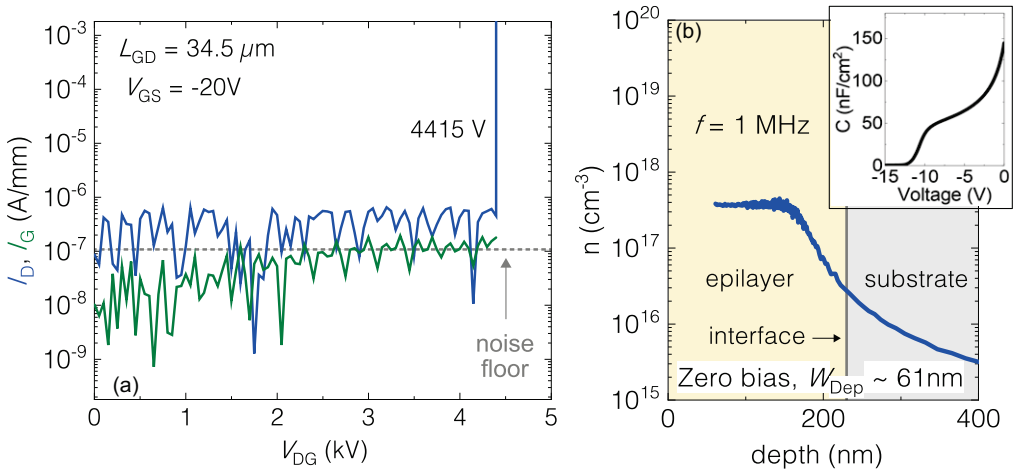

Fig. 3. (Color online) (a) Three-terminal OFF-state reverse breakdown characteristics of the β-Ga_2O_3 MESFET with $L_{GD} = 34.5$ μm. (b) Channel charge profile extracted from C–V measurements (inset: capacitance–voltage profile).

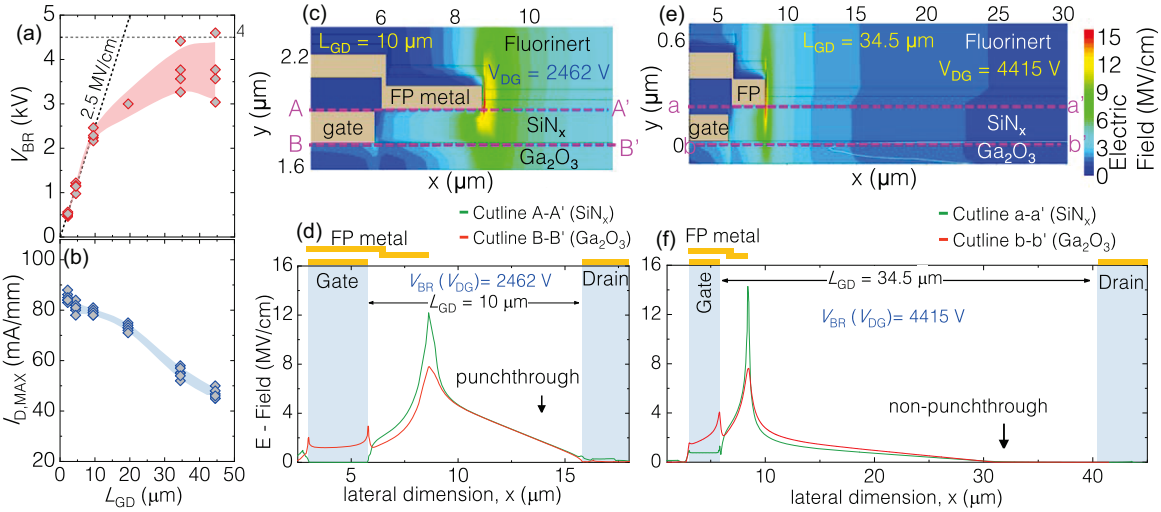

Fig. 4. (Color online): (a) V_{BR} and (b) I_{DMAX} measured in our β-Ga_2O_3 MESFETs as a function of L_{GD} (shaded region shows device-to-device variation and is a guide to the eye). Simulated 2D E-field contour and E-field profile in SiN_x and Ga_2O_3 for (c), (d) device with $L_{GD} = 10$ μm at the experimental V_{BR} (V_{DG}) = 2462 V and (e), (f) device with $L_{GD} = 34.5$ μm at the experimental V_{BR} (V_{DG}) = 4415 V.

conductivity (charge and mobility) is fairly uniform. From Sentaurus TCAD simulations [as shown in Figs. 4(d) and 4(f)], it was seen that the peak field was found at the FP edge in the SiN_x layer and, hence, dielectric leakage/breakdown could also be limiting the V_{BR} and causing the saturation in V_{BR}. For higher V_{BR} values, dielectrics with higher $\epsilon.E_{CR}$ values will be necessary to attain PT to hold higher E-fields (where ϵ is relative DC dielectric permittivity and E_{CR} is the critical breakdown electric field of the dielectric material).

The power figures of merit (PFOM) ($V^2_{BR}/R_{on,sp}$) of these devices were estimated, where $R_{on,sp}$ is R_{ON} normalized to the device active region ($L_{SD} + 2L_T$). L_T corresponds to the transfer length of the whole ohmic contact (metal to channel) including the regrown layer resistance ($2L_T = 0.6$ μm) extracted from patterned TLM patterns on the same wafer. A PFOM of 132 MW cm^{-2} was estimated for the device with $L_{GD} = 34.5$ μm ($V_{BR} = 4.4$ kV, $R_{on,sp} = 148$ m Ω cm^2 and $L_{SD} = 37.9$ um). The device with $L_{GD} = 44.5$ μm exhibited a maximum PFOM of 96 MW cm^{-2} ($V_{BR} = 4.57$ kV, $R_{on,sp} = 219$ mΩ cm^2 and $L_{SD} = 47.9$ μm). These PFOM values are benchmarked with the existing literature reports on β-Ga_2O_3 lateral FETs in Fig. 5. It can be seen that the devices reported here are the first >4 kV class β-Ga_2O_3 FET devices to surpass the theoretical unipolar FOM of silicon. Furthermore, our reported $R_{on,sp}$ are the lowest for any β-Ga_2O_3 FET exceeding a breakdown voltage of 4 kV. The V_{BR}–L_{GD} linearity is expected to be further improved by eliminating any parasitic bulk/surface leakage paths and passivation including extreme permittivity materials.[29] The V_{BR}–$R_{on,sp}$ trade-off can be further improved by utilizing accumulation channels, improved channel/buffer stack engineering to improve channel mobility in conjunction with minimizing reverse leakage to prevent premature breakdown.

In summary, we demonstrate a 4.4 kV class β-Ga_2O_3 lateral MESFET with a PFOM of 132 MW cm^{-2} and ON current of 56 mA mm^{-1}—the first >4 kV class β-Ga_2O_3 transistor to surpass theoretical UFOM of silicon. The devices exhibit very low leakage of 10–100 nA mm^{-1} until catastrophic breakdown occurs. The reported devices show the highest I_{DMAX} and lowest R_{ON} values simultaneously for any β-Ga_2O_3 device with $V_{BR} > 4$ kV to date. This work highlights that high breakdown voltages (V_{BR}), high PFOM and high ON currents can be achieved simultaneously in β-Ga_2O_3 lateral transistors

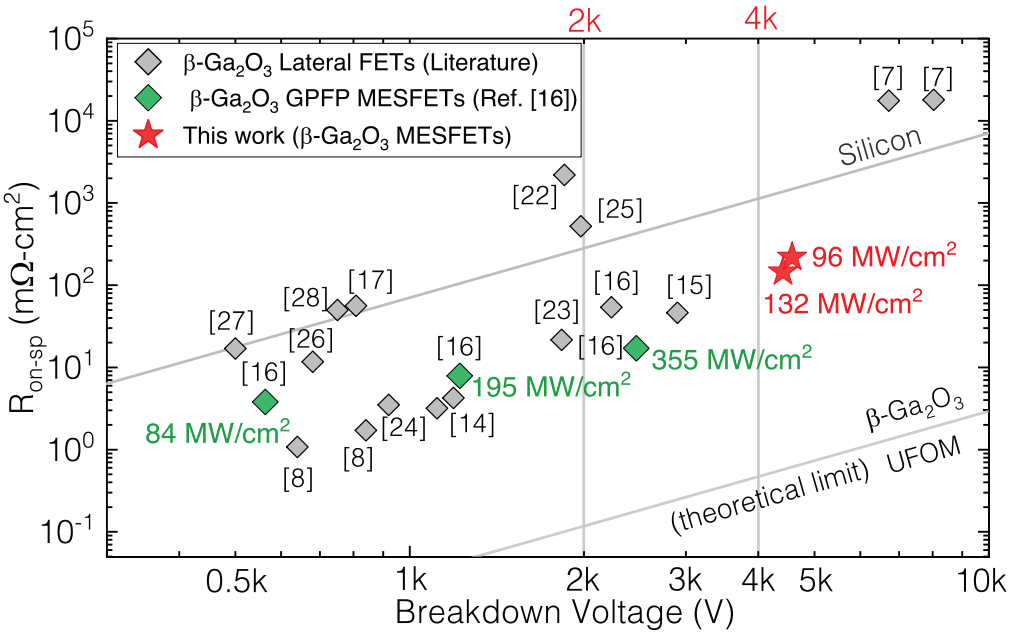

Fig. 5. (Color online) Differential $R_{on,sp}$–V_{BR} benchmark plot of our β-Ga_2O_3 MESFET with the literature reports.[7,8,14–16,22–28] Green data points correspond to PFOM values from Ref. 16.

—showing great promise for MOVPE-grown β-Ga_2O_3 FETs in the low to medium voltage power-device applications.

Acknowledgments This material is based upon work supported by the II–VI foundation Block Gift Program 2020–2022 and the DoD SBIR Phase I—AF203-CS01 (Contract No: FA864921P0304). Work at UB was supported by AFOSR grant FA9550-18-1-0479 (Monitor: Dr. Ali Sayir), NSF ECCS 2019749. This work was performed in part at the Utah Nanofab sponsored by the College of Engineering, Office of the Vice President for Research, and the Utah Science Technology and Research (USTAR) initiative of the State of Utah. The author(s) appreciate the support of the staff and facilities that made this work possible. A. B. extends special thanks to Wei Jia for assistance in preparing the figures used in this work.

ORCID iDs Arkka Bhattacharyya https://orcid.org/0000-0002-7209-5681 Praneeth Ranga https://orcid.org/0000-0001-9002-1523 Sriram Krishnamoorthy https://orcid.org/0000-0002-4682-1002

1) M. Higashiwaki and G. H. Jessen, Appl. Phys. Lett. **112**, 060401 (2018).
2) G. Seryogin, F. Alema, N. Valente, H. Fu, E. Steinbrunner, A. T. Neal, S. Mou, A. Fine, and A. Osinsky, Appl. Phys. Lett. **117**, 262101 (2020).
3) M. Saleh, A. Bhattacharyya, J. B. Varley, S. Swain, J. Jesenovec, S. Krishnamoorthy, and K. Lynn, Appl. Phys. Express **12**, 085502 (2019).
4) J. Jesenovec, B. L. Dutton, N. Stone-Weiss, A. Chmielewski, M. Saleh, C. Peterson, N. Alem, S. Krishnamoorthy, and J. S. McCloy, J. Appl. Phys. **131**, 155702 (2022).
5) K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, J. Cryst. Growth **378**, 591 (2013).
6) Y. Song et al., ACS Appl. Mater. Interfaces **13**, 40817 (2021).
7) S. Sharma, K. Zeng, S. Saha, and U. Singisetti, IEEE Electron Device Lett. **41**, 836 (2020).
8) N. K. Kalarickal, Z. Xia, H.-L. Huang, W. Moore, Y. Liu, M. Brenner, J. Hwang, and S. Rajan, IEEE Electron Device Lett. **42**, 899 (2021).
9) P. Ranga, A. Bhattacharyya, L. Whittaker-Brooks, M. A. Scarpulla, and S. Krishnamoorthy, J. Vac. Sci. Technol. A **39**, 030404 (2021).
10) P. Ranga, A. Rishinaramangalam, J. Varley, A. Bhattacharyya, D. Feezell, and S. Krishnamoorthy, Appl. Phys. Express **12**, 111004 (2019).
11) S. Roy, A. E. Chmielewski, A. Bhattacharyya, P. Ranga, R. Sun, M. A. Scarpulla, N. Alem, and S. Krishnamoorthy, Adv. Electron. Mater. **7**, 2100333 (2021).
12) A. J. Green et al., IEEE Electron Device Lett. **37**, 902 (2016).
13) S. Roy, A. Bhattacharyya, P. Ranga, H. Splawn, J. Leach, and S. Krishnamoorthy, IEEE Electron Device Lett. **42**, 1140 (2021).
14) C. Wang et al., IEEE Electron Device Lett. **42**, 485 (2021).
15) Y. Lv et al., IEEE Electron Device Lett. **41**, 537 (2020).
16) A. Bhattacharyya, P. Ranga, S. Roy, C. Peterson, F. Alema, G. Seryogin, A. Osinsky, and S. Krishnamoorthy, IEEE Electron Device Lett. **42**, 1272 (2021).
17) A. Bhattacharyya, S. Roy, P. Ranga, D. Shoemaker, Y. Song, J. S. Lundh, S. Choi, and S. Krishnamoorthy, Appl. Phys. Express **14**, 076502 (2021).
18) A. Bhattacharyya, P. Ranga, S. Roy, J. Ogle, L. Whittaker-Brooks, and S. Krishnamoorthy, Appl. Phys. Lett. **117**, 142102 (2020).
19) P. Ranga, A. Bhattacharyya, A. Chmielewski, S. Roy, N. Alem, and S. Krishnamoorthy, Appl. Phys. Lett. **117**, 172105 (2020).
20) P. Ranga, A. Bhattacharyya, A. Chmielewski, S. Roy, R. Sun, M. A. Scarpulla, N. Alem, and S. Krishnamoorthy, Appl. Phys. Express **14**, 025501 (2021).
21) A. T. Neal et al., Appl. Phys. Lett. **113**, 062101 (2018).
22) K. Zeng, A. Vaidya, and U. Singisetti, IEEE Electron Device Lett. **39**, 1385 (2018).
23) K. Tetzner, E. B. Treidel, O. Hilt, A. Popp, S. B. Anooz, G. Wagner, A. Thies, K. Ickert, H. Gargouri, and J. Würfl, IEEE Electron Device Lett. **40**, 1503 (2019).
24) N. K. Kalarickal, Z. Feng, A. A. U. Bhuiyan, Z. Xia, W. Moore, J. F. McGlone, A. R. Arehart, S. A. Ringel, H. Zhao, and S. Rajan, IEEE Trans. Electron Devices **68**, 29 (2020).
25) K. Zeng, A. Vaidya, and U. Singisetti, Appl. Phys. Express **12**, 081003 (2019).
26) Y. Lv et al., IEEE Electron Device Lett. **40**, 83 (2018).
27) K. D. Chabak et al., IEEE Electron Device Lett. **39**, 67 (2017).
28) M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, IEEE Electron Device Lett. **37**, 212 (2015).
29) M. W. Rahman, N. K. Kalarickal, H. Lee, T. Razzak, and S. Rajan, Appl. Phys. Lett. **119**, 193501 (2021).