Power-Efficient LFP-Adaptive Dynamic Zoom-and-Track Incremental ΔΣ Front-End for Dual-Band Subcortical Recordings

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***Abstract*—We report a power-efficient analog front-end integrated circuit (IC) for multi-channel, dual-band subcortical recordings. In order to achieve high-resolution multi-channel recordings with low power consumption, we implemented an incremental ΔΣ ADC (IADC) with a dynamic zoom-and-track scheme. This scheme continuously tracks local field potential (LFP) and adaptively adjusts the input dynamic range (DR) into a zoomed sub-LFP range to resolve tiny action potentials. Thanks to the reduced DR, the oversampling rate of the IADC can be reduced by 64.3% compared to the conventional approach, leading to significant power reduction. In addition, dual-band recording can be easily attained because the scheme continuously tracks LFPs without additional on-chip hardware. A prototype four-channel front-end IC has been fabricated in 180 nm standard CMOS processes. The IADC achieved 11.3-bit ENOB at 6.8 μW, resulting in the best Walden and SNDR FoMs, 107.9 fJ/c-s and 162.1 dB, respectively, among two different comparison groups: the IADCs reported up to date in the state-of-the-art neural recording front-ends; and the recent brain recording ADCs using similar zooming or tracking techniques to this work. The intrinsic dual-band recording feature reduces the post-processing FPGA resources for subcortical signal band separation by >45.8%. The front-end IC with the zoom-and-track IADC showed an NEF of 5.9 with input-referred noise of 8.2 μV_{rms}, sufficient for subcortical recording. The performance of the whole front-end IC was successfully validated through *in vivo* animal experiments.**

***Index Terms* — Dual-band recording, Dynamic zoom-and-track scheme, Incremental delta-sigma ADC, Power-efficient ADC, Neural recording front-end**

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I. Introduction

Neural activities from individual neurons and their ensembles control the brain functions [1]. In order to understand how the brain works, it is necessary to monitor the individual neural activities with high spatiotemporal resolution in subcortical regions of a behaving animal and correlate those with slow brain oscillations [2], [3]. Subcortical recording front-end integrated circuits (ICs) have been developed to meet this demand [4]-[7]. Typically, the front-end circuit is composed with low-noise amplifiers (LNAs) followed by analog-to-digital converters (ADCs) and digital wireline or wireless telemetry [8], [9]. The ADC is one of the most essential building blocks for construction of the front-end circuit because the acquired brain signals should be digitized for robust data transmission and post analysis [9], [10]. Therefore, it is important to choose an optimal architecture of ADCs for the energy-efficient recording front-end circuit.

For high-performance subcortical recording, ADCs should satisfy a couple of requirements as shown in Fig. 1. First, the resolution of ADCs should be sufficiently high to resolve tiny action potentials (APs), often as small as 10 μV, mixed with mV-scale local field potentials (LFPs) [11], [12]. Considering this magnitude range of subcortical signals as well as the circuit noise floor that must be lower than the smallest input, it is desired to use an ADC with 10 bit or higher effective number of bits (ENOB). Here, the electrode DC offset (EDO), that is much larger than neural signals, is ignored because it can be easily removed by the AC-coupled front-end architecture with a DC-cutoff frequency of ~0.1 Hz [46]. Second, the ADC integrated in the multi-channel recording front-end should accommodate time-division multiplexed (TDM) inputs for optimized power and area efficiencies [13]-[15].

Conventionally, Nyquist-rate ADCs, such as successive-approximation-register (SAR) ADCs, were widely used for multi-channel neural recording front-ends. The SAR ADCs consume low power and easily accommodate multiplexed inputs through sampling operation. However, the Nyquist ADCs are susceptible to performance degradation due to process variations, requiring additional circuits for compensation. For instance, the accuracy of high-resolution SAR ADCs typically depends on complex calibration techniques to alleviate distortions caused by mismatches and/or

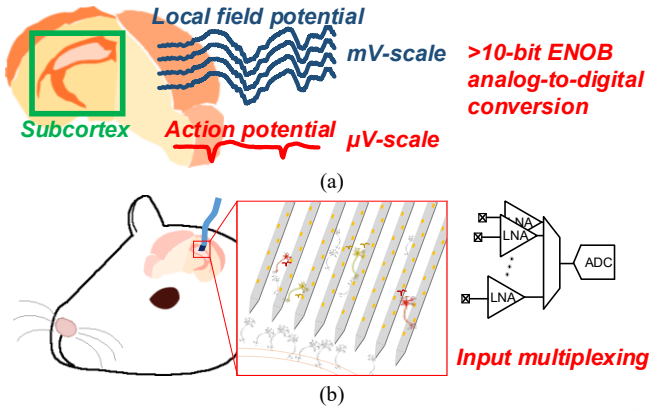


Fig. 1. ADC requirements for a high-performance subcortical recording front-end: (a) high effective resolution (>10bit ENOB), (b) capability of multiplexed inputs for high-channel count recording.

incomplete settling in capacitor digital-to-analog converters (CDACs) [16], [17]. Alternative option is an oversampled ADC. Delta-sigma (ΔΣ) ADCs can achieve a high resolution through in-band quantization noise shaping by oversampling without complex calibration circuits. By taking advantage of low noise features, various ΔΣ ADC schemes, such as Δ or Δ-ΔΣ ADCs, have been adopted for recording front-ends [11], [12], [18]-[20]. However, one of drawback in the ΔΣ ADCs is that they cannot accommodate the multiplexed inputs unless multiple integrator memories are used to store the sampled data from each input, which may significantly increase the design complexity [21], [22]. Considering the pros and cons of the two types of ADCs, a hybrid of ΔΣ and Nyquist ADCs can be a good fit to multi-channel neural recording front-ends. Since the incremental ΔΣ ADC (IADC) inherits the quantization noise shaping from ΔΣ modulation, it can easily achieve an effective resolution higher than 10-bits without calibrations. Furthermore, integrate-and-reset operation can allow for TDM inputs, similar to the Nyquist ADCs [22]-[24], [51].

One thing that should be considered is the IADC may not give the best noise-power efficiency. This is due to the accumulate-and-dump operation associated with periodic resets in IADCs [22]-[24]. In this operation, the quantized samples are accumulated in an integrate-and-reset filter, such as a cascade-of-integrators (CoI) filter, for decimation. Each sample has an uneven weighting coefficient in the multi-order (≥ 2nd-order) implementation; in other words, the earlier quantized sample may have a larger weight than the later ones in the integrate-and-reset filter. Therefore, the total noise accumulated during a single conversion period can be unequally weighted and cannot be averaged out from the oversampled noise [22]-[24]. On the other hand, the oversampled noise can be averaged out in the ΔΣ ADCs because all the quantized samples have the equal weight during the integrate-and-differentiate decimation process which uses the previously sampled data without reset. Due to such noise penalty, the multi-order IADCs must consume more power than the ΔΣ ADCs to achieve the same target resolution. To compensate for the noise-power penalty, a novel power saving scheme is desired for the energy-efficient IADCs.

A few techniques have been recently presented to enhance the performance of the IADCs for multi-channel neural recordings. A slicing technique was introduced to optimize the noise-power performance by dynamically activating or deactivating the sliced integrators during a single conversion period [22], [25]. However, this approach requires delicate design of multiple replica integrators as well as a complicated timing controller. In another approach, a two-step conversion was adopted to save power by reducing an oversampling ratio (OSR) [26]. Although the OSR could be effectively reduced, this technique is also affected by the mismatch between the coarse and fine DACs.

Here, we propose an LFP-adaptive dynamic zoom-and-track scheme that can significantly enhance the power-efficiency of the IADC. In addition, it can also improve noise-power performance when engaged in multi-channel subcortical recording front-ends [27]. The proposed scheme enables the IADC to resolve tiny and fast-changing APs in a zoomed sub-LFP range while simultaneously tracking the large but slow-varying LFPs. The sub-LFP range is adaptively adjusted at each conversion period. This scheme has an inherent advantage because the envelope of subcortical signals (LFPs) has high temporal correlations while fast APs are sporadic. Note that neural signals have $1/f^N$ (N = 1 – 2) spectral characteristics. The IADC can effectively narrow-down the input dynamic range (DR) by exploiting such a spectral characteristic of subcortical signals [28]-[30]. As a result, the dynamic range (DR) can be substantially relaxed. For example, the OSR of a 2nd-order IADC can be reduced by 64.3% when compared to the conventional design, resulting in low power operation. Furthermore, since the proposed zooming operation can be implemented without an additional coarse DAC or ADC, it completely eliminates the concern of mismatches in the coarse-fine conversion circuits, as found in [26], [31], [32]. The proposed scheme also allows for on-chip dual-band recording (broadband and LFP band) without using additional hardware. As a proof of the concept, we implemented a four-channel subcortical recording front-end IC employing the proposed LFP-adaptive dynamic zoom-and-track IADC. The implemented chip demonstrated the acquisition of dual-band neural recording from multi-channel high-resolution data conversion in animal experiments.

The remaining contents of this paper are organized as follows. A concept of the proposed LFP-adaptive dynamic zoom-and-track incremental ΔΣ front-end is explained in Section II. The detailed implementations of subcortical recording front-end circuits are described in Section III. Section IV provides the results of bench-top and *in vivo* experimental results. The performance of the fabricated front-end IC is summarized and compared with the state-of-the-art works. Finally, Section V concludes the paper.

II. LFP-Adaptive Dynamic Zoom-and-Track Front-End

A. Operational Principle

Subcortical neural signals consist of APs and LFPs. The AP represents the activity of each individual neuron [1]. Since the AP is generated by the rapid change of membrane potential in

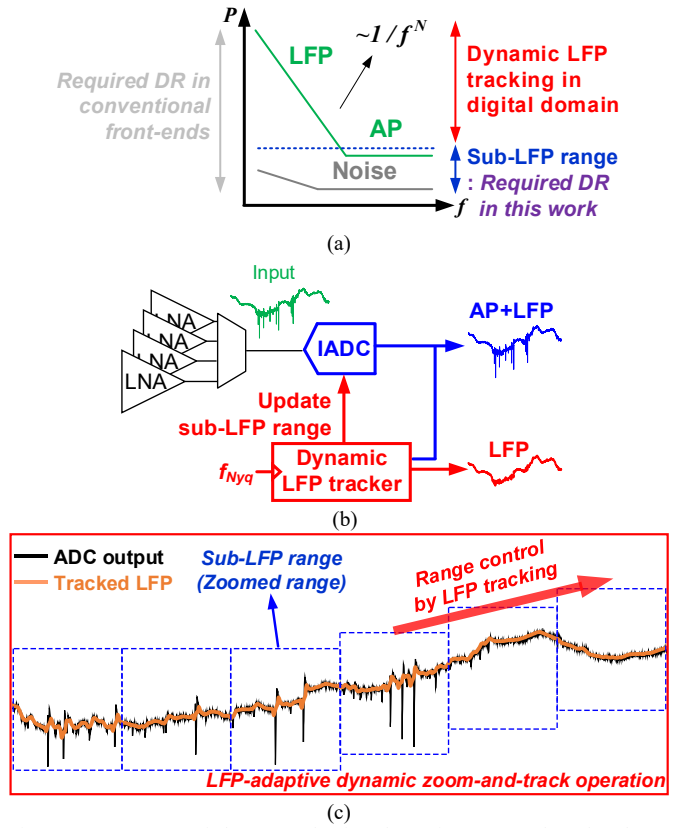


Fig. 2. (a) Concept of the LFP-adaptive dynamic zoom-and-track scheme using the $1/f^N$ spectral characteristic of subcortical signals. (b) Conceptual architecture block diagram of the front-end using the proposed scheme. (c) Conceptual transient operation with the proposed LFP-adaptive dynamic zoom-and-track scheme.

neurons, it appears as a high frequency spiky waveform (300 Hz – 10 kHz) with a small magnitude (10 – 300 μV). On the other hand, the LFP composes the superposition of potentials generated from multiple neurons and other cells around a recording site. It varies slowly (0.1 – 300 Hz) with a relatively large magnitude (~3 mV). In terms of spectral characteristics, the LFPs strongly follow a $1/f$ slope, while the APs exhibit an approximately flat spectrum due to its Poisson-distributed characteristics in the frequency domain [28], [33]. The subcortical signal is observed as the mixture of APs and LFPs; thus, it shows the power spectrum approximated as a $1/f^N$ curve (N = 1 – 2) [28], [29]. The subcortical recording front-end circuits should fully embrace both signal components with a wide input DR, a broad bandwidth, and low input-referred noise.

Especially, the DR specification is directly related to the power consumption of the ADC. The DR imposes two things: the minimum resolvable signal for analog-to-digital conversion and the maximum signal the ADC can handle. The least-significant bit (LSB) size should be smaller than the given noise floor. With the fixed noise floor, a wider DR means that the ADC should accommodate a larger input amplitude. One solution is to increase the supply voltage accordingly to cover the full-scale range. Otherwise, input signals have to be folded, since the supply voltage is lower than the maximum input magnitude [34]. Either strategy necessitates more power consumption due to the increased supply voltage or from the signal folding circuits added in front of the ADC [35], [36]. The requirement of a wider DR eventually results in more power dissipation in the ADC. In some cases, the ADC often consumes more than half of the entire front-end [25], [37].

In order to reduce the power consumption, we propose the LFP-adaptive dynamic zoom-and-track scheme that significantly reduces the required signal DR in the analog-to-digital conversion. This scheme splits the DR into multiple amplitude ranges and adaptively allocates a given DR depending on the LFP magnitude. As shown in Fig. 2(a), the proposed scheme only requires a small sub-LFP dynamic range that marginally covers AP signals to record the whole neural signals. This is feasible because the proposed scheme tracks the large LFPs in the digital domain and reallocates a sub-LFP dynamic range. As a result, the IADC only needs to convert a small dynamic range of signals. Through this adaptive DR allocation, a relatively-low resolution A-D conversion can be used, consequently reducing the power consumption significantly.

The proposed scheme may look similar to a signal folding technique in terms of operation principle: dividing the input signal into multiple amplitude ranges. However, this scheme gives much higher power-efficiency than the conventional signal folding technique since the large amplitude input is processed in digital domain at low power consumption. For example, a couple of recent works using the signal folding technique consumed ~2.6 μW to fold the input signal in analog domain, and achieved ~12 bit resolution [35], [36]. On the other hand, the proposed scheme adds a negligible digital power overhead (< 0.2 μW) but can achieve ~11 bit resolution. Assuming that the power needed to split the input signal is proportional to a target resolution, the proposed scheme can achieve ~6.5× higher power efficiency than the conventional signal folding technique.

Some prior arts may also look similar to our approach. For example, a mixed-signal DC-servo loop was used to reject the EDO in the DC-coupled LNA or LFPs in the summing amplifier to truncate the signal over the ADC input range, with the assistance of an off-chip FPGA [52]. However, our approach reuses the tracked LFPs to adaptively allocate the signal DR into multiple amplitude regions to improve the power-efficiency of the ADC significantly. It realizes the LFP tracking by a compact zooming scheme using an on-chip digital tracker, which does not require an additional summing amplifier and an external FPGA. In addition, our scheme can remove the EDO by simply using the AC-coupled pre-amplification stage without a complicated offset cancellation loop. Neural signal acquisition can be reliably achieved with an AC-coupled front-end from the advanced high-density microelectrodes [12]. Other prior arts, such as the track-and-zoom ADC, cover the large inputs by using the radix-2 autoranging technique that dynamically expands the conversion range of the ΔΣ modulator [18-20]. Although this technique can effectively track rapidly-varying large signals, the resolution must be compromised during the tracking operation since the conversion range expands exponentially. On the other hand, the proposed scheme maintains the magnitude of conversion range; therefore, the resolution is not affected by tracking operation.

Fig. 2(b) conceptually illustrates how the proposed scheme operates in a multi-channel subcortical recording front-end.

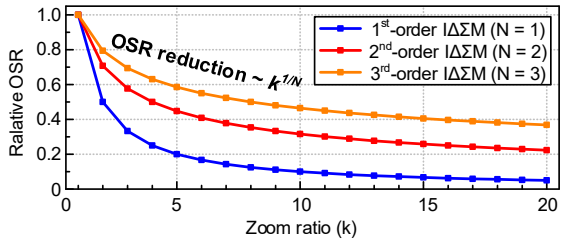


Fig. 3. OSR ratio between the proposed scheme and the conventional design, as a function of a zoom ratio (k) in 1st – 3rd-order incremental ΔΣ modulators.

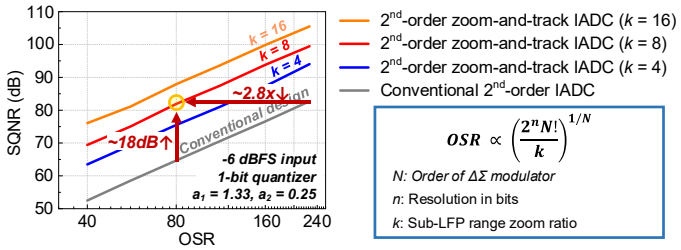


Fig. 4. Simulated SQNR versus OSR at -6 dBFS input in the 2nd-order LFP-adaptive dynamic zoom-and-track IADC with various k compared to the conventional design.

The multi-channel subcortical neural signals are pre-amplified by the LNAs. The IADC resolves the amplified APs in a sub-LFP range, *i.e.,* a zoom-in range, during a single conversion cycle. Then, the dynamic LFP tracker estimates the LFP magnitude by filtering the decimated outputs in digital domain. Finally, the sub-LFP range is updated according to the tracked LFP signals. The feedback of the LFP tracker allocates a small effective input range for the IADC. Fig. 2(c) shows a pre-recorded subcortical neural signal processed by the proposed scheme. The scheme follows the trace of LFPs (orange) without loss of signal integrity by seamlessly adjusting the sub-LFP range. The IADC operates with a sufficiently high rate (in this work, 25 kHz, that sets a Nyquist rate for sampling subcortical neural signals).

As aforementioned, the reduced DR relaxes the resolution requirement of the ADC. Since the resolution of the IADC is determined by the OSR, the proposed scheme significantly lowers the OSR. The required OSR of the conventional Nth-order IADC with 1-b quantization is proportional to $(2^n \cdot N!)^{1/N}$, where n is a full-scale resolution in bits [24]. Here, it is assumed that the OSR is much larger than 1. By using the proposed scheme, the required resolution in a sub-LFP range is equal to $[n - \log_2 k]$ bit where k is a zoom ratio. The magnitude ratio of the full-scale to a sub-LFP range (*i.e., k*) is inversely proportional to the sub-LFP range magnitude. Therefore, the OSR can be reduced by a factor of $k^{1/N}$. Fig. 3 shows the ratio of the OSR in the proposed scheme to the conventional design as a function of k, for 1st – 3rd-order incremental ΔΣ modulators. As shown in Fig. 3, the required OSR becomes smaller as k increases. It is noteworthy that the proposed technique is more useful for neural recording and bioinstrumentation applications, where the low order (< 3rd-order) ΔΣ modulators are preferred for optimal operation in terms of precision, speed, and area [7], [38], [39]. For choosing an optimal k, signal integrity has to be considered in addition to the OSR reduction. The larger k is, the narrower a sub-LFP range becomes. In case k becomes extremely large, the sub-LFP range may become smaller than the maximum magnitude of pre-amplified AP signals. This can

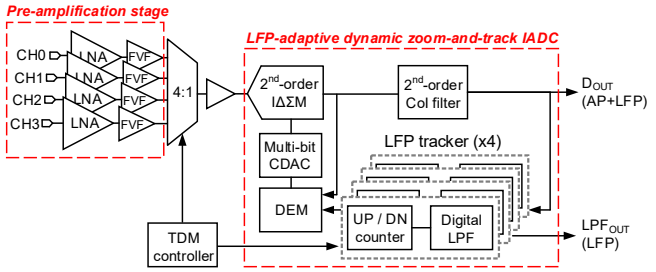


Fig. 5. Overall architecture of the subcortical recording front-end IC using an LFP-adaptive dynamic zoom-and-track scheme.

severely degrade the signal integrity because the pre-amplified AP signals can be clipped in the sub-LFP range. In this work, we chose k as 8 to ensure the signal integrity. The related details are explained in Section III.

Fig. 4 shows the estimated signal-to-quantization noise ratio (SQNR) as a function of the OSR for the 2nd-order IADCs. The SQNR values were simulated in time-domain with -6 dBFS input [59]. It indicates that the 2nd-order LFP-adaptive dynamic zoom-and-track IADC with the selected zoom ratio (k = 8) and loop-filter coefficients (a_1 = 1.33, a_2 = 0.25) can achieve the SQNR of ~82 dB at -6 dBFS input with an OSR of 80, which is by ~2.8× smaller than that required for the conventional design using the same loop-filter coefficients. Here, the values of a_1 and a_2 are given according to the dynamic-range scaling [42]. The relevant detail is explained in Section III.

This reduced OSR relieves the speed requirement of analog integrators in the IADC. Since the proposed scheme significantly down-scales the input amplitude of the ADC, we can easily implement an integrator from an operational transconductance amplifier (OTA) without stringent requirement of linearity and slew rates. Therefore, the relaxed requirement of gain-bandwidth product (GBW) for an OTA translates into power reduction by a factor of 2.8, corresponding to 64.3% power saving compared with the same linear OTA (no slewing) in the conventional IADC. For estimation, we also assume that the main transistors in the OTA operate in the sub-threshold region. Please note that the actual power saving can be larger than 64.3%. In the conventional design, the OTA slews when large input signals are applied; thus, it consumes more power to satisfy the required operation speed with the limited driving current [53]. The required slew rate of a quantizer is also relaxed according to the OSR reduction. Note that, an additional hardware, an LFP tracker, is required in the proposed scheme. However, this power overhead is negligible due to a slow clock speed of 25 kHz to process the 80× decimated signals in each recording channel with TDM operation. Please note that the LFP trackers are assigned to each recording channel individually. Actually, the LFP tracker contributes only 6% of the per-channel digital power consumption in this work.

B. System Architecture

Fig. 5 shows the overall system architecture of an incremental ΔΣ front-end using the proposed LFP-adaptive dynamic zoom-and-track scheme. The front-end is composed of two parts: a multi-channel pre-amplification stage and an LFP-adaptive dynamic zoom-and-track IADC. The total four subcortical neural recording channels have been implemented for proof of concept. Each recording channel consists of an

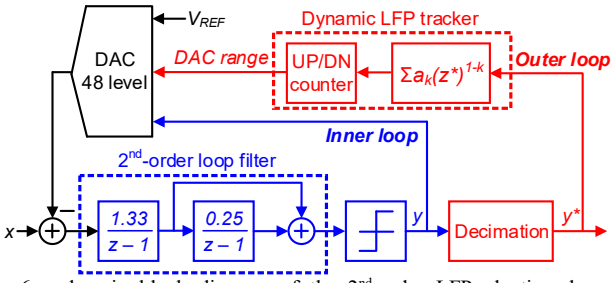


Fig. 6. z-domain block diagram of the 2nd-order LFP-adaptive dynamic zoom-and-track IADC.

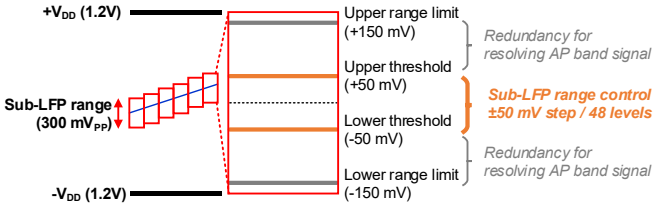


Fig. 7. Sub-LFP range control with preset thresholds.

LNA with a mid-band voltage gain of 40 dB and a pair of flipped voltage follower (FVF) buffers. Those four recording channels are time-division multiplexed with a 2nd-order LFP-adaptive dynamic zoom-and-track IADC.

In the IADC block, a 2nd-order cascade-of-integrator (CoI) decimation filter and four digital LFP trackers are integrated with a 2nd-order incremental ΔΣ modulator. Since the LFP tracker is assigned to each recording channel, the LFPs from different recording sites can be tracked independently. Therefore, the proposed front-end circuit can record signals from broad regions in the brain without strict limitation in the spatial coverage, unlike the previous work that depends on the spatial correlation among the multi-channel LFP waveforms [40]. A multi-bit feedback CDAC is used for zooming operation. Since the sub-LFP range is determined according to the CDAC output, the CDAC mismatch can cause offsets and coverage variations in different sub-LFP ranges. Therefore, a dynamic element matching (DEM) module is used to suppress the CDAC mismatch. The front-end provides the two output signals: one is the decimated ADC output (broadband signal) and the other is the tracked LFP. Dual-band outputs are provided through the on-chip serial peripheral digital interface (not shown in the figure). The benefit of this feature is explained in detail in Section IV.

III. Circuit Implementation

A. LFP-Adaptive Dynamic Zoom-and-Track IADC

Fig. 6 shows a z-domain block diagram of the proposed LFP-adaptive dynamic zoom-and-track IADC. The IADC consists of two loops. The inner loop implements the 2nd-order ΔΣ modulation. The loop filter is constructed with a cascade of integrators with feed-forward (CIFF) topology for high linearity with minimal input referred noise and distortion contributed by the 2nd integrator, and low power implementation using a single feedback DAC [41], [42]. The loop filter coefficients (a_1 = 1.33, a_2 = 0.25) are determined through the dynamic-range scaling [42]. The output swing of each integrator can be much larger than the sub-LFP range that confines the ADC input. Therefore, the 1st integrator coefficient

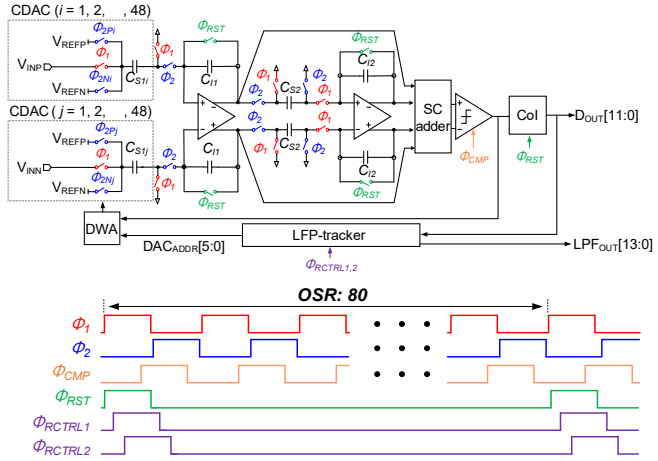


Fig. 8. Schematic and operation timing diagram of the 2nd-order LFP-adaptive dynamic zoom-and-track IADC.

(a_1) can be substantially upscaled for effectively suppressing the noise and distortion contributed from the 2nd integrator. The 1-bit quantization has been chosen to avoid quantizer nonlinearity.

The outer loop dynamically tracks the LFP band signals and regulates the sub-LFP range. The output range of the multi-bit DAC is tracked in the digital domain. As shown in Fig. 7, the LFP tracker adjusts the sub-LFP range up or down by one DAC level if the tracked LFP amplitude becomes higher or lower than the preset threshold, respectively. For design simplicity, the magnitude of a range relocating step (= one DAC level) is set to be equal to the preset threshold level. The values for sub-LFP ranges, preset thresholds, and range relocating steps are selected to meet the following condition given by:

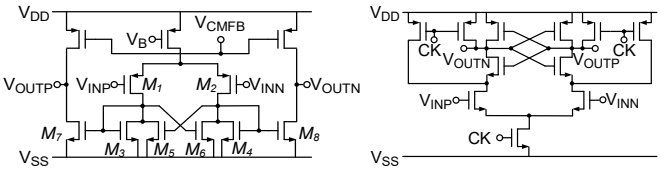
$$(|V_{thr}| + |V_{AP,max}| + |\Delta V_{LFP,max}|)(1+\alpha) \le MSA_{sub}|V_{lim}| \quad (1)$$

where V_{thr} is a preset threshold, $V_{AP,max}$ is the maximum magnitude of pre-amplified AP signals, $\Delta V_{LFP,max}$ is the maximum variation of pre-amplified LFP signals during a single conversion period, α is the ratio of the additional amplitude margin to accommodate variations and external interferences in real operation, MSA_{sub} is the maximum stable input amplitude in the sub-LFP range, and V_{lim} is the upper/lower limit amplitude of the sub-LFP range. Here, $\Delta V_{LFP,max}$ can be approximated as:

$$\Delta V_{LFP,max} \approx V_{LFP,max}\, \omega_{LFP,max}\, T_{Nyq} \quad (2)$$

where $V_{LFP,max}$ is the maximum magnitude of pre-amplified LFP signals, $\omega_{LFP,max}$ is the maximum frequency of the LFP, and T_{Nyq} is the conversion period of the IADC. With an enough amplitude margin (α = 0.3) and a given MSA_{sub} (-3 dB), the sub-LFP range and preset threshold can be set at ±150 mV and ±50 mV, respectively. In this work, k (zoom ratio) is selected to be 8 with a full scale of ±1.2 V. A 48-level DAC is adequate to cover the full-scale since the range adjusting steps are ±50 mV, the same as the preset threshold.

Fig. 8 shows the schematic and operation timing diagram of the 2nd-order LFP-adaptive dynamic zoom-and-track IADC.



(a) (b)

Fig. 9. (a) Schematic of a current mirror OTA in SC integrators. (b) Schematic of the dynamic comparator used as a 1-bit quantizer.

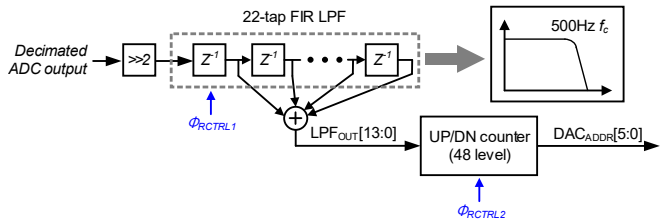


Fig. 10. Block diagram of the LFP tracker.

We chose a discrete-time ΔΣ modulator with switched-capacitor (SC) integrators which are more robust to process and timing variations than continuous-time RC-integrators [42]. The 48-level feedback CDAC, also working as a sampling capacitor (C_{S1}) of the 1st integrator, is implemented with an array of unit metal-insulator-metal (MIM) capacitor of 35.6 fF, which is the minimum capacitance allowed in the given CMOS process. The total input sampling capacitance (C_{S1}) is 1.71 pF. It contributes to the LNA input referred noise less than 1 μV_{rms}. The 2nd integrator is implemented with a sampling capacitance (C_{S2}) of 35.6 fF. The *kT/C* noise of C_{S2} is substantially attenuated by the 1st integrator gain. The outputs of the 1st and 2nd integrators are summed at the SC adder that is also implemented with the minimum capacitors. The data weighted averaging (DWA) is used to reject the in-band distortion caused by the feedback CDAC mismatches [43]. With the given OSR of 80, the in-band distortion from the 48-level CDAC is suppressed below -110 dBFS. This is sufficiently low to achieve a target SQNR of 80 dB. According to simulation assuming that the CDAC mismatch follows the Gaussian distribution, the DWA can reduce the total amount of the mismatch error accumulated in a Nyquist conversion period by 98.4% in average with various input amplitudes. We chose the DWA for its simple implementation with a multi-level feedback DAC although the DWA is not be fully optimized for the accumulate-and-dump operation of IADCs. As an alternative, the Smart-DEM, which may be more optimal but require more complicated architecture, can be considered for further improvement [54]. The oversampling frequency is set at 8 MHz for achieving the Nyquist rate of 25 kS/s per channel.

Fig. 9(a) shows the schematic of a current mirror OTA used for SC integrators. The local positive feedback is used to boost the GBW of OTAs for high speed settling with low power consumption [11], [44]. The GBW of the designed OTA is given by:

$$GBW = \frac{g_m}{2\pi C_L}\frac{\beta}{1-\alpha} \quad (3)$$

where g_m is the input transconductance, α is the current ratio of $M_{5,6}$ to $M_{3,4}$, β is the current ratio of $M_{7,8}$ to $M_{3,4}$, and C_L is the load capacitance. We chose α = 0.8 and β = 5 in the 1st integrator OTA, considering the relatively large integration capacitance (C_{I1}) of 1.3 pF. Since the 2nd integrator uses much smaller integration capacitance (C_{I2}) of 142.4 fF, we chose relatively relaxed parameters (α = 0.5 and β = 1) in the 2nd integrator OTA. A 1-bit quantizer was implemented with a low-power dynamic comparator as shown in Fig. 9(b).

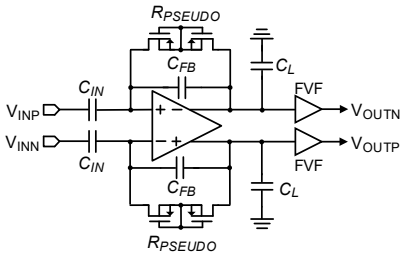


Fig. 11. Schematic of the AC-coupled low-noise pre-amplification stage.

Fig. 10 shows the detailed components of an LFP tracker. A 22-tap finite impulse response (FIR) digital low-pass filter (LPF) is used to reject high frequency signals out of the LFP band. The FIR filter is chosen to avoid the phase distortion of the tracked LFPs [45]. The LPF provides a low-pass cutoff frequency of 500 Hz at a sampling rate of 25 kS/s. Two LSBs of the FIR LPF input, *i.e.*, the decimated ADC output, are truncated to reduce the area and power consumed by the FIR LPF. An error caused by this truncation is negligible because a sufficiently large amplitude margin is assigned between the upper (or lower) threshold and the corresponding sub-LFP range limits. For design simplicity, all the filter coefficients are set to be unity. The 48-level up/down counter is used to adjust the 6-bit DAC address according to the magnitude of tracked LPF band signals, *i.e.*, the output of the FIR LPF.

In this proof-of-concept, we implemented the 2nd order IADC with the most commonly used architecture that consists of SC integrators and feedback CDAC. However, it is noteworthy that the proposed zoom-and-track scheme can be applied to any IADCs with multi-bit feedback, in which the circuit performance can be further improved by combining our scheme with other design techniques used for high-performance IADCs, such as two-phase linear-exponential accumulation or low-power voltage-controlled oscillator-based integrators [55], [56].

B. Pre-Amplification Stage

Fig. 11 shows the schematic of the low-noise pre-amplification stage dedicated to each recording channel. Neural signals from recording electrodes are capacitive-coupled to an LNA. This will reject the dc-offset that can easily saturate the LNA [46]. A pre-amplification gain of 40 dB is set by the ratio of the input capacitance (C_{IN}) to the feedback capacitance (C_{FB}). C_{IN} is 3.56 pF and the minimum capacitance of 35.6 fF is used for C_{FB}. The input impedance of an LNA is estimated as ~40 MΩ at 1 kHz. This is sufficiently large to be paired with typical microelectrodes for subcortical neural recording [47]. The LNA bandwidth is designed as 0.1 Hz to 10 kHz for recording broadband neural signals, while rejecting the electrode DC-offset. The sub-Hz high-pass (DC)

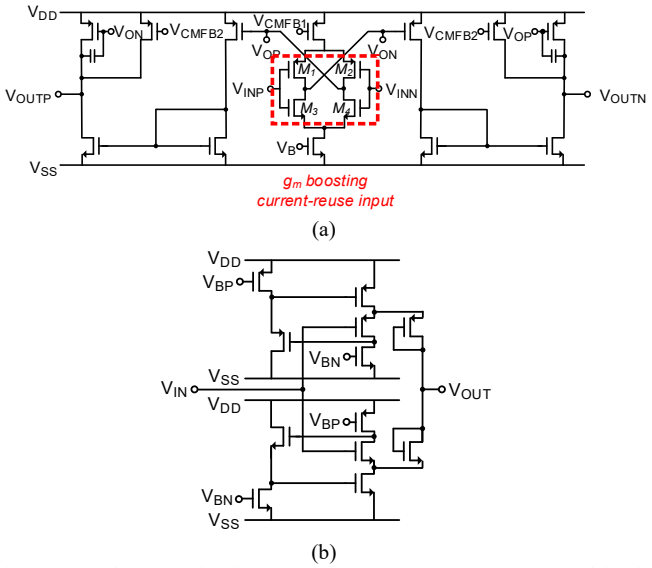


Fig. 12. (a) Schematic of a class AB two-stage current-reuse OTA used for the AC-coupled LNA. (b) Schematic of a flipped voltage follower used for the LNA output buffer.

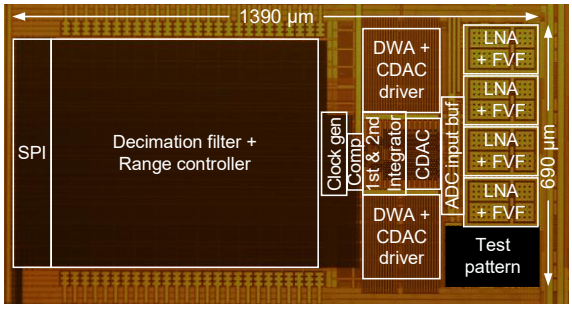


Fig. 13. Microphotograph of the fabricated front-end IC.

cutoff frequency is realized by near off-state PMOS pseudo resistors (R_{PSEUDO}) [12], [13]. The design of R_{PSEUDO} was chosen due to its implementation simplicity. The PMOS transistors composing R_{PSEUDO} were sized to achieve a sub-Hz cutoff frequency with the process variation. The post-layout Monte-Carlo simulation results (N = 200) show that the designed R_{PSEUDO} limits the high-pass cutoff frequency under 1 Hz (m = 0.14 Hz, σ = 0.057 Hz at room temperature; m = 0.40 Hz, σ = 0.15 Hz at 40 ºC). The load capacitance (C_L) of 3.63 pF is used to set the low-pass cutoff frequency.

Fig. 12(a) shows the schematic of a class AB two-stage current-reuse OTA used for the AC-coupled LNA. The input g_m of the OTA is doubled by using the complementary input transistor pairs, $M_{1,2}$ and $M_{3,4}$. As a result, the input referred thermal noise power of the OTA can be reduced by half. A push-pull output stage is used to provide a wide output linear range. A pair of flipped voltage follower (FVF) buffers are used to fix the LNA bandwidth regardless of TDM operation, and also drive the multiplexer and ADC input buffer. The FVF buffer was chosen due to low power consumption and design simplicity [48].

IV. Experimental Results

Fig. 13 shows a microphotograph of the front-end IC fabricated through the TSMC 180 nm mixed-signal CMOS process. The core of the front-end IC, including test patterns, occupies an area of 0.96 mm^2. The active circuit area is measured as 0.23 mm^2 per channel. Fig. 14 shows the breakdowns of per-channel power consumption measured from the fabricated front-end IC, compared with the one estimated from simulation without the proposed scheme. A significant amount (57.6%) of power reduction has been achieved because the proposed zoom-and-track scheme relaxes the speed requirement of an ADC input buffer as well as the dynamic range burden of the ADC. Each recording channel of the fabricated front-end IC consumes a total power of 25.2 µW. The dynamic zoom-and-track IADC only consumes 6.8 µW. The LFP tracker, the main overhead block in the presented architecture, dissipates 0.17 µW that is only 2.4% of the total ADC power consumption.

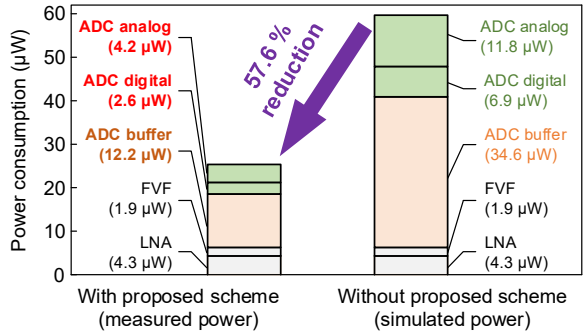


Fig. 14. Per-channel power breakdowns of the fabricated front-end IC compared with the simulated power consumption of the front-end without the proposed LFP-adaptive dynamic zoom-and-track scheme.

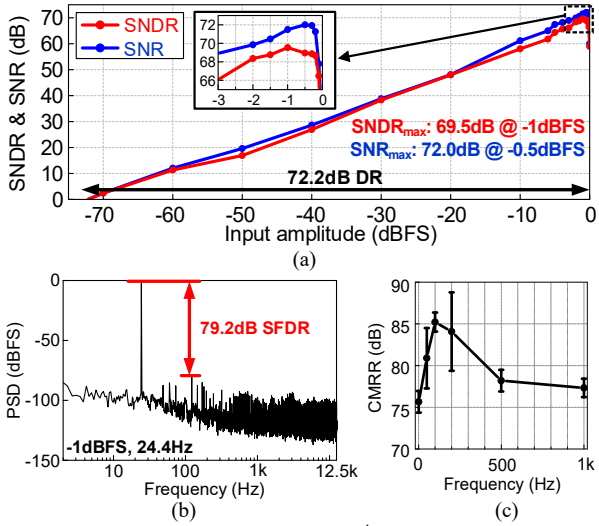


Fig. 15. Measured performance of the 2nd-order LFP-adaptive dynamic zoom-and-track IADC. (a) SNDR and SNR versus input amplitude. (b) Output power spectrum at -1 dBFS input. (c) CMRR versus common-mode input frequency (n = 3).

A. Performance Measurements

Fig. 15 shows the measured performance of the fabricated LFP-adaptive dynamic zoom-and-track IADC. The maximum signal-to-noise-and-distortion ratio (SNDR) was measured as 69.5 dB. The corresponding ENOB was 11.3-bit. The peak signal-to-noise ratio (SNR) and DR were measured as 72.0 dB and 72.2 dB, respectively. Fig. 15(b) shows the power spectrum of the de-multiplexed ADC output at -1 dBFS input. The spurious-free dynamic range (SFDR) was measured as 79.2 dB. Fig. 15(c) shows the common-mode rejection ratio (CMRR)

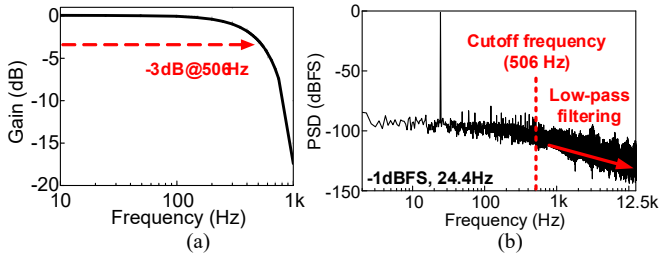


Fig. 16. Measured characteristics of the LFP tracker. (a) Frequency response of the FIR LPF. (b) Output power spectrum at -1 dBFS input.

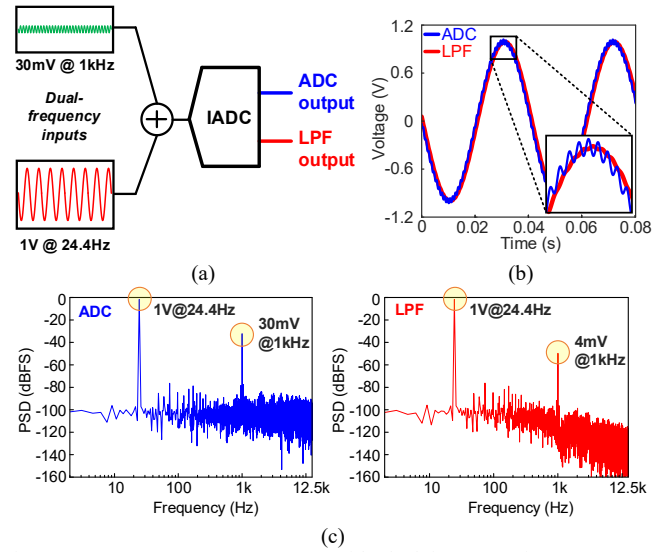


Fig. 17. ADC output measurement with dual-frequency inputs. (a) Test configuration. (b) Output transient diagrams. (c) Output power spectra.

measured from the fabricated IADC. The CMRR was higher than 74.5 dB. Finally, FoM_{Walden} and FoM_{SNDR} of the fabricated IADC are calculated as 107.9 fJ/c-s and 162.1 dB, respectively, based on the measurement.

Fig. 16 shows the measured performance of the LFP tracker. According to the measured frequency response in Fig. 16(a), the FIR LPF shows a low-pass cutoff frequency at 506 Hz that is sufficient to obtain LFP band signals from an animal brain [49]. Fig. 16(b) shows the power spectrum of the LPF output at -1 dBFS input. As clearly shown in the spectrum, high frequency components outside the LFP band were well suppressed through the digital low-pass filtering. The LPF output achieves the peak SNDR (72.9 dB) and SNR (79.5 dB) that are slightly higher than those of the ADC output.

Fig. 17 shows a test setup for dual-band recording performance of the fabricated IADC. As illustrated in Fig. 17(a), the dual-frequency inputs, consisting of a small amplitude high frequency signal (-32 dBFS at 1 kHz, emulating spikes) superimposed on a large amplitude low frequency signal (-1.6 dBFS at 24.4 Hz, emulating LFPs), were applied to the fabricated IADC. Fig. 17(b) shows the dual-band output transients. The ADC output shows both signals clearly, while the LFP tracker provides only the large amplitude low frequency signal. Fig. 17(c) shows the output power spectra of the ADC and LFP tracker, respectively. As shown in the graphs, the fabricated IADC resolves both input components (*i.e.*, broad-band signals that contains both LFPs and spikes) without amplitude degradation, while the LFP tracker suppresses the high-frequency signals accordingly.

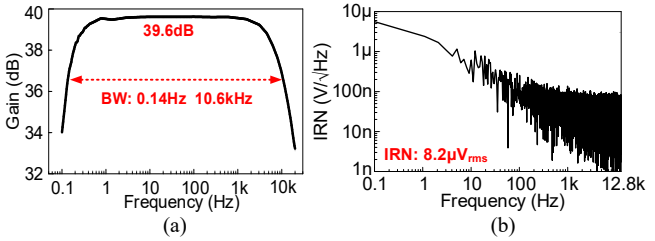


Fig. 18. Measured characteristics of the LNA: (a) Frequency response, (b) Input-referred noise power spectrum.

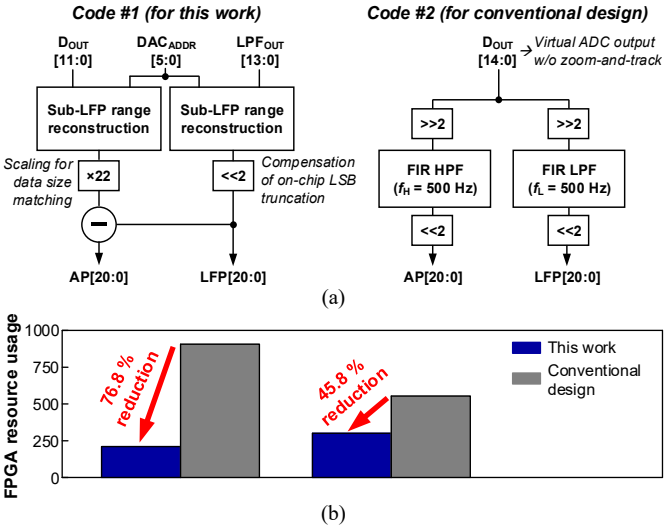


Fig. 19. (a) Algorithm diagrams of two post-processing codes. (b) Reduction in the post-processing FPGA resources for subcortical signal band separation through the on-chip dual-band recording.

The measured performance of the pre-amplification stage is shown in Fig. 18. The frequency response of the fabricated LNA is depicted in Fig. 18(a). The LNA provides a mid-band gain of 39.6 dB within the bandwidth from 0.14 Hz to 10.6 kHz. Fig. 18(b) shows the LNA input-referred noise power spectrum. The input-referred noise of the fabricated LNA was measured as 8.2 μV_{rms} within 0.1 Hz to 10.6 kHz. The noise efficiency factor (NEF) of the fabricated LNA is calculated as 5.9 from 4.3 μW power consumption. The measured THD was lower than 1% with <8.2 mV_{PP} input. Here, the reference input of the measured LNA is shared with all the other LNAs.

B. Evaluation of Post-Processing Hardware Reduction

We also evaluated the benefit of on-chip dual-band recording features by estimating the amount of post-processing resources required to separate the subcortical signal bands (AP and LFP signals, respectively). For comparison, we prepared two different versions of post-processing codes in Verilog. The first code was written to extract dual-band signals, APs and LFPs, from the proposed front-end. The AP band signal can be easily acquired by subtracting the LFP tracker output from the ADC output. The second code was prepared for the conventional front-end. The AP and LFP bands are separated through the two filters that that are dedicated to each band, the same as the conventional procedure where the independent filters are used for each signal band of interest [57], [58]. For fair comparison, FIR filters with a 500 Hz cutoff frequency and 2-LSB truncated inputs are used in the second code. The LPF and HPF are

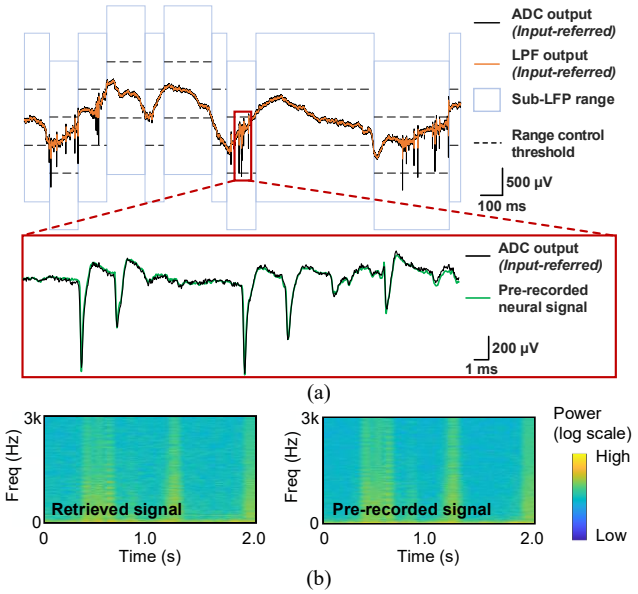


Fig. 20. Results of the bench-top test using the pre-recorded subcortical signals. (a) Transients of the pre-recorded (input) and retrieved (output) signals. (b) Power spectra of the pre-recorded (input) and retrieved (output) signals.

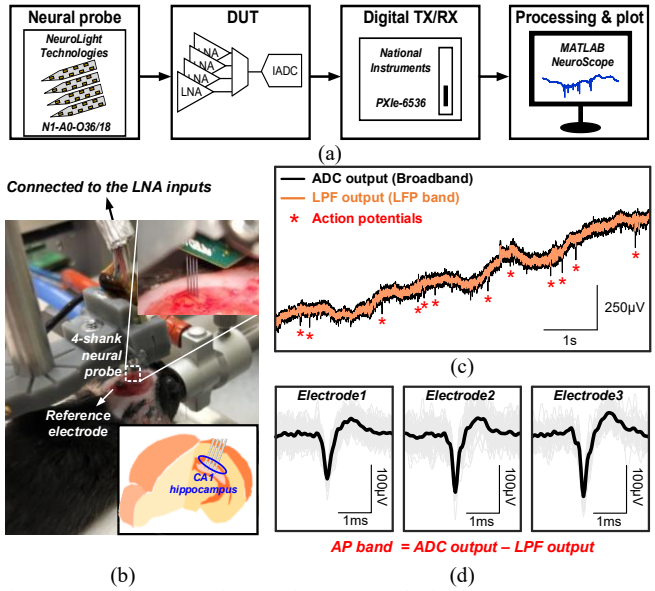


Fig. 21. *In vivo* experiments in an anesthetized mouse. (a) Overall experimental setup. (b) Brain implant configuration. (c) Recorded dual-band subcortical signals. (d) Sorted AP waveforms.

composed of 22 and 13 taps, respectively. Fig. 19(a) shows the algorithms used in the two post-processing codes. In the second code, it is assumed that the conventional front-end provides the same resolution to this work without zooming operation. Spartan-6 FPGA (XC6SLX45, Xilinx, CA, USA) was used to synthesize the prepared Verilog codes. Fig. 19(b) shows difference in the FPGA resources required between the two approaches. The on-chip dual-band recording reduces the significant amount of post-processing hardware resources: 76.8% in registers and 45.8% in lookup tables, respectively. It is noteworthy that these reductions can be achieved by directly reusing the tracked LFP signals without additional on-chip circuit blocks [25].

C. Neural Recording Experiments

We conducted a couple of experiments to evaluate the acquisition of subcortical signals. First, the performance of the fabricated IC was validated in a bench-top test using the pre-recorded neural signals. The pre-recorded mouse subcortical signal was applied to a PBS solution in which the four recording electrodes were placed to pick up the signals to the input of the fabricated front-end IC. Fig. 20 shows the measured results from the bench-top recording experiment. The transient response and power spectra support that the fabricated front-end IC successfully retrieved the pre-recorded subcortical signals by adjusting the sub-LFP ranges from the tracked LFPs.

Second, *in vivo* experiments were conducted in an anesthetized mouse. The animal procedures were approved by the Institutional Animal Care and Use Committee of the University of Michigan IACUC (protocol number: PRO00009668). Fig. 21 shows the *in vivo* experimental setup and obtained results. As illustrated in Fig. 21(a), a commercial multi-channel neural probe (N1-A0-O36/18, NeuroLight Technology LLC, MI, USA) was used to acquire subcortical signals from the mouse brain. The neural probe was implanted in the CA1 hippocampus region and the recording sites were connected to the input of the fabricated front-end IC, as shown in Fig. 21(b). Fig. 21(c) shows the measured subcortical signals in the *in vivo* test. The fabricated front-end IC accurately recorded broadband neural signals with distinctive action potentials and simultaneously tracked the LFPs. Fig. 21(d) shows the AP waveforms obtained from different recording sites. The AP signals were sorted from the rest of the signals by subtracting the LFP tracker output from the ADC output, following the aforementioned resource-efficient band separation method.

D. Performance Comparison

Table I shows the comparison of performance with the state-of-the-art neural recording front-end ICs using an IADC. The proposed LFP-adaptive dynamic zoom-and-track scheme can significantly save the ADC power consumption. As a result, the IADC integrated in this front-end achieved the best FoM_{Walden} of 107.9 fJ/c-s and FoM_{SNDR} of 162.1 dB, respectively, compared to the recently reported IADCs implemented in the other state-of-the-art neural recording front-ends. Furthermore, this work provides the intrinsic dual-band recording features without additional on-chip circuit blocks.

Table II summarizes the performance comparison with the recent brain recording oversampling ADCs. Majority of the works in the table adopted similar zooming or tracking techniques, such as radix-2 exponential tracking [18]-[20] or automatic gain control of a pre-amplifier [38]. This work realized the smallest FoM_{Walden} and highest FoM_{SNDR} among those ADCs implemented with zooming or tracking techniques. Also, the presented IADC provides a high bandwidth of >10 kHz, which is required to accurately record the whole neural activities including APs, unlike the other works targeting the narrowband signals with limited information, such as the LFP, ECoG, or EEG [18]-[20].

TABLE I
COMPARISON TO THE STATE-OF-THE-ART NEURAL RECORDING FRONT-END ICS USING THE IADCS

	This work	[7]	[26]	[50]
Application	**Broadband**	Broadband	Broadband	ECoG
Architecture	**IA+ADC**	ADC only	ADC only	ADC only
Technology (nm)	**180**	180	180	22
Supply voltage (V)	**1.2**	1.8	1.8	0.6/0.8
IADC type	**2nd-order**	1st-order	Two-step	1st-order
Dual-band recording	**Yes (reusing of tracked LFP)**	No	No	No
TDM	**Yes (4 ch)**	No	No	Yes (16 ch)
# of channel	**4**	144	8-24	256
ADC SNDR (dB)	**69.5**	51.1	58.0	46.1[a]
ADC BW/ch (kHz)	**12.5**	10	10	0.5
ADC power/ch (μW)	**6.8[c]**	21.0[d]	8.6[c]	1.6[c]
FoM_{Walden} (fJ/c-s)[e]	**107.9**	3577.4	681.4	9763.5
FoM_{SNDR} (dB)[f]	**162.1**	137.9	148.7	131.0
IRN (μV_{rms})	**8.2**	21.0[g]	2.3 (LFP), 3.9 (AP)	1.6
Power/ch (μW)	**25.2[c]**	46.3[c,h]	13.9[c,h]	1.8[c,h]
Area/ch (mm^2)	**0.23**	0.0049	0.00378	0.001

[a.] Estimated from the reported graph. [b.] Estimated from the reported ENOB. [c.] Including the decimation filter. [d.] Simulated value.
[e.] Calculated through FoM_{Walden} = Power / $\{2 \times BW \times 2^{(SNDR - 1.76) / 6.02}\}$ [f.] Calculated through FoM_{SNDR} = SNDR + $10\log_{10}$(BW / Power)
[g.] Calculated by aggregating the reported noise data in the LFP and AP bands. [h.] Including the data chain.

TABLE II
COMPARISON TO THE RECENT BRAIN RECORDING OVERSAMPLING ADCS

	This work	[18]	[19]	[20]	[38]	[37]	[60]
Application	**Broadband**	LFP, ECoG	EEG	LFP, ECoG	Broadband	Broadband	Broadband
ADC type	**2nd-order DT IADC**	2nd-order hybrid ΔΣADC	1st-order DT ΔADC	1st-order DT Δ^2ΣADC	2nd-order CT zoom ADC	3rd-order CT ΔΣADC	2nd-order CT ΔΣADC
Zooming or tracking technique	**LFP-adaptive dynamic zoom-and-track**	Radix-2 predictive digital autoranging	Radix-2 adaptively clock-boosted autoranging	Radix-2 track-and-zoom	Automatic-gain -controlled AFE	N/A	N/A
Technology (nm)	**180**	65	130	130	180	40	110
Supply voltage (V)	**1.2**	0.8	1.2/3.3	1.2/0.6	1.2/0.8	1.2	1.0
Dual-band recording	**Yes**	No	No	No	No	No	No
TDM	**Yes**	No	No	No	No	No	No
Power (μW)	**6.8[a,b]**	0.8	0.79	1.7[a]	10.9	4.5	6.5
SNDR (dB)	**69.5**	66.0	62.5	70.0	70.1	93.5	80.4
DR (dB)	**72.2**	92	-	92.0	99.5	96.5	81.0
ENOB (bit)	**11.3**	10.7	10.1	11.3	11.4	15.2	13.1
CMRR (dB)	**>74.5**	81.0	-	70.0	68.0	81.2	76.0
Bandwidth (kHz)	**12.5[c]**	0.5	0.5	0.5	5	5	10
Quantizer # of bit	**1**	1	1	1	1	6	4
FoM_{Walden} (fJ/c-s)[d]	**107.9**	480.9	719.8	674.2	403.4	11.6	38.0
FoM_{SNDR} (dB)[e]	**162.1**	154.0	150.5	154.7	156.7	184.0	172.3

[a.] Including the decimation filter. [b.] Power per channel. [c.] Bandwidth per channel.
[d.] Calculated through FoM_{Walden} = Power / $\{2 \times BW \times 2^{(SNDR - 1.76) / 6.02}\}$ [e.] Calculated through FoM_{SNDR} = SNDR + $10\log_{10}$(BW / Power)

V. CONCLUSIONS

In this paper, we presented an energy-efficient front-end integrated circuit chip employing an LFP-adaptive dynamic zoom-and-track scheme for high-resolution multi-channel subcortical recording systems. The implemented IADC in this front-end achieved the best FoM_{Walden} (107.9 fJ/c-s) and FoM_{SNDR} (162.1 dB), respectively, among the IADCs reported up to date in the neural recording front-ends. Also, among the state-of-the-art brain recording ADCs that adopted the zooming or tracking techniques similar to this work, the fabricated IADC showed the best FOMs. The performance of the front-end IC was successfully validated through bench-top tests and *in vivo* animal experiments. The dual-band subcortical signals were recorded with low noise of 8.2 μV_{rms}, and high-resolution of 11.3-bit ENOB at low power consumption of 6.8 μW. The inherent dual-band recording features can significantly reduce the post-processing hardware burdens for subcortical signal band separation. The presented front-end IC can be a suitable candidate for future low-power multi-channel high-resolution closed-loop neuromodulation systems.

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