

Gate-Tuning Silicon Microring Resonator Filters for On-chip Wavelength Division Multiplexing

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Abstract: We demonstrated efficient gate-tuning on-chip wavelength division multiplexing filters using a silicon microring resonator array driven by high-mobility titanium-doped indium oxide gates. It shows extensive wavelength coverage for entire channel spacing over 5 nm.

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1. Introduction

On-chip wavelength division multiplexing (WDM) enables high bandwidth and energy efficient optical interconnect systems for data centers and high-performance computing [1]. A typical on-chip WDM module can be formed by coupling an array of silicon microring resonators (Si-MRRs) with different resonant wavelengths (λ_{res}) to a single bus waveguide [2]. The λ_{res} of Si-MRR is very sensitive to temperature fluctuations and fabrication errors. Therefore, each Si-MRR in the WDM system requires precise control. However, λ_{res} of Si-MRR is commonly controlled by the thermal heater with the sacrifice of high-power consumption in the order of mW/nm [3], which poses a grand challenge for large-scale on-chip WDM systems. In contrast to the thermal-tuning of Si-MRR, the gate-tuning of Si-MRR integrated with a metal-oxide-semiconductor (MOS) capacitor can achieve wavelength tuning with near-zero power consumption [4]. We demonstrated a tunable Si-MRR heterogeneously integrated with indium tin oxide (ITO)/hafnium oxide (HfO₂)/Si MOS capacitor using a narrow microring waveguide to achieve a high electro-optic (E-O) tunability of 271 pm/V [5]. However, it had a low-quality factor (Q-factor) of 1000 due to the low mobility of the ITO gate, which restricts the channel density of the WDM module [2]. The Q-factor of the tunable Si-MRR was improved to 12000 by replacing the ITO gate with high-mobility titanium-doped indium oxide (ITiO) [6]. In this work, four tunable Si-MRRs are cascaded to form the on-chip WDM filters in the experiment. Each tunable Si-MRR is formed by ITiO/HfO₂/Si MOS capacitor with a reduced waveguide width of 300 nm. The on-chip WDM filters show the large wavelength coverage of the entire channel spacing with a low gate voltage and negligible power consumption.

2. Device Fabrication & Characterization of Individual Tunable Si-MRR

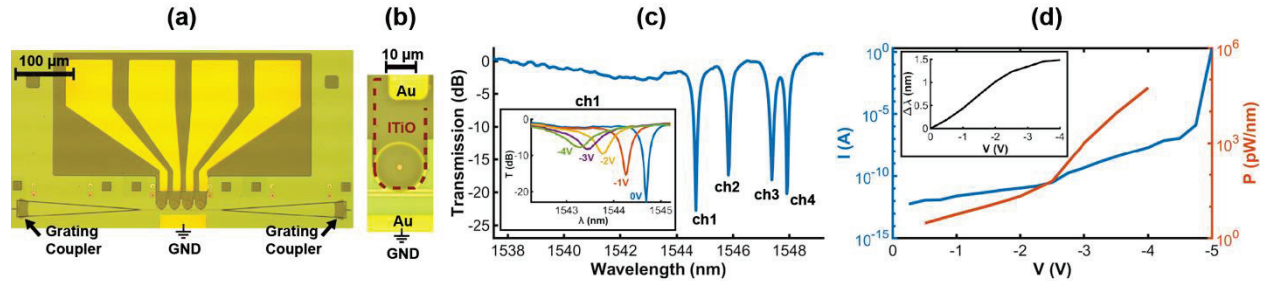


Fig 1 (a) Optical microscope image of the fabricated on-chip WDM filters consisting of four cascaded tunable Si-MRRs. (b) Zoom-in view of the individual tunable Si-MRR of the on-chip WDM filters. The dashed line highlights the ITiO gate. (c) Normalized transmission spectrum of the on-chip WDM filters with four resonant dips (four channels). Inset: Normalized transmission spectra of a tunable Si-MRR with different gate biases. (d) The leakage current of a tunable Si-MRR (blue). The wavelength tuning power consumption (red) is calculated with the wavelength tunability in the inset.

Fig. 1(a) shows the on-chip WDM filters consists of four cascaded tunable Si-MRRs with radii of 8.00 μm , 8.03 μm , 8.06 μm , 8.09 μm , respectively. Each tunable Si-MRR has a narrow Si waveguide width of 300 nm and a Si waveguide height of 250 nm with a 30 nm slab. In the active region, the 9 nm HfO₂ and 10 nm ITiO are conformally deposited on microring waveguides to form the ITiO/HfO₂/Si MOS capacitors, as highlighted by the dashed line in fig. 1(b). Fig. 1(c) shows the transmission spectrum of the on-chip WDM filters, and the four channels can be fitted into the free spectral range (FSR) of 11 nm. Besides, each tunable Si-MRR has a Q-factor of 5200. The inset in fig. 1(c) shows the example of ch1 that the λ_{res} has a blue shift when the negative voltages are applied to the ITiO gate. It has the gate-

voltage wavelength tuning range of 1.5 nm from 0V to -4V, and the maximum E-O wavelength tunability of 589 pm/V occurs at -1V, corresponding to $V_{\pi}L$ of 0.050 V·cm. The leakage current of the tunable Si-MRR with ITiO/HfO₂/Si MOS capacitor is measured, as shown in fig. 1(d). Moreover, the power consumption is calculated with the E-O wavelength tunability, as shown in the inset in fig. 1(d). It has a near-zero tuning power consumption from pW/nm to nW/nm. It is much more power efficient than thermal tuning (mW/nm) and suitable for the WDM modules.

3. Characterization of on-chip WDM Filters

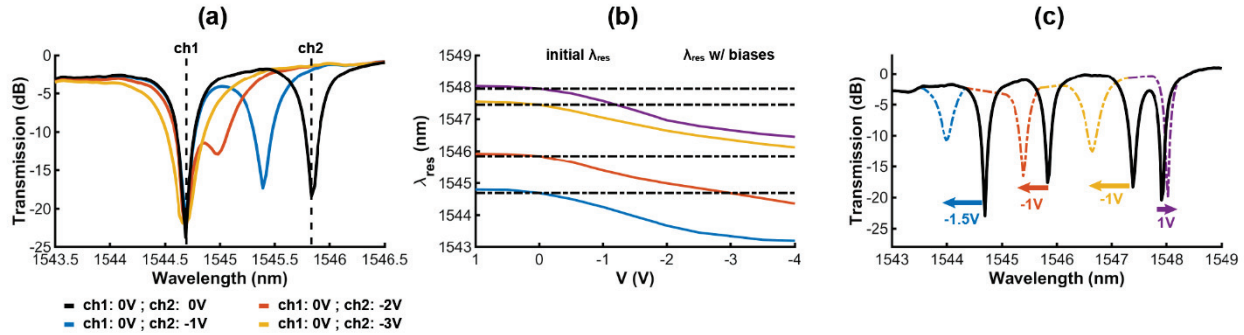


Fig. 2 (a) The black curve is the spectrum at 0V, and color curves show the different biases applied on ch2 in the on-chip WDM filters. (b) λ_{res} map with the applied biases. The dashed lines show the initial λ_{res} of channels, and the color curves show the λ_{res} of channels shift. (c) The non-uniform channel spacing is caused by fabrication errors (black solid curve). Apply gate bias on each channel (color dashed curves) to maintain uniform channel spacing of the on-chip WDM filters.

The λ_{res} of each channel can be electrically tuned to cover the entire channel spacing with gate voltage and negligible power consumption. For example, fig. 2(a) shows the λ_{res} of ch2 can be electrically tuned to ch1 with a gate voltage of -3V. Fig. 2(b) shows the λ_{res} tuning map of the on-chip WDM filters with gate voltages on each channel. The dashed lines represent the initial λ_{res} of each channel, and each channel can be tuned independently with the gate voltages, as shown in the solid curves. Therefore, gate biases can continuously tune the on-chip WDM filters across the 1543 to 1548 nm wavelength range. Additionally, the solid black curve in fig. 2(c) shows the initial spectrum of the fabricated on-chip WDM filters and shows the non-uniform channel spacing caused by fabrication errors. The non-uniform channel spacing can be compensated by applying gate voltages on each gate. The dashed color curves illustrate the gate bias can independently tune each channel, and different colors represent the shift of each channel. Finally, the WDM filters can be fine-tuned to achieve uniform channel spacing with applied gate biases.

4. Conclusion

In conclusion, we experimentally demonstrated on-chip WDM filters using a Si-MRR array driven by ITiO/HfO₂/Si MOS capacitors, showing an extensive wavelength coverage of the entire channel spacing. The on-chip WDM filters can be continuously tuned across the 1543 to 1548 nm wavelength range by gate biases with near-zero power consumption. It also showed that gate biases could fine-tune the on-chip WDM filters to maintain uniform channel spacing, which can be influenced by fabrication fluctuation.

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