Comparing the thermal performance and endurance of resistive and PIN silicon microheaters for phase-change photonic applications

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Abstract: Optical phase-change materials have enabled nonvolatile programmability in integrated photonic circuits by leveraging a reversible phase transition between amorphous and crystalline states. To control these materials in a scalable manner on-chip, heating the waveguide itself via electrical currents is an attractive option which has been recently explored using various approaches. Here, we compare the heating efficiency, fabrication variability, and endurance of two promising heater designs which can be easily integrated into silicon waveguides—a resistive microheater using n-doped silicon and one using a silicon p-type/intrinsic/n-type (PIN) junction. Raman thermometry is used to characterize the heating efficiencies of these microheaters, showing that both devices can achieve similar peak temperatures but revealing damage in the PIN devices. Subsequent endurance testing and characterization of both device types provide further insights into the reliability and potential damage mechanisms that can arise in electrically programmable phase-change photonic devices.

1. Introduction

The ability to reversibly control the phase and amplitude of light in both a nonvolatile and highly compact form-factor has been a key motivation behind current research into optical phase-change materials (PCMs) [1]. However, achieving this reversible control using a scalable integrated approach (i.e., electronic integration) has been more challenging for the optical community than it has for the electronics community. This can be attributed to the significant difference in area and volume between electronic PCM memristors (typically sub-50 nm in x-, y-, and z-dimensions) and photonic PCM devices (typically >1 μm in-plane, while ≤50 nm out-of-plane) which rules out directly applying current to the PCM itself. To reversibly switch these materials, high melting temperatures (~900 K) and fast quenching rates (~0.1 to 1 K/ns in the case of $Ge_2Sb_2Te_5$) are required which demands careful thermal engineering [2]. Additionally, the heat source used to switch the PCM should be optically transparent to prevent high insertion loss.

To address this challenge, several approaches have been demonstrated to enable scalable electrical control over optical PCMs for photonic circuits using waveguide-integrated resistive microheaters. This includes the use of transparent conductors [3]–[7], metallic heaters [8]–[10], graphene [11], [12], doped-silicon waveguides [13], [14], and silicon p-type/intrinsic/n-type (PIN) junctions [15]. For monolithic integration with silicon photonic platforms, microheaters based on single-doped silicon [13], [14], [16] and silicon PIN junctions [15], [17] are the most attractive choices as they can be fabricated using the same foundry-compatible processes commonly used to fabricate active silicon photonics devices (e.g., p-type/n-type (PN) modulators [18] and doped-silicon thermo-optic phase shifters [19]). While both designs can be easily incorporated into the standard silicon photonics process flow, these two approaches have their relative strengths and weaknesses. Using microheaters comprised of forward-biased silicon PIN junctions (here on referred to as "PIN microheaters") has the potential to have very low insertion loss as the waveguide can be patterned in the intrinsic region of the junction. However, the heating response of these devices can be quite sensitive to device dimensions and doping levels as we have observed in simulations [17] and show experimentally in this work. On the other hand, single-doped silicon microheaters (here on referred to as "doped microheaters") have simpler design considerations, which can be arbitrarily large, at the cost of higher applied voltages. A direct comparison between these two designs is challenging, since the reported devices from previous works have been processed separately under different process flows and doping conditions.

Here, we compare both doped and PIN microheater designs for switching PCMs which have been fabricated on the same chip together under the same conditions. This work investigates the steady-state heating response of PIN and doped microheaters using Raman thermometry and compares different PIN device geometries to further understand critical design parameters for these embedded heaters. Damage at the metal contacts was observed in the PIN devices after steady-state measurements (but not the doped devices), prompting us to explore the conditions under which this damage occurs. Endurance tests performed on doped and PIN microheaters revealed that for the same electrical power dissipation, doped microheaters exhibited less thermally-induced aging than PIN microheaters. Our results highlight the need for further research to improve the efficiency and lifetime of these microheaters for phase-change photonics applications.

2. Methods

PIN microheaters of differing intrinsic region lengths and widths were fabricated in a 90 nm CMOS line at the MIT Lincoln Laboratory [13], along with an array of n-doped microheaters with a constant geometry and varying levels of internal doping. All devices were fabricated on silicon-on-insulator wafers with a device layer of ~140 nm Si on 1 μm of SiO_2. While waveguides were not patterned on these devices, the thin silicon device layer has similar dimensions to partially etched silicon contacts in a typical rib waveguide process. To make electrical contact to the silicon, 200 nm Al metal contacts were deposited on top of a thin Ti/TiN adhesion/barrier layer. Finally, a thin 10 nm passivating layer of SiO_2 was uniformly deposited on the chip which is needed to provide electrical isolation for a PCM layer deposited on top of the microheater.

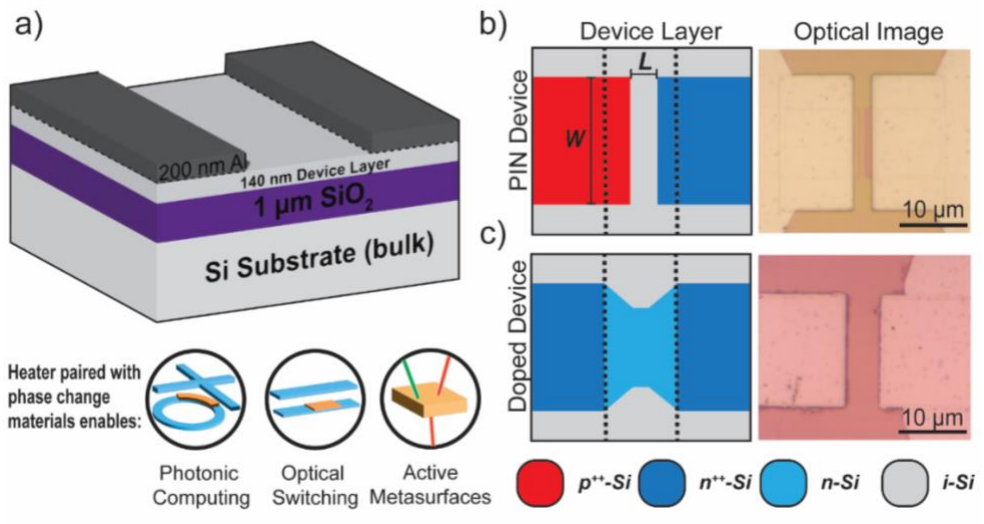

Fig. 1. Schematic views of the microheaters studied (10 nm passivating SiO_2 layer is omitted for clarity). All devices share the same layer structure (a), as shown above. Schematics of both the (b) PIN and (c) doped device layers are shown, with specific doping areas color coded as denoted. For the PIN device, specific W and L dimensions are denoted. Contact edges are represented by the dotted lines. The top down views of both devices are paired with optical images of pristine devices. The doped regions for the PIN device are visible in the optical image.

2.1 Device Details

We fabricated 12 unique PIN microheater geometries based on the design demonstrated by Zheng et al. [15] which have four different device widths (W= 5, 10, 15, and 20 μm), and three different lengths (L = 0.9, 1.2, and 1.5 μm) as indicated in Fig. 1. To keep the contact resistance of the PIN devices consistent between different geometries, the distance between the edge of the metal contacts and the edge of the doped regions was kept constant at 0.8 μm, so that the total distance between contacts was always equal to L + 1.6 μm. Additionally, the distance between each metal contact edge and the doped region edge was kept constant at 5 μm so that edge-to-edge, the contact was always W + 10 μm. The doped microheaters based on the design by Ríos et al. [13] had a fixed geometry with 5 μm between contacts and a tapered, lightly n-doped channel, as shown in Fig. 1. This channel tapers to a 10×0.5 μm^2 area which localizes the Joule heating to the PCM/waveguide region in the center. The metal contacts for the doped microheaters are separated by 16 μm from edge-to-edge. Due to their high uniformity and reliability, only two devices of each doping level are measured to characterize their thermal performance, see Supporting Information (SI) Fig. S1 and S2 for more details.

For the PIN microheaters, both the p^{++} and n^{++} regions of the device were heavily doped (~10^{20} cm^{-3}) to minimize contact resistance as well as maximize current through the device [17]. The intrinsic region was unaltered, and as such is henceforth referred to as *undoped*. For the doped microheaters, the two n^{++} regions used for ohmic contact were similarly heavily doped (~10^{20} cm^{-3}), while the interior n-regions were lightly doped at two different levels. Devices 1 and 2 were doped with n = 3 x 10^{18} cm^{-3}, while devices 3 and 4 were doped with n = 8 x 10^{17} cm^{-3}. Sheet resistances of each device measured can be found in section 2 of the SI.

2.2 Raman Thermometry

Raman thermometry has emerged as a way to measure material specific temperatures inside of samples by tracking the shift of Raman peaks as a function of temperature [16], [20]–[26]. To acquire Raman spectra of our microheaters, a Horiba XploRA PLUS Raman microscope with 473 nm excitation laser and long working distance 50×, 0.55 NA objective was used, resulting in a diffraction limited spot size of 1.18 μm. During measurements, we set the 473 nm laser to a power of 250 μW to ensure minimal excess heat was imparted into the devices through optical absorption. In order to convert the measured Raman spectra to the device temperature, we first calibrated the Si peak position versus sample temperature using a custom sample holder with built-in hotplate. More details regarding Raman spectra acquisition can be found in section 3 of the SI. The resulting calibration curve is shown in Fig. 2b and matches well with other results in the literature [20], [21], [24]. After calibration, the fabricated chip was wire bonded to a custom printed circuit board (PCB) to simplify electrical connectivity as shown in the inset in Fig. 2a. Devices were powered during the measurements using a Keithley 2450 Source Measure Unit (SMU) with up to 4 V for the PIN devices and up to 10 V for the doped devices. The resulting current-voltage (IV) characteristic of each device shown in Fig. 3a-b.

During temperature measurements, each applied DC voltage was maintained for 5 min to ensure both electrical and mechanical stability. Line scans were then performed to recenter and refocus the beam to account for any thermal drift present. Raman spectra were then obtained and fit using a similar peak-fitting and averaging method used for the calibration data, discussed in section 3 of the SI. However, at higher temperatures splitting of the Si peak occurred, as can be seen in Fig. 2d. This splitting is attributed to the higher temperature of the thin Si device layer (i.e., the Si layer in which the microheater is fabricated) relative to the bulk Si substrate beneath the SiO_2, causing the Si peaks from the different temperatures of these two layers to split [16]. These peaks were fitted using a double Lorentz curve, and device temperature was then calculated using the redshift of the proper Si peak using the calibration curve (Fig. 2b). This effect was not present in the generation of the calibration curve (Fig. 2c), since both the thin film Si and the underlying Si substrate were at the same temperature, resulting in one single Lorentz peak for the Si temperature.

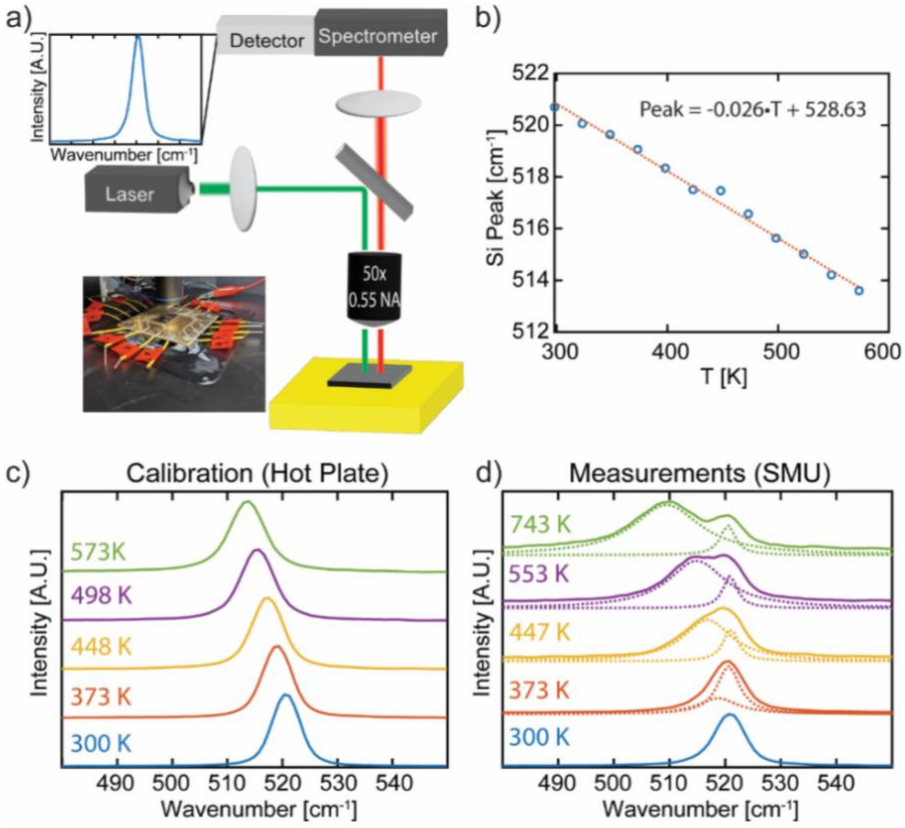

Fig. 2. (a) Schematic of a Raman Microscopy process, inset shows an image of the wire bonded test sample. (b) Calculated calibration curve of Si peak location against a known temperature using a hotplate. (c) Example of the Si Raman peak shifting at known temperatures, generated by the in-situ hot plate. (d) Demonstrating the peak splitting observed at higher temperatures for the devices while powered. This peak splitting does not occur during generation of the calibration curve, due to the consistent heat provided by the hot plate used.

3. Results

3.1 Temperature vs. Applied Power

The IV curves during Raman measurements for all devices are shown in Fig. 3a (PIN) and Fig. 3b (single doped). The measured current for each device is normalized by device width (W) to better facilitate comparison between the different device geometries. Fig. 3c-d shows the corresponding device temperature as a function of applied voltage and Fig. 3e-f shows the temperature as a function of applied power with temperature obtained using Raman thermometry. The PIN microheaters were grouped by device channel length (L), while the doped microheaters were grouped by the concentration of the lightly n-doped region between the contacts. Heating in these devices should be linearly proportional to applied power (quadratic with respect to applied voltage in Fig. 3c-d) due to Joule heating. Note, we expect the temperature-power dependence in the PIN devices to be slightly non-linear due to additional heating from carrier recombination at the P-I and I-N interfaces [17]. For each group of devices in Fig. 3e-f (3 groups of 4 PIN devices and 2 groups of 2 doped devices), we fit a linear trend

(quadratic for Fig. 3c-d) to compare the relative heating efficiency of the devices. While we expected that channel length would be the dominant parameter to influence current and heating in the PIN devices, we observed significant variability in both the IV and thermal heating efficiency. This appears to indicate that the PIN devices showed greater sensitivity to our fabrication process than specific device geometry.

The doped microheaters reveal nonlinear IV behaviors at higher applied voltages as can be seen in Fig. 3b. At lower applied voltages, like those available on-chip (<5 V), the IV behavior is linear as expected, resulting in the higher doped device reaching higher currents (and therefore, higher applied power) at a given voltage [13], [16]. However, as the voltage approaches the highest applied voltage (10 V), the current behaviors significantly deviated from the linear trend. In addition, the device temperatures converge as shown in Fig. 3d. Further insight on the device IV behaviors is given through various calculations performed on the measured data (see Fig. S3). We hypothesize that this is due to velocity saturation effects in silicon where the linear relationship between carrier velocities and electric field breaks down at high electric fields [27], [28]. Velocity saturation has been widely accepted to be driven by carrier scattering with optical phonons [29]–[32], where once an electron's kinetic energy exceeds the optical phonon energy, it scatters with the lattice and generates an optical phonon, causing its velocity to drop. This puts an effective cap on the carrier velocities seen in semiconductors, leading to the observed current saturation observed at high fields [29]–[32]. To confirm this, we measured the IV curves for different channel lengths and doping levels. Normalizing the voltage by channel length gives us a saturation field of ~1 x 10^4 V/cm which is consistent with literature [27], [30] (see Fig. S4). In our devices, this effect would imply that there is a nonlinear increase in phonon production above a certain applied voltage (E-field), resulting in increased heating rates.

Interestingly, we observe that the devices with a lower doping level (8×10^{17} cm^{-3}) reach higher temperatures than the devices with higher doping (3×10^{18} cm^{-3}) for the same applied power above a certain threshold (see black dashed line in Fig. 3f). This indicates that the devices with lower doping become more efficient heaters above this threshold which happens to occur at the onset of velocity saturation (around ~7 V). One possible explanation for this effect is a higher phonon generation rate per carrier for the devices with lower doping levels. If we consider the systems below the saturation region, we know that mobility decreases with increasing doping (μ_n is ~2× lower at room temperature for the higher doped devices [33]). Since the lower doped devices have higher mobilities and below velocity saturation $v_{drift} = -\mu_n E$ is a valid assumption, we can thus conclude under these assumptions that the average carrier kinetic energy in the lower doped device is higher ($E = \frac{m^* v_{drift}^2}{2}$). We further hypothesize that as the E-field continues to increase with increasing voltage, the kinetic energy of the carriers in both devices also increase, but the lower doped devices would then be able to reach the optical phonon scattering regime at lower fields.

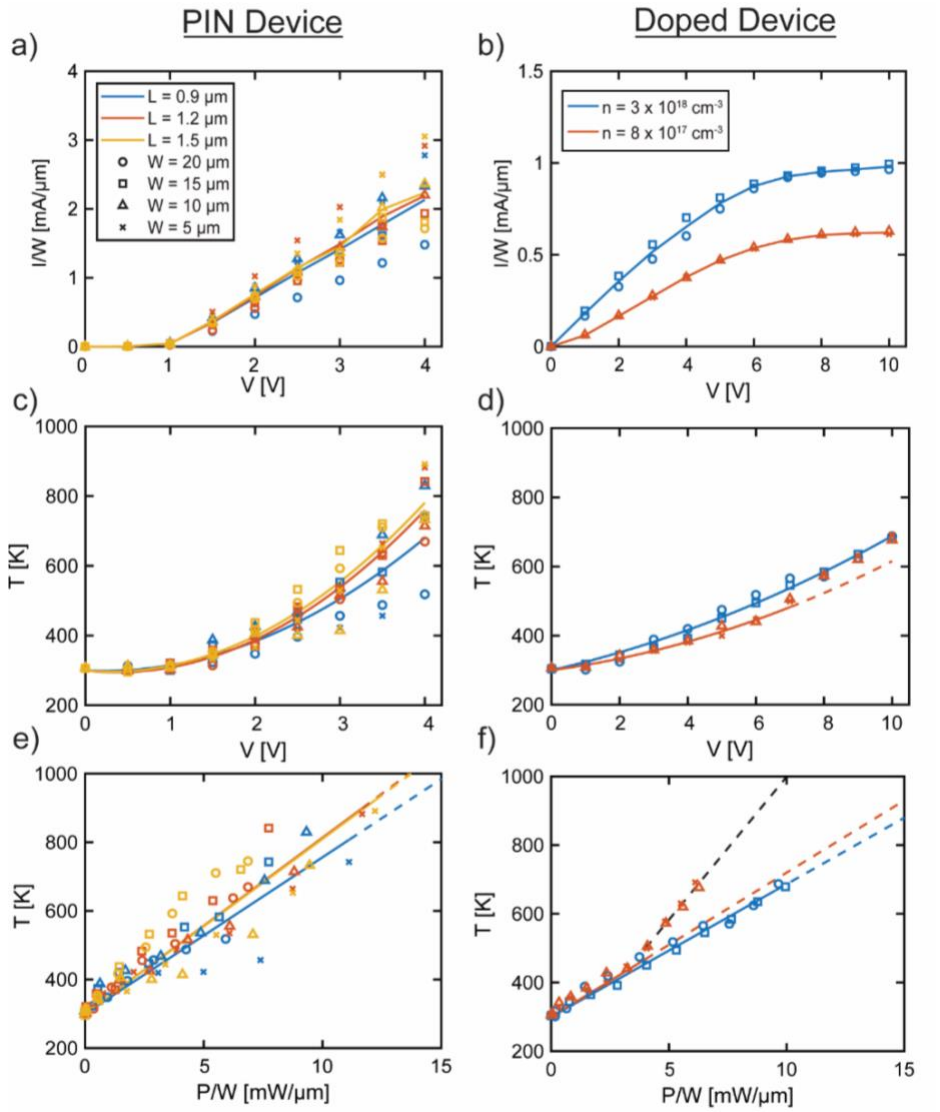

Fig. 3. IV performance of the (a) PIN devices, and (b) doped devices. The solid lines are average IV performance, one for each length of the PIN devices, and one for each doping of the doped devices. Data points shown on both are for specific devices. (c) and (d) Results of the Raman Thermometry measurements showing the calculated device temperature vs. applied voltage for (c) PIN devices and (d) doped devices. The thermal fits assume a second order polynomial ($T = T_0 + aV + bV^2$) to account for both Joule heating and temperature-dependent device resistance. For the $n = 8 \times 10^{17}$ cm^{-3} devices in (d), continuation of the expected quadratic fit is given by the dashed orange line, showing the deviation from this behavior above 7 V. Results of the Raman Thermometry measurements shown vs normalized applied power for (e) PIN devices and (f) doped devices. Linear trend lines are fit for the data for each device (both the 1.2 and 1.5 µm long devices in (e) had similar trendlines, resulting in overlapping lines). For the $n = 8$ x 10^{17} cm^{-3} devices in (f), the deviation from expected Joule heating above 7 V is indicated by the dashed black line as a guide to the eye, with the expected linear trend continuing using the dashed orange line.

As can be seen in Fig. 3f, there is significant overlap in the device heating performance as a function of the applied power below the saturation region. However, once the lower doped device reaches velocity saturation conditions (4 mW/μm at 7 V), the amount of heat generated greatly increases. As the E-field continues to increase beyond this point, our hypothesis implies the electrons in the channel generate optical phonons at a higher rate, increasing the amount of heat generated. The trend from pre-saturation conditions is continued using the dotted orange line to highlight this abrupt increase in heat generation in Fig. 3d and 3f.

Overall, the PIN microheaters can reach higher temperatures at much lower applied voltages and total power, as shown by Fig. 3c-d. However, when the results are normalized by device width the doped microheaters have a similar power efficiency, as shown in Fig. 3e-f. Additionally, the doped devices show a much larger degree of consistency between devices of the same doping level. Compared to the large variance in both thermal performance and IV response for the PIN devices (shown in Fig. 4a and Fig. 1c, respectively), it appears that the doped microheaters are much less sensitive to fabrication imperfections and could lead to improved reliability and yield. The higher doped devices behave extremely consistently with each other, as do the lower doped (see SI Fig. S1 and S2). These device pairs only differ through their n-channel doping level as discussed above.

3.2 Endurance Testing

After performing Raman thermometry, we observed that holding the device at high temperatures and current densities for several minutes cause significant damage to the p^{++} terminal of the forward-biased PIN devices. This was consistently observed across the majority of the PIN devices tested as depicted in Fig. 4a. However, this damage was not observed in the doped devices. One possible explanation for this could be due to a larger separation of the metal contacts from the center region of highest temperature in the case of the doped devices. For the PIN devices, we attributed the cause of this damage to the relatively low melting temperature of the metal contacts (Al) which are exposed to high temperatures over several minutes. To test this hypothesis and further understand the full impact of this damage on the device performance as well as the extent of the damage, we performed further characterization and testing. The damaged devices were imaged using scanning electron (SEM) and atomic force microscopy (AFM). AFM topographic scans revealed that damaged regions of the electrode indeed matched the ~200 nm thickness of the deposited Al layer (Fig. 4c-d). SEM images of the device (shown in Fig. 4b) also appear to show removal of the Al layer while the Ti/TiN adhesion and barrier layers remain undamaged after steady-state testing.

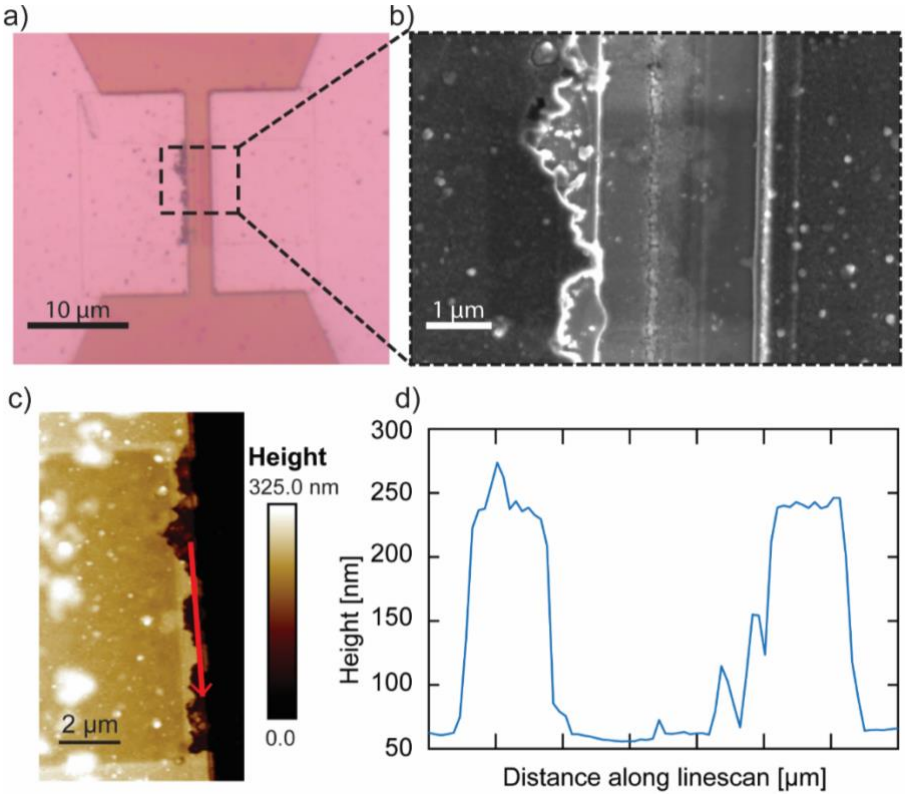

Fig. 4. Example of damage observed during Raman process. (a) shows a device after being powered. Devices were then characterized by (b) Scanning electron microscope image showing the contact disappearance. In addition, brighter spots in the midst of the channel likely indicate that the 10 nm SiO_2 passivation layer has suffered ablation, allowing the underlying thin-film Si layer to shine brighter. The slightly darker area denotes carbon contamination from a previous, higher magnification scan. (c) Atomic force microscope image of the device, the red line depicts the path of a line scan. The results of which (d) show the resulting step size is ~200 nm, implying the contact edge has completely delaminated and disappeared.

While steady-state operation can provide insights into device aging, these microheaters are intended to operate under pulsed conditions to reversibly switch optical PCMs. To investigate the potential effects that pulsed operation may cause on device performance and to observe which pulse conditions may cause similar electrode damage, endurance testing was carried out on new devices from both types of microheater. For both the PIN and doped microheaters, a width of $W = 10$ µm was chosen ($L = 0.9$ µm for the PIN device, $n = 3 \times 10^{18}$ cm^{-3} for the doped device). During testing, up to 10 million pulses were applied to a test device, with varying pulse widths of 1 µs, 10 µs and 1 ms. To reproduce the conditions causing the damage during the Raman measurements, we applied 4 V pulses to the PIN devices. To also ensure the same applied power was used for both PIN and n-doped devices, we calculated an applied power of 7.4 mW/µm for the PIN microheater, when normalized by device width. The same applied power corresponds to a pulse amplitude of 8 V for the doped devices, which was then used during testing. A pulse duty cycle of 50% was used for each test.

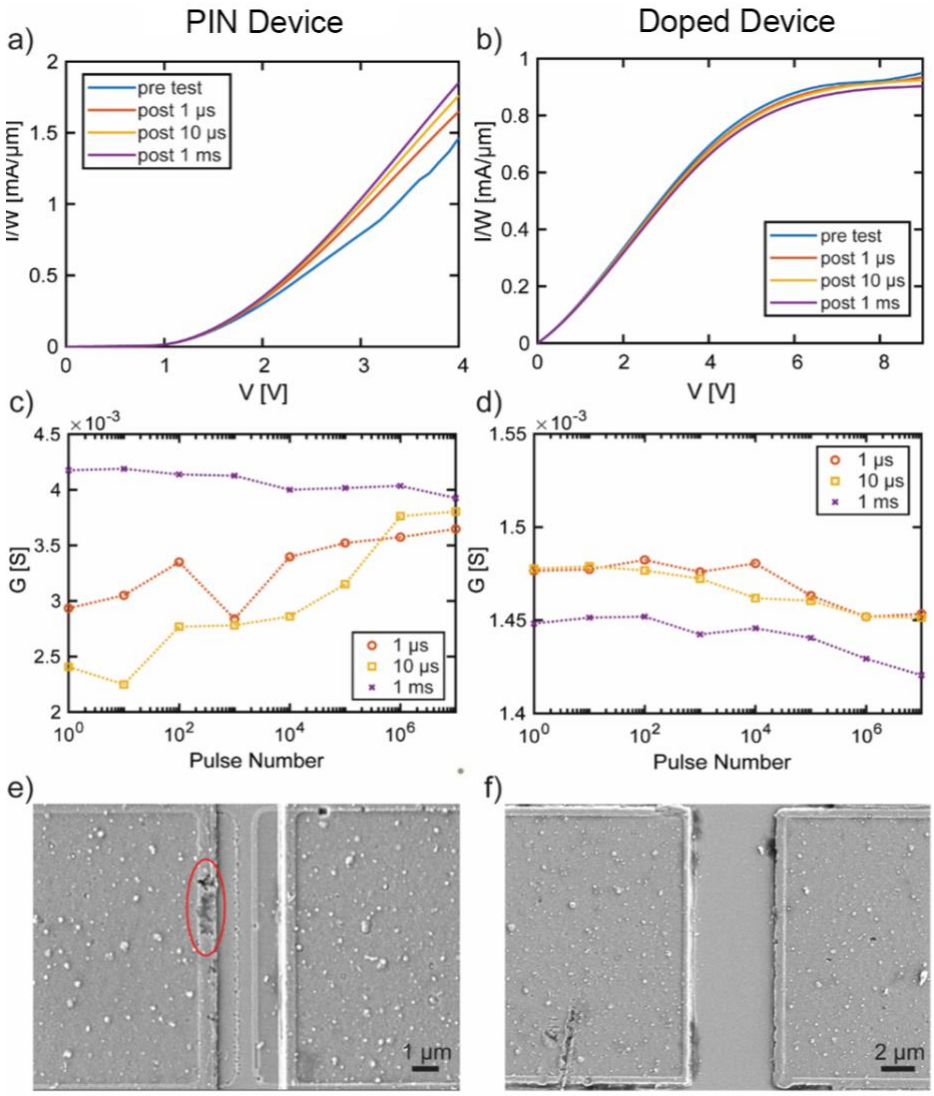

Fig. 5. Results of endurance testing of the devices. IV sweeps of the (a) PIN and (b) n-doped device taken after each set of pulse widths. (c) and (d) Device conductivity was measured after every decade of cycling. SEM images of the (e) PIN and (f) doped devices post testing showing the onset of damage in the PIN microheater (highlighted area), and the lack thereof in the doped device.

At the end of the 10 million pulse test for each pulse width, an IV sweep was performed (Fig. 5a-b) and the device was inspected under an optical microscope. In addition, after each decade a short 400 ns long read pulse was applied to characterize the electrical performance of the stressed device (Fig. 5c-d). Visible damage was not observed on the PIN device until after the 1 ms pulse width cycle, shown in Fig. 5e. No damage was observed in the doped device after endurance testing (Fig. 5f) which agreed with our observations from Raman thermometry experiments. Although the damage did in fact occur in the PIN device as shown in Fig. 5e, the electrical performance of the device as measured by IV was not significantly affected after cycling beyond a moderate increase in forward bias current.

4. Discussion

While the initial goal of this work was to compare different intrinsic region lengths of PIN diodes, it became abundantly clear that a more important parameter was device width, *W*. With this in mind, temperature versus power results were then normalized by device width, as the smaller (low *W*) devices all consistently outperform the larger (high *W*) devices due to the smaller amount of volume being heated. In addition, appears that the smaller *L* devices heat much less efficiently than the wider devices, as evidenced by the lower slope of the trend line in Fig. 4a. This under performance is likely due to the lower volume of material being heated, as well as the closer proximity of the contacts which act as heat sinks. In this steady state measurement, both of those factors result in lower total temperatures, although their performance in pulsed applications are projected to be better in terms of heating speed then their wider companions [17].

As can be seen through the spread of points in Fig. 4a, there is still a large spread among the different PIN devices (likely due to the high requirements for consistent fabrication of these devices). In comparison, the doped microheater devices heat more consistently than the PIN devices, with a similar efficiently depending on the interior region doping level. However, it is worth emphasizing that PIN heaters still offer a higher potential for efficient heating at lower voltages, as evidenced by Fig. 3, which is ideal for typical on-chip voltages (i.e., <5 V).

We have also demonstrated unexpected behaviors of the doped heaters in the current saturation range of operation exhibited at higher voltages (Fig. 3f). We hypothesize the increased emission rate of optical phonons in devices operating at current saturation led to a second, more efficient heating regime in these devices. Lower doped devices are able to reach this regime at lower powers, therefore outperforming higher doped devices (Fig. 3f). However, for applications that are limited to on-chip voltages (<5 V) we find that higher doped devices reach higher temperatures at lower voltages (Fig. 3d).

When comparing PIN microheaters with doped resistive microheaters, it is important to note some relative advantages and disadvantages of both designs. First, while not explored here, we do expect the maximum intrinsic channel length to be limited to sub-10 μm to operate at reasonable applied voltages. This makes doped microheaters more appropriate for scaling to larger area devices such as reconfigurable metalens pixel arrays. Secondly, to prevent electromigration, RF pulses can be used to heat doped microheaters which is an impossibility for microheaters based on PIN diodes. Finally, it seems that fabricating consistent embedded PIN devices is more challenging than doped devices, both in regard to mitigating the large degree of randomness observed in the IV performance of our devices and further optimizing device endurance. However, the potential for operating at low applied voltages (<5 V) with low optical insertion loss warrants further improvements and optimizations. In terms of optical performances, PIN and doped microheaters can offer comparable optical attenuation properties, (~0.02–0.4 dB/μm for devices of intrinsic region lengths 0.9-1.5 μm [17] compared to 0.03 dB/μm for doping levels like those found in [13]). The PIN devices tested here compared promisingly with single doped devices for the dimensions tested. The final results of the comparison are summarized below in Table 1. With more improvements in both device structure and fabrication methods, PIN heaters should have a bright future.

Table 1 – Comparison of PIN and Doped Devices

	PIN Devices	**Doped Devices**
Max Temp. (<10 mW/μm)	829.7 K (9.32 mW/μm)	687.4 K (9.65 mW/μm)
Max Temp. (4 V)	891.269 K	419.4 K
Power efficiency[a]	45.6–51.3 K·μm/mW	38.7–42.02 (83.28[b]) K·μm/mW
Endurance	Medium	High
Sensitivity to fabrication	High	Low
Footprint	12.5–62 μm^2	25–100 μm^2
Optical Losses	0.02–0.4 dB/μm [17]	0.03 dB/μm [13]

[a]Values from fitted P-T trends.

[b]Value from observed increase in lower doped samples post velocity saturation.

5. Conclusion

This work has studied the heating response of two different types of embedded doped Si heaters, PIN and single doped devices. Specifically, the geometric effect of the intrinsic region length, and device width for PIN diodes was investigated. The PIN diodes were found to have a larger spread in device operation then expected, and as such are less consistent then the single doped microheaters, as fabricated. Both these devices were held at high DC power, and their steady state temperatures measured through Raman Thermometry methods, and it was found that both types of devices can reach significantly high temperatures under similar applied power densities. We also revealed unexpected heating performances at higher applied powers, showing lower doping can result in more efficient heating in single doped devices. During measurements damage was observed on the positive contacts of each PIN device, notably not at all on the single doped devices, and the impact of this damage on electrical performance was investigated through endurance testing. The endurance testing revealed that while damage does begin to occur at high enough ON time (10 million 1-ms-long pulses) the damage did not affect device operation. From this investigation, it was concluded that both devices have high potentials for large scale embedded heaters for photonic devices, but PIN devices of this nature might require a higher investment in device design and fabrication processes, while single doped microheater devices offer more reliable operation at the cost of requiring higher operating voltages.

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Disclosures

The authors declare no conflicts of interest.

Data Availability

Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Supplemental Document

See Supplement 1 for supporting content.

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