Robust Avalanche in 1.7 kV Vertical GaN Diodes with a Single-Implant Bevel Edge Termination

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***Abstract*—This work demonstrates a novel junction termination extension (JTE) with a graded charge profile for vertical GaN p-n diodes. The fabrication of this JTE obviates GaN etch and requires only a single-step implantation. A bi-layer photoresist is used to produce an ultra-small bevel angle (~0.1°) at the sidewall of a dielectric layer. This tapered dielectric layer is then used as the implantation mask to produce a graded charge profile in p-GaN. The fabricated GaN p-n diodes show a breakdown voltage (*BV*) of 1.7 kV (83% of the parallel-plane limit) with positive temperature coefficient, as well as a high avalanche current density over 1100 A/cm^2 at *BV* in the unclamped inductive switching test. This robust avalanche is ascribed to the migration of the major impact ionization location from the JTE edge to the main junction. This single-implant, efficient, avalanche-capable JTE can potentially become a building block of many vertical GaN devices, and its fabrication technique has wide device and material applicability.[1]**

***Index Terms*— power electronics, gallium nitride, avalanche, junction termination extension, breakdown voltage, circuit test**

I. Introduction

Gallium nitride (GaN) power devices have been commercialized up to 900 V. Vertical GaN devices are under extensive development for kilovolt applications [1]. Edge termination is an essential building block of any vertical power device to laterally spread the crowded electric field (E-field) at the electrode edge and enable high breakdown voltage (*BV*).

Several edge termination designs, including field plate [2], [3], deep or bevel mesa [4]–[9], isolation implant [10], guard ring [11]–[13], junction termination extension (JTE) [14]–[19], and their combinations, have been demonstrated in vertical GaN p-n diodes. Among these designs, JTE is of great interest as it has become the mainstream choice in industrial Si and SiC devices [20]. State-of-the-art JTEs are featured by a decreased charge density away from the active region, which allows for higher efficiency and broader design space as compared to the single-zone (non-graded) JTE [20]–[22].

The fabrication of GaN JTEs is more challenging than SiC and Si, due to difficulties in p-type implantation or diffusion. Current GaN JTE fabrication mostly relies on the compensation implant into an epitaxial p-GaN to form a single-zone JTE [14], [16], which suffers from small process windows (e.g., requiring precise control of the implant depth down to 10 nm [16]). On the other hand, the graded charge profile has only been enabled by the beveled etch [5], [9] instead of implantation in GaN.

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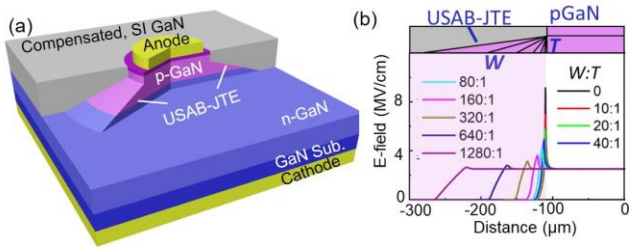

Fig. 1. (a) 3D schematic of the JTE p-n diode. (c) Simulated E-field profile in the JTE region with different JTE bevel angles at the voltage of -1.7 kV.

In addition to high *BV*, edge termination is also the key to enabling avalanche capability, which allows devices to pass a high avalanche current (I_{AVA}) at *BV*. While a vital signature of avalanche is a positive temperature coefficient of *BV*, the robust avalanche for passing the high I_{AVA} has to be tested by inductive switching circuits [23]. Among various GaN terminations, such a robust avalanche has only been reported in a single-zone JTE [19] and two bevel-etched terminations [6], [9].

This work demonstrates a novel, etch-free, single-implant GaN JTE that has a graded charge profile and enables the circuit-level avalanche. A new process is developed to produce a tapered dielectric layer with an ultra-small bevel angle, which serves as the mask for nitrogen implantation to compensate the p-GaN. The produced bevel JTE is embedded in bulk GaN and far from the surface. Therefore, its effectiveness is insensitive to the interface charge commonly introduced by the passivation. An on-wafer avalanche circuit test is performed, and the key physics is unveiled by physics-based TCAD simulation.

II. JTE Design and Fabrication

Fig. 1(a) shows the 3D schematic of the proposed JTE, the ultra-small-angle bevel JTE (USAB-JTE). The uncompensated p-GaN at the device edge exhibits a wedge shape with a large ratio between the JTE width (*W*) and thickness (*T*). The wafer comprises 20 nm p^{++}-GaN ([Mg]: 10^{20} cm^{-3}), 500 nm p-GaN ([Mg]: 10^{19} cm^{-3}) and 10 μm n-GaN ([Si]: 10^{16} cm^{-3}), grown by Enkris Semiconductor Inc. on a 2-inch GaN substrate from Nanowin Co., Ltd. The net donor concentration (N_D-N_A) in n-GaN is 8×10^{15} cm^{-3} as revealed from C-V measurements.

TCAD simulations based on the models in [17] are used to quantify the impact of the bevel angle on the peak E-field. Fig. 1(c) shows the simulated E-field profile along the junction for the JTEs with various *W/T* ratios. A higher ratio allows the peak E-field to be more effectively suppressed. This trend agrees

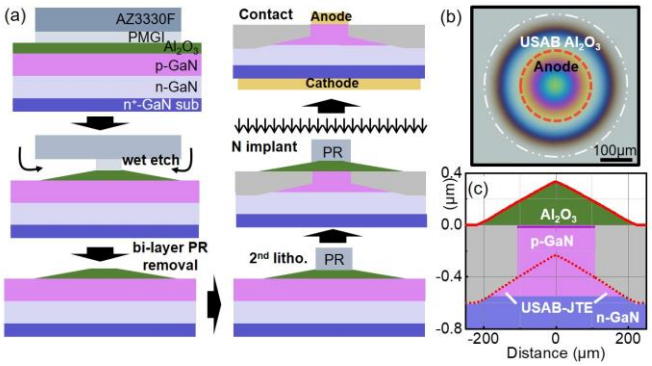

Fig. 2. (a) Schematics of the main fabrication steps of the JTE p-n diode. (b) Top-view microscopic image of the fabricated USAB Al_2O_3 mask. (c) Surface profile of Al_2O_3 measured by Dektak (solid red line) and the simulated profile of the uncompensated p-GaN (dashed line) from Monte Carlo simulations.

with the simulation results in [24] for a bevel-etched GaN JTE.

Fig. 2(a) illustrates the main fabrication steps. A 480 nm Al_2O_3 layer is first deposited by atomic layer deposition (ALD) at 300 ºC. A bilayer photoresist (PR) consisting of 2 μm PMGI and 3 μm AZ3330F is then used in the lithography. After baking at 200 ºC, the sample is immersed in a 2.38% TMAH solution to fully etch Al_2O_3 in the PR-uncovered region. Under the PR, a very large lateral undercut is formed, as the etch rate of PMGI (~750 nm/min) is much higher than Al_2O_3 (~1.2 nm/min). A very small bevel angle is thereby formed at the Al_2O_3 sidewall. The bevel angle is controlled by the ratio between the lateral (PMGI) and vertical (Al_2O_3) etch rates.

Fig. 2(b) shows the top-view microscopic image of the USAB Al_2O_3 mask after 7 hours of wet etch. The circular interference fringes suggest the isotropic dimension. This Al_2O_3 mask is slightly over-etched to showcase the large process latitude, where the PMGI is fully etched in this device (it retains in larger-area devices) and the boundary of Al_2O_3 is smaller than PR (white dashed line). As shown from the surface profile measured by a Dektak stylus profilometer (Fig. 2(c)), Al_2O_3 shows a small tapered angle (0.09º) with a very smooth surface. As compared to the prior tapered PR formed by the greyscale lithography [21] and reflow technique [5], [9], our Al_2O_3 mask shows a smoother surface, smaller angle, and superior hardness for implantation. At the edge of the p-GaN active region, the Al_2O_3 thickness is 190 nm (Fig. 2(c)).

This tapered Al_2O_3 is then used as the mask for nitrogen (N) implantation. The implantation design aims at a full and partial p-GaN compensation in the un-masked and masked region, respectively. Here a five-energy implantation with energies of 25, 80, 150, 240, and 320 keV and doses of 8.54, 1.51, 1.36, 5.81, and 4.48×10^{12} cm^{-2} is used to produce a box-like profile. Monte Carlo simulations [25] confirms a compensation depth (N defect density higher than [Mg]) of 400 nm and 610 nm with the 190 nm Al_2O_3 mask and without mask, respectively. In this way, the small bevel angle in the Al_2O_3 mask is transferred to the un-compensated p-GaN, forming a USAB-JTE with T of ~120 nm and W of ~75 μm (Fig. 2(c)).

Before this implantation, a PR is coated on top of the anode region for protection. Finally, anode and cathode are formed. A control device with only the through p-GaN implant isolation is also fabricated. The radius of the anode metal and p-GaN active region is 100 μm and 110 μm, respectively, for all diodes described in this paper.

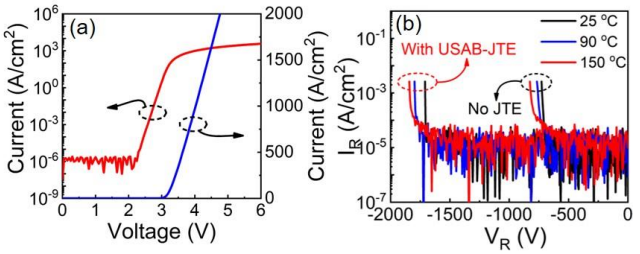

Fig. 3. (a) Forward I-V characteristics of the JTE p-n diode. (b) Reverse I-V characteristics of the diodes with and without the JTE at various temperatures.

We finally discuss the manufacturability and tunability of the above dielectric mask process. The Al_2O_3 thickness (480 nm) is redundant to show a large process window. An Al_2O_3 slightly thicker than the inner edge of the mask (190 nm) is sufficient. Also, the deposition rate can be much higher using by plasma-enhanced chemical vapor deposition (PECVD) [26], further allowing for reductions in the deposition and etch time.

A wide range of dielectric bevel angles can be produced by tuning the lateral or vertical etch rate. The former can be raised by lowering the PMGI baking temperature. The bevel angle is found to be 0.09º to 0.03º for baking at 200 ºC and 160 ºC, respectively. The vertical etch rate can be adjusted by varying the TMAH concentration or dielectric materials. For example, the TMAH etch rate of PECVD SiO_2 and SiN_x is 0.07~0.45 nm/min [27] and 0.08~1.3 nm/min [28], respectively.

III. Device Characterization and Circuit Tests

Fig. 3(a) shows the forward I-V characteristics of the JTE p-n diodes, revealing an on/off ratio >10^9 and a turn-on voltage similar to the GaN's bandgap. As the JTE has high resistivity (due to small T), current spreading is very limited, as confirmed by simulations. The current density is normalized to the active region, rendering a specific on-resistance (R_{ON}) of 0.8 mΩ·cm^2.

Fig. 3(b) shows the reverse I-V characteristics of the diodes with the USAB-JTE and without it (i.e., only with implant isolation). The current compliance in the measurement is 1 μA. The USAB-JTE is effective in boosting the BV from 700 V to >1.7 kV at 25 ºC (>1.8 kV at 150 ºC). The breakdowns of

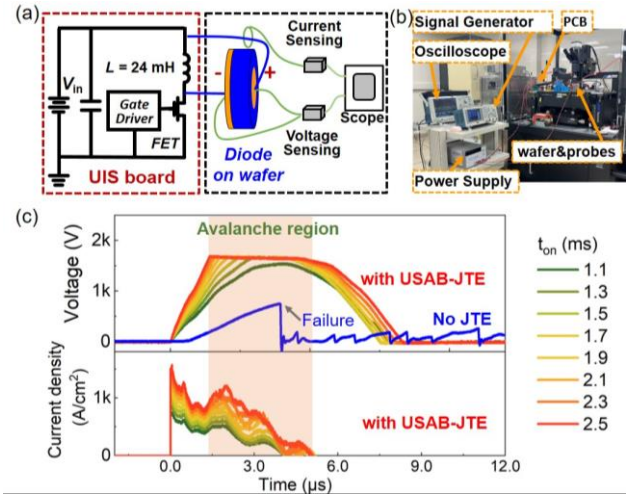

Fig. 4. (a) Schematic and (b) photo of the UIS test setup for on-wafer devices. (c) UIS waveforms of the diodes with and without JTE under various t_{on}.

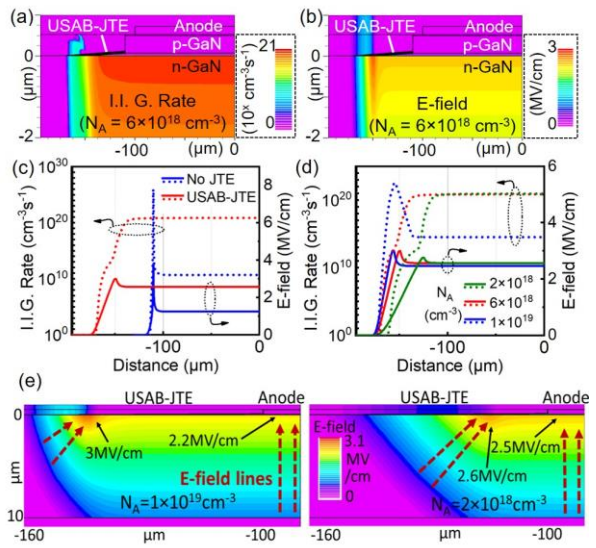

Fig. 5. Simulated contours of (a) I. I. generation rate and (b) E-field in a JTE diode at -1.7 kV. (c) The extracted profiles of the I. I. generation rate (dashed lines) and E-field (solid lines) along the junction of a JTE diode and a non-JTE diode near their respective *BV*. (d) Extracted profiles of the I. I. rate (dashed lines) and E-field (solid lines) along the junction of the JTE diodes with three different N_A, all at -1.7 kV with the JTE geometry identical. (e) Simulated E-field contours in the JTE diodes with two N_A in p-GaN, both at the initiation of avalanche (I_{AVA}=1 μA). Exemplar E-field lines are shown. Avalanche occurs when the I. I. integral along an E-field line reaches unity.

both devices are non-destructive and repeatable as well as possess a positive temperature coefficient (η_T), suggesting the dominant role of the impact ionization (I. I.) in the breakdown. Note that a positive η_T may not ensure the robust avalanche to pass high I_{AVA}, as the avalanche could occur locally or be intervened by trap-filling [17].

Unclamped inductive switching (UIS) circuit test is a routine method to validate the high I_{AVA} avalanche capability of power devices. In the UIS test, device is first ON to charge the inductor. Device is then turned-OFF, and the inductive energy is dissipated in the device through avalanching. The working principle and circuit design are detailed in [19]. Here we develop an on-wafer UIS test platform, which directly connects the UIS board to the probe station (Fig. 4(a)-(b)) to enable the test of the as-fabricated devices without the need for packaging.

Fig. 4(c) show the voltage and current waveforms of the diodes with and without the USAB-JTE in the UIS tests with an increased device-ON time (t_{ON}) and inductive energy. The JTE diodes show classic avalanche waveforms with the voltage clamped at the avalanche *BV* and the current reduced to zero. At 1.7 kV, the I_{AVA} is higher than 1100 A/cm^2. In contrast, the diode without JTE shows a destructive failure at the capacitive charging phase. This failure behavior is identical to that of the non-avalanche device under the UIS test [29], suggesting the diodes without JTE have no capability to dissipate a high I_{AVA}.

TCAD simulations are performed using the Selberherr I. I. model with the experimental I. I. coefficients in [30]. Fig. 5(a) and (b) show the simulated contours of the I. I. generation rate and E-field in the JTE diodes with an acceptor concentration (N_A) of 6×10^{18} cm^{-3}, considering a doping efficiency (N_A/[Mg]) of 60~70% reported in p-GaN due to the M-H complexes that cannot be fully broken in the annealing [31]. As shown, while the peak E-field is at the JTE outer edge, the peak I. I. location moves to the active device region. This guides the I_{AVA} to flow through the active region, allowing for a high I_{AVA}.

TABLE I. Comparison of edge termination technologies that enable avalanche vertical GaN p-n diodes with a *BV* over 600 V.

Structure	Ref	Avalanche		Fabrication		Efficiency	
		circuit [a]	I-V [b]	GaN etch	implant	BV_{AVA} (kV)	BV_{AVA}/BV_{PP}^{AVA}
USAB-JTE	This work	Yes	Yes	0	1	1.7	83%
JTE [c]	[19]	Yes	Yes	0	1	1.58	79%
Bevel mesa + FP	[6]	Yes	Yes	1	0	2.8	85%
Bevel mesa + FP	[3]	No	Yes	1	0	2.2 [d]	62% [d]
Deep mesa	[4]	No	Yes	1	0	0.88	57%
Deep bevel mesa	[9]	Yes	Yes	1	0	0.835	86%
Single-zone JTE	[14]	No	No	0	1	2.4 [e]	87%

[a] UIS circuit tests; [b] I-V characteristics showing a positive temperature coefficient of BV; [c] detailed implant design not disclosed; [d] highest BV with positive temperature coefficient reported in [3]; [e] avalanche claimed based on light emission during the I-V sweep.

Fig. 5(c) shows the simulated profiles of the I. I. generation rate and E-field in the diodes without JTE (along the junction), revealing crowded I. I. and E-field both at the device edge. The crowded I. I. can lead to serious localized carrier congregation. The locally aggregated carriers are difficult to be removed efficiently and result in the formation of high E-field spikes. This can lead to device failure before I_{AVA} grows and explains the limited I_{AVA} experimentally observed.

Finally, we use simulation to explore the impact of N_A on the avalanche capability of JTE diodes. As shown in Fig. 5(d), as N_A increases to 10^{19} cm^{-3}, the peak I. I. location moves from the active device region to the JTE's outer edge. This is because, at high N_A, the high peak E-field in the JTE region makes the I. I. integral first reach the unity (see Fig. 5(e)), leading to a localized avalanche. At lower N_A, the more uniform E-field enhances the ionization integral along the E-field lines in the active region, rendering a spatially uniform avalanche.

Table I benchmarks the key metrics (robustness, fabrication, efficiency) of the avalanche-capable edge terminations reported in vertical GaN devices. Here the efficiency is defined as the ratio between the device BV_{AVA} and the parallel-plane BV_{AVA} limit (BV_{PP}^{AVA}). BV_{PP}^{AVA} is calculated from the punch-through E-field profile: $BV_{PP}^{AVA} = E_C^{AVA}t - qN_Dt^2/2\varepsilon$, where ε is GaN's permittivity (10.4 dielectric constant used for c-axis); E_C^{AVA} is avalanche critical E-field of GaN, which can be calculated by $E_C^{AVA} = 2.81/(1 - 0.205log_{10}(N_D/10^{16}))$ [32] fitted by the I. I. coefficients in [30]. The comparison shows that our USAB-JTE simultaneously achieves the circuit-level avalanche, simple etch-free fabrication, and high efficiency in vertical GaN.

IV. Summary

We demonstrate an etch-free, single-implant USAB-JTE that enables the circuit-level avalanche in vertical GaN devices. This JTE relies on a new fabrication process to form a USAB, tapered dielectric mask for implantation. This process has wide material and device applicability. The USAB-JTE shows good potential as a building block for a variety of high-voltage, avalanche-robust vertical GaN devices.

REFERENCES

[1] Y. Zhang, F. Udrea, and H. Wang, "Multidimensional device architectures for efficient power electronics," *Nat. Electron.*, vol. 5, no. 11, Art. no. 11, Nov. 2022, doi: 10.1038/s41928-022-00860-5.

[2] K. Nomoto, Z. Hu, B. Song, M. Zhu, M. Qi, R. Yan, V. Protasenko, E. Imhoff, J. Kuo, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, "GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ-cm2: A record high figure-of-merit of 12.8 GW/cm2," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2015, p. 9.7.1-9.7.4. doi: 10.1109/IEDM.2015.7409665.

[3] Z. Bian, K. Zeng, and S. Chowdhury, "2.8 kV Avalanche in Vertical GaN PN Diode Utilizing Field Plate on Hydrogen Passivated P-Layer," *IEEE Electron Device Lett.*, vol. 43, no. 4, pp. 596–599, Apr. 2022, doi: 10.1109/LED.2022.3149748.

[4] H. Fukushima, S. Usami, M. Ogura, Y. Ando, A. Tanaka, M. Deki, M. Kushimoto, S. Nitta, Y. Honda, and H. Amano, "Vertical GaN p–n diode with deeply etched mesa and the capability of avalanche breakdown," *Appl. Phys. Express*, vol. 12, no. 2, p. 026502, Feb. 2019, doi: 10.7567/1882-0786/aafdb9.

[5] T. Maeda, T. Narita, H. Ueda, M. Kanechika, T. Uesugi, T. Kachi, T. Kimoto, M. Horita, and J. Suda, "Design and fabrication of GaN pn junction diodes with negative beveled-mesa termination," *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 941–944, 2019.

[6] B. Shankar, Z. Bian, K. Zeng, C. Meng, R. P. Martinez, S. Chowdhury, B. Gunning, J. Flicker, A. Binder, J. R. Dickerson, and R. Kaplar, "Study of Avalanche Behavior in 3 kV GaN Vertical P-N Diode Under UIS Stress for Edge-termination Optimization," in *2022 IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2022, p. 2B.2-1-2B.2-4. doi: 10.1109/IRPS48227.2022.9764525.

[7] D. Ji, S. Li, B. Ercan, C. Ren, and S. Chowdhury, "Design and Fabrication of Ion-Implanted Moat Etch Termination Resulting in 0.7 mΩcm2/1500 V GaN Diodes," *IEEE Electron Device Lett.*, vol. 41, no. 2, pp. 264–267, Feb. 2020, doi: 10.1109/LED.2019.2960349.

[8] H. Ohta, N. Asai, F. Horikiri, Y. Narita, T. Yoshida, and T. Mishima, "Two-Step Mesa Structure GaN p-n Diodes With Low ON-Resistance, High Breakdown Voltage, and Excellent Avalanche Capabilities," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 123–126, Jan. 2020, doi: 10.1109/LED.2019.2955720.

[9] Y. Bai, W. Xu, F. Zhou, Y. Wang, L. Guo, F. Ren, D. Zhou, D. Chen, R. Zhang, Y. Zheng, and H. Lu, "Over 10 kA/cm2 inductive current sustaining capability demonstrated in GaN-on-GaN pn junction with high ruggedness," *Micro Nanostructures*, vol. 170, p. 207367, Oct. 2022, doi: 10.1016/j.micrna.2022.207367.

[10] P. Pandey, T. M. Nelson, W. M. Collings, M. R. Hontz, D. G. Georgiev, A. D. Koehler, T. J. Anderson, J. C. Gallagher, G. M. Foster, A. Jacobs, M. A. Ebrish, B. P. Gunning, R. J. Kaplar, K. D. Hobart, and R. Khanna, "A Simple Edge Termination Design for Vertical GaN P-N Diodes," *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 5096–5103, Sep. 2022, doi: 10.1109/TED.2022.3192796.

[11] H. Fu, K. Fu, S. R. Alugubelli, C.-Y. Cheng, X. Huang, H. Chen, T.-H. Yang, C. Yang, J. Zhou, J. Montes, X. Deng, X. Qi, S. M. Goodnick, F. A. Ponce, and Y. Zhao, "High Voltage Vertical GaN p-n Diodes With Hydrogen-Plasma Based Guard Rings," *IEEE Electron Device Lett.*, vol. 41, no. 1, pp. 127–130, Jan. 2020, doi: 10.1109/LED.2019.2954123.

[12] M. Matys, T. Ishida, K. P. Nam, H. Sakurai, K. Kataoka, T. Narita, T. Uesugi, M. Bockowski, T. Nishimura, J. Suda, and T. Kachi, "Design and demonstration of nearly-ideal edge termination for GaN p–n junction using Mg-implanted field limiting rings," *Appl. Phys. Express*, vol. 14, no. 7, p. 074002, Jun. 2021, doi: 10.35848/1882-0786/ac0b09.

[13] V. Talesara, Y. Zhang, V. G. T. Vangipuram, H. Zhao, and W. Lu, "Vertical GaN-on-GaN pn power diodes with Baliga figure of merit of 27 GW/cm2," *Appl. Phys. Lett.*, vol. 122, no. 12, p. 123501, Mar. 2023, doi: 10.1063/5.0135313.

[14] J. R. Dickerson, A. A. Allerman, B. N. Bryant, A. J. Fischer, M. P. King, M. W. Moseley, A. M. Armstrong, R. J. Kaplar, I. C. Kizilyalli, O. Aktas, and J. J. Wierer, "Vertical GaN Power Diodes With a Bilayer Edge Termination," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 419–425, Jan. 2016, doi: 10.1109/TED.2015.2502186.

[15] I. C. Kizilyalli, A. P. Edwards, H. Nie, D. Disney, and D. Bour, "High Voltage Vertical GaN p-n Diodes With Avalanche Capability," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3067–3070, Oct. 2013, doi: 10.1109/TED.2013.2266664.

[16] J. Wang, L. Cao, J. Xie, E. Beam, R. McCarthy, C. Youtsey, and P. Fay, "High voltage, high current GaN-on-GaN p-n diodes with partially compensated edge termination," *Appl. Phys. Lett.*, vol. 113, no. 2, p. 023502, Jul. 2018, doi: 10.1063/1.5035267.

[17] J. Liu, M. Xiao, R. Zhang, S. Pidaparthi, C. Drowley, L. Baubutr, A. Edwards, H. Cui, C. Coles, and Y. Zhang, "Trap-Mediated Avalanche in Large-Area 1.2 kV Vertical GaN p-n Diodes," *IEEE Electron Device Lett.*, vol. 41, no. 9, pp. 1328–1331, Sep. 2020, doi: 10.1109/LED.2020.3010784.

[18] W. Lin, M. Wang, R. Yin, J. Wei, C. P. Wen, B. Xie, Y. Hao, and B. Shen, "Hydrogen-Modulated Step Graded Junction Termination Extension in GaN Vertical p-n Diodes," *IEEE Electron Device Lett.*, vol. 42, no. 8, pp. 1124–1127, Aug. 2021, doi: 10.1109/LED.2021.3091335.

[19] J. Liu, R. Zhang, M. Xiao, S. Pidaparthi, H. Cui, A. Edwards, L. Baubutr, C. Drowley, and Y. Zhang, "Surge Current and Avalanche Ruggedness of 1.2-kV Vertical GaN p-n Diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10959–10964, Oct. 2021, doi: 10.1109/TPEL.2021.3067019.

[20] D. Johannesson, M. Nawaz, and H.-P. Nee, "Assessment of Junction Termination Extension Structures For Ultrahigh-Voltage Silicon Carbide Pin-Diodes; A Simulation Study," *IEEE Open J. Power Electron.*, vol. 2, pp. 304–314, 2021, doi: 10.1109/OJPEL.2021.3072486.

[21] E. A. Imhoff, F. J. Kub, K. D. Hobart, M. G. Ancona, B. L. VanMil, D. K. Gaskill, K.-K. Lew, R. L. Myers-Ward, and C. R. Eddy, "High-Performance Smoothly Tapered Junction Termination Extensions for High-Voltage 4H-SiC Devices," *IEEE Trans. Electron Devices*, vol. 58, no. 10, pp. 3395–3400, Oct. 2011, doi: 10.1109/TED.2011.2160948.

[22] B. Wang, M. Xiao, J. Spencer, Y. Qin, K. Sasaki, M. J. Tadjer, and Y. Zhang, "2.5 kV Vertical Ga2O3 Schottky Rectifier With Graded Junction Termination Extension," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 221–224, Feb. 2023, doi: 10.1109/LED.2022.3229222.

[23] J. P. Kozak, R. Zhang, M. Porter, Q. Song, J. Liu, B. Wang, R. Wang, W. Saito, and Y. Zhang, "Stability, Reliability, and Robustness of GaN Power Devices: A Review," *IEEE Trans. Power Electron.*, pp. 1–31, 2023, doi: 10.1109/TPEL.2023.3266365.

[24] K. Zeng and S. Chowdhury, "Designing Beveled Edge Termination in GaN Vertical p-i-n Diode-Bevel Angle, Doping, and Passivation," *IEEE Trans. Electron Devices*, vol. 67, no. 6, pp. 2457–2462, Jun. 2020, doi: 10.1109/TED.2020.2987040.

[25] "SRIM & TRIM." http://www.srim.org/ (accessed May 18, 2023).

[26] P. Saint-Cast, D. Kania, M. Hofmann, J. Benick, J. Rentsch, and R. Preu, "Very low surface recombination velocity on p-type c-Si by high-rate plasma-deposited aluminum oxide," *Appl. Phys. Lett.*, vol. 95, no. 15, p. 151502, Oct. 2009, doi: 10.1063/1.3250157.

[27] D. Tetzlaff, M. Dzinnik, J. Krügener, Y. Larionova, S. Reiter, M. Turcu, R. Peibst, U. Höhne, J.-D. Kähler, and T. F. Wietler, "Introducing pinhole magnification by selective etching: application to poly-Si on ultra-thin silicon oxide films," *Energy Procedia*, vol. 124, pp. 435–440, Sep. 2017, doi: 10.1016/j.egypro.2017.09.270.

[28] J. Q. Han, R. S. Feng, and X. F. Wang, "Wet Etching Studies of PECVD Silicon Nitride Films in Doped TMAH Solutions," *Adv. Mater. Res.*, vol. 465, pp. 1–7, 2012, doi: 10.4028/www.scientific.net/AMR.465.1.

[29] R. Zhang, J. P. Kozak, M. Xiao, J. Liu, and Y. Zhang, "Surge-Energy and Overvoltage Ruggedness of P-Gate GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13409–13419, Dec. 2020, doi: 10.1109/TPEL.2020.2993982.

[30] D. Ji, B. Ercan, and S. Chowdhury, "Experimental determination of impact ionization coefficients of electrons and holes in gallium nitride using homojunction structures," *Appl. Phys. Lett.*, vol. 115, no. 7, p. 073503, Aug. 2019, doi: 10.1063/1.5099245.

[31] A. Castiglia, J.-F. Carlin, and N. Grandjean, "Role of stable and metastable Mg–H complexes in p-type GaN for cw blue laser diodes," *Appl. Phys. Lett.*, vol. 98, no. 21, p. 213505, May 2011, doi: 10.1063/1.3593964.

[32] J. A. Cooper and D. T. Morisette, "Performance Limits of Vertical Unipolar Power Devices in GaN and 4H-SiC," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 892–895, Jun. 2020, doi: 10.1109/LED.2020.2987282.