A New Hybrid Modular Multilevel Rectifier as MVAC-LVDC Active Front-End Converter for Fast Charging Stations and Data Centers

Jian Liu, *Student Member, IEEE*, Jayesh Kumar Motwani, *Student Member, IEEE*, Rolando Burgos, *Senior Member, IEEE,* Zhi Zhou, *Member, ASNE,* Dong Dong, *Senior Member, IEEE*

Abstract- **As the power demands from DC energy-storage and loads continue to grow in electric vehicle (EV) fast charging stations and data centers, the power delivery infrastructure faces challenges with the installation of bulky, heavy, and slow responsive line-frequency power transformer (LFT). These transformers are required to step-down the feeder voltage from medium-voltage (MV) ac grid-service to low-voltage (LV) ac, followed by LVac-LVdc rectifiers. This approach results in a large equipment footprint, heavy conductor copper usage, and lower efficiency. Consequently, there is increasing interest in exploring direct interface from MVac to LVdc without the need for LFT. This paper proposed a new solution called MVac-LVdc hybrid modular multilevel rectifier (HMMR). The HMMR serves as a centralized step-down active front-end converter, enabling power delivery to LVdc with a reduced number of dc/dc back-end isolated converters. Compared to the modular multilevel converter (MMC) used as the MVac interface solution, the proposed HMMR could save the submodule number by 40%, reduce losses by 22%, and significantly reduce the footprint area by 37%, effectively increasing the power density and reducing the construction cost. Moreover, the proposed HMMR has the potential to operate in both unity and non-unity power factor modes, allowing it to provide the grid-support functionality. The performance of HMMR is evaluated and compared with full-bridge MMC in the case of 13.8 kV ac to 6 kV dc. The feasibility of the proposed converter is verified by the simulation results with the same specifications. Finally, a scale-down 1.4 kV HMMR prototype is developed to validate the effectiveness of the proposed converter.**

Index Terms- **Fast charging stations, Hybrid modular multilevel rectifier (HMMR), active front-end converter.**

I. Introduction

The exponential rise in power demand for dc-based energy storage and loads can be attributed to the proliferation of electric vehicles (EVs) on the roads and the emergence of next-generation data centers with artificial intelligence (AI) platforms [1-3]. Fig. 1(a) illustrates a typical power delivery architecture that employs a low-frequency transformer (LFT) to step down the voltage from the three-phase medium voltage (MV) grid [4-6]. The centralized LVac-LVdc active front-end (AFE) converter produces a LV dc bus, capable of accommodating EV fast charging stations (FCSs), energy storage systems (ESSs), and data center dc loads. According to [6], the power demand from EV charging stations and data centers is expected to escalate to the multi-MW to -GW range. However, the usage of the step-down LFT presents several challenges. Firstly, as power levels increase, the LFT imposes a maximum efficiency barrier of approximately 95%. Furthermore, the significant footprint of LFTs leads to higher capital investments, especially in urban areas with high land costs. The large impedance within the LFTs also introduces the grid sags, swells, and other grid stability issues when dealing with pulse-type power delivery in EV charging. These challenges have motivated the exploration of highly efficient and compact power delivery solutions.

Currently, some alternative solutions have been proposed to replace the existing power delivery structure. One possible scheme, depicted in Fig. 1(b), uses the medium- / high-frequency transformers (M/HFTs) inside isolated dc/dc converters after the MVac-MVdc AFE. The M/HFTs can provide galvanic isolation while significantly reducing the size

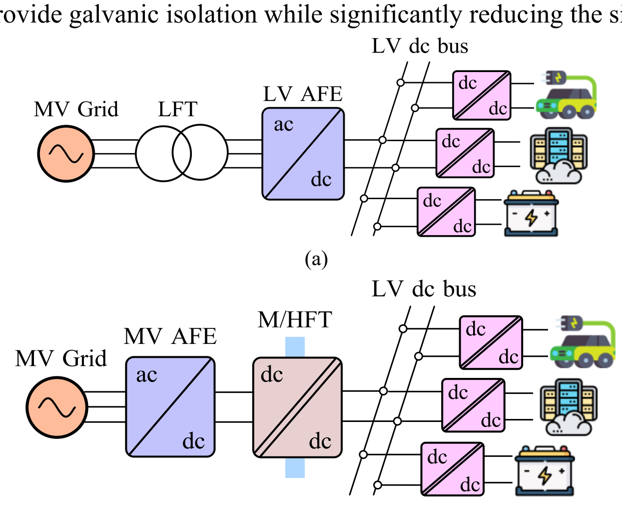

Fig. 1 Two MVac/LVdc schemes for EV charging and data centers, (a) LFT + LV AFE + dc/dc and (b) centralized MV AFE + M/HFT-based dc/dc.

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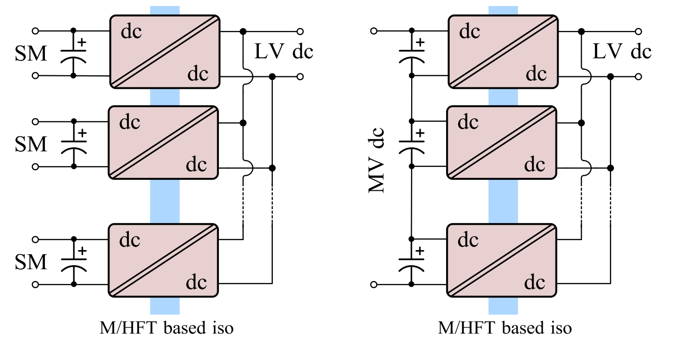
Jian Liu, Jayesh Kumar Motwani, Rolando Burgos and Dong Dong are with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA, (e-mail: jianl@vt.edu; jayeshkmotwani@vt.edu; rolando@vt.edu; dongd@vt.edu).

Zhi Zhou is with GE Power Conversion of GE Vernova, Niskayuna, NY 12309, (e-mail: zhouzhi@ge.com).



(a) (b)

Fig. 2 Connection of back-end dc/dc stage, (a) multiport SST structure, (b) ISOP structure.

the neutral point clamp (NPC) converter [8], cascaded H-bridge (CHB) [9-11], and modular multilevel converter (MMC) [12-14], have been proposed. The CHB and MMC configurations, in particular, offer attractive features such as modularity, scalability, and redundancy. Notably, both solutions require minimal AC filters, resulting in faster charging power delivery and higher power density.

By capitalizing on its modular structure, the back-end dc/dc converter can connect to the individual submodule (SM) dc-link, creating a multiport system as depicted in Fig. 2(a). Such solid-state transformer (SST) units have been extensively utilized in dc microgrid and renewable energy systems [15-17]. Nevertheless, this solution presents some practical challenges. Firstly, the galvanic isolation is required to ensure safety in LV system [7], whereas the isolation level depends on the MV ac voltage class and is not easily scalable. Secondly, compared to the modular concepts with MV isolation requirement, the centralized transformer occupies smaller amount of space [18], [19]. Consequently, with regard to transformer efficiency and power density, a smaller number of MV-insulated transformers in the system perform better.

To decouple the AFE and the back-end dc/dc stage, the input series and output parallel (ISOP) connection in Fig. 2(b) is employed to handle the MV voltage at the input and high current at the output [20]. The isolated dc/dc converters such as dual active bridge (DAB) and CLLC converter [21], [22] could be utilized here to ensure good voltage and current sharing while enhancing fault-tolerant operation. In this arrangement, the back-end dc/dc stage acts as a "dc transformer" and the MV insulation is only the dc voltage level without the ac components. Moreover, compared to the SST structure, the total number of MV-insulated transformers can be significantly reduced [23].

To further simplify the back-end dc/dc converters and reduce the number of transformers, a step-down AFE which can convert MVac directly to LVdc is preferred [23]. The existing common solution is the FB MMC. However, it suffers from drawbacks such as a large number of SMs and significant SM dc-link capacitor size. Recently, various "hybrid multilevel converters (HMCs)" have emerged to address these issues [24], based on the concept of combining high voltage (HV) switches and chain-links (CLs). A group of converters, including alternate arm converter (AAC) [25], and hybrid modular multilevel converters [26-31] have been proposed. They can address one or more issues of MMC, but the HV switch based on series connected active devices requires active voltage sharing and extra auxiliary power supplies. Therefore, the hybrid modular multilevel rectifier (HMMR) were proposed by replacing the HV active switch stacks with HV diodes [32-35]. In this way, the key benefits of HMMC are retained, while significantly reducing the design complexities associated with HV switches. It is worth noting that the previously proposed HMMR was only suitable for step-up conversion with dc voltage amplitude higher than the ac side. Consequently, it was more appropriate for the HVDC power transmission rather than the EV charging station and data center applications discussed in this paper. In [23], it was revealed that the $HMMC_3$ exhibits the best performance among three HMCs and FB-HMMC. Therefore, this paper introduces the rectifier version of $HMMC_3$, referred as the step-down HMMR, aiming to further reduce costs and volume for unidirectional power delivery. Above all, the main contribution of this paper is:

- The proposed step-down HMMR topology is desired for the AFE in the fast charging stations or other MVac to LVdc power distribution applications like dc Microgrid for datacenters, which could reduce the number of back-end dc/dc converters.
- The unity and non-unity power factor (PF) operation principles of the proposed HMMR are explained.
- Performance is evaluated and compared between the traditional FB-MMC and HMMR in terms of the device number, capacitor energy storage and efficiency.
- Dc and ac fault ride-through strategy is analyzed.

The paper is organized as follows. The step-down HMMR-based AFE topology, the single-phase as well as the three-phase operation principles are illustrated in Section II. In Section III, the performance comparison between the traditional MMC and HMMR at different PF is conducted. The control strategy and the fault ride-through are explained in Section IV. The simulation and the experimental results of a scale-down prototype are provided to validate the proposed topology in Section V. Finally, Section VI draws conclusions.

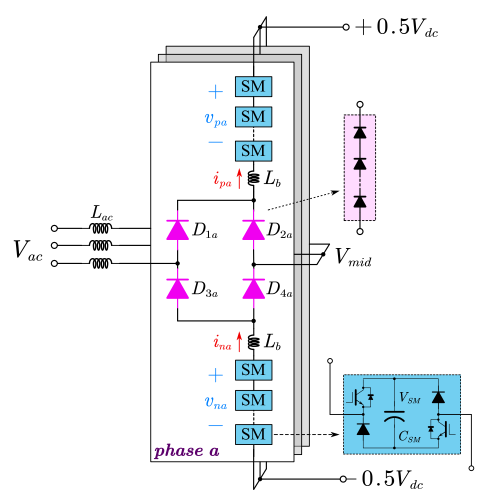


Fig. 3 Topology of the proposed step-down HMMR.

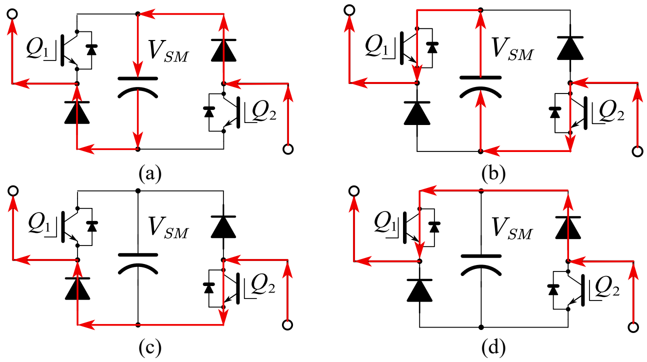


Fig. 4 Four working modes of UCH-SM.

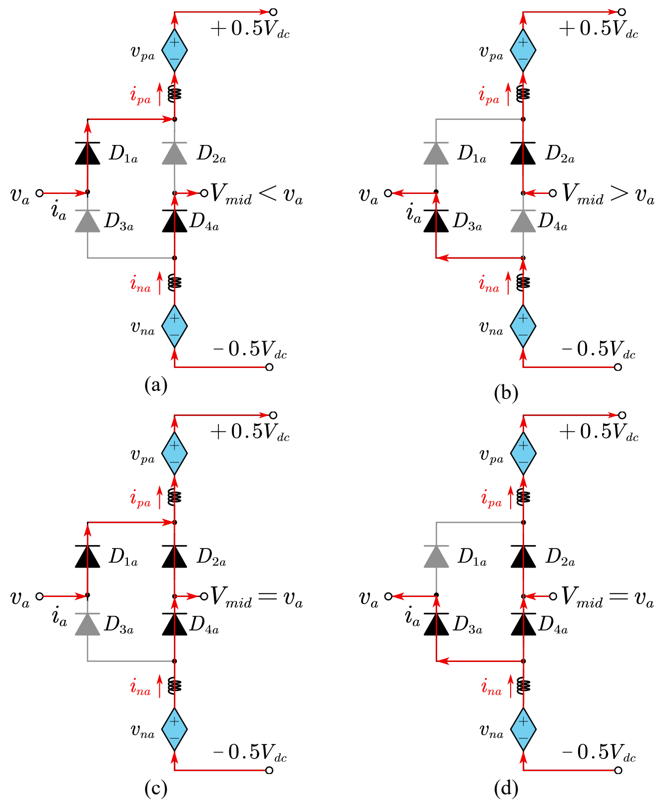


Fig. 5 Four working states of single phase HMMR, (a) state 1, (b) state 2, (c) state 3, (d) state 4.

II. System Overview and Operation Principle

A. System Topology

Fig. 3 depicts the topology of the proposed three-phase step-down HMMR. V_{dc} and V_{ac} are the rated dc-side voltage and ac-side voltage amplitude, respectively. Each phase-leg consists of one upper and one lower arm connected between four HV diode stacks (D_1 - D_4). The midpoints of three-phase diode stacks are connected together at the voltage potential of V_{mid}, which provides the freedom to reshape the CL voltage. In this type of HMMR, each arm consists of one arm inductor L_b and series connected unidirectional current H-bridge SMs (UCH- SMs) [36]. Instead of four fully controlled devices, two parallel chopper circuits could be used here due to the unipolar CL current. The basic working modes of UCH-SM are given in Fig. 4. When both Q_1 and Q_2 are turned off, the UCH-SM output voltage becomes $-V_{SM}$. On the contrary, the UCH-SM output voltage becomes V_{SM} with Q_1 and Q_2 turned on. If only one of Q_1 and Q_2 is turned on, this SM is bypassed.

Each SM has a floating capacitor C_{SM} at voltage V_{SM}. v_{pa}, and v_{na} represent the total voltages across the upper and lower CLs, respectively. While the upper and lower arm currents are denoted as i_{pa} and i_{na}. The ac side variables are defined as,

$$v_a = V_{ac}\sin(\omega t - \varphi),\ i_a = I_{ac}\sin(\omega t) \tag{1}$$

where V_{ac} and I_{ac} represent the amplitude of ac voltage and current, respectively. The angular frequency is denoted as ω. The phase angle difference between current and voltage is given by φ, which determines the PF value. The modulation index M is defined as M=2V_{ac}/V_{dc}.

Considering the symmetrical structure of HMMR, phase a is taken as an example to illustrate the single-phase operation. It can be observed that two diodes in the upper or lower arms have the same polarity. Therefore, a constraint is imposed that the CL current should always keep positive. The conduction of D_{1a} or D_{3a} is determined by the polarity of the ac current. When i_a is positive, D_{1a} is on, and when i_a is negative, D_{3a} is on. While the conduction of D_{2a} and D_{4a} is determined by the voltage potential relationship between v_a and V_{mid} as in (2).

$$\begin{gathered} V_{mid} < v_a,\ D_{4a}\ \text{on} \\ V_{mid} > v_a,\ D_{2a}\ \text{on} \\ V_{mid} = v_a,\ D_{2a}\ \&\ D_{4a}\ \text{on} \end{gathered} \tag{2}$$

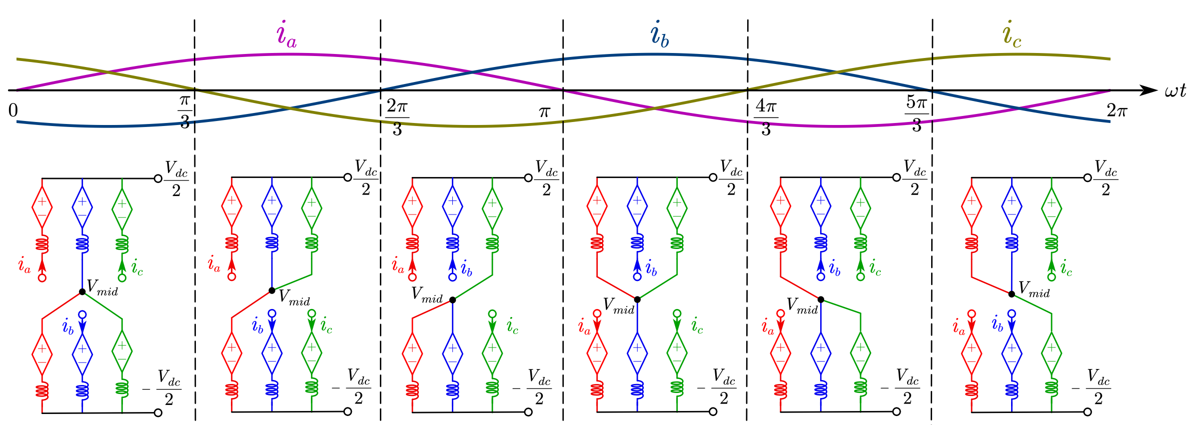


Fig. 6 Three-phase configuration of HMMR at unity PF.

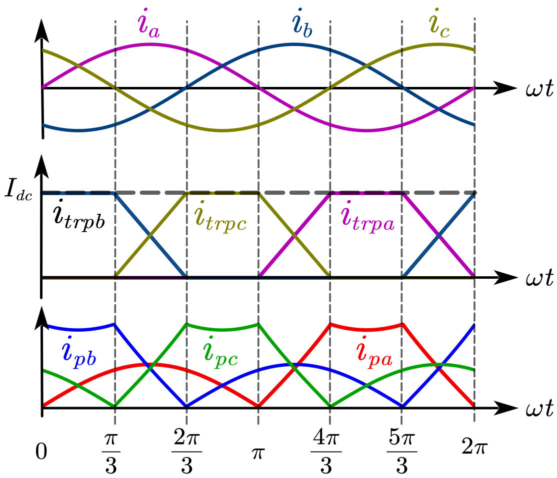


Fig. 7 Three-phase currents and trapezoidal current allocation.

As a result, there are four kinds of working states for the single-phase HMMR as shown in Fig. 5. Moreover, the upper and lower CL voltages could be calculated in (3) if neglecting the inductor voltage,

$$\begin{aligned} &v_{pa}^* = 0.5V_{dc} - v_a,\ v_{na}^* = 0.5V_{dc} + V_{mid}\ \ (\text{state } 1,3) \\ &v_{pa}^* = 0.5V_{dc} - V_{mid},\ v_{na}^* = 0.5V_{dc} + v_a\ \ (\text{state } 2,4) \end{aligned} \tag{3}$$

B. Unity PF Operation and Current Allocation

According to the single-phase working principle, the three-phase connection of HMMR during one line cycle could be depicted in Fig. 6. The six different combinations of three-phase ac current polarity means six different configuration. It can also be observed that three upper arms are always connected to the positive bus while three lower arms are connected to the negative bus. Therefore, this configuration looks more similar to the conventional MMC.

The current distribution among upper three arms should be designed to maintain the constant dc bus current. Taking the upper arm of phase a as an example, there is constraint that i_{pa} should equal i_a in state 1 and 3. However, i_{pa} could be arbitrary in state 2 and 4, and a trapezoidal current i_{trpa} is added to synthesize i_{pa} as in (4).

$$i_{pa} = i_a + i_{trpa} = i_a + \begin{cases} 0,\ \omega t \in [0,\pi) \\ I_{dc} \cdot (\omega t - \pi) \Big/ \left(\frac{\pi}{3}\right),\ \omega t \in [\pi, 4\pi/3) \\ I_{dc},\ \omega t \in [4\pi/3, 5\pi/3) \\ I_{dc} \cdot (2\pi - \omega t) \Big/ \left(\frac{\pi}{3}\right),\ \omega t \in [5\pi/3, 2\pi) \end{cases} \tag{4}$$

The upper arm current for phase b and phase c has same shape with 120º phase shift. In this way, the total positive dc bus current i_{dcp} becomes,

$$\begin{aligned} i_{dcp} &= i_{pa} + i_{pb} + i_{pc} \\ &= i_a + i_{trpa} + i_b + i_{trpb} + i_c + i_{trpc} \\ &= i_{trpa} + i_{trpb} + i_{trpc} \\ &= I_{dc} \end{aligned} \tag{5}$$

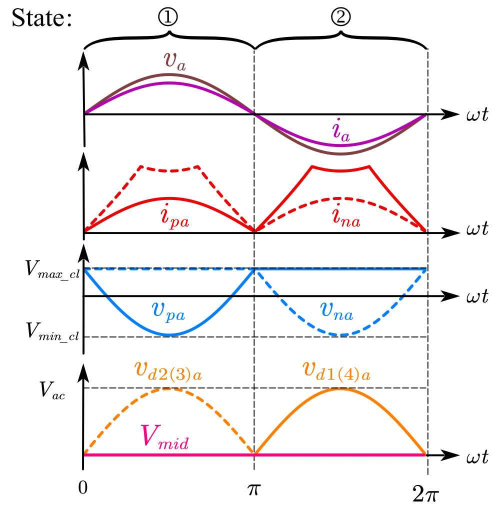


Fig. 8 Single-phase arm current and voltage waveforms at unity PF.

As shown in Fig. 7, this trapezoidal allocation in (4) could achieve constant dc bus current. Then the single-phase CL voltage and currents could be plotted in Fig. 8. It can be seen that this phase changes the working state between state 1 and 2 naturally at the ac voltage zero-crossing point with the midpoint voltage V_{mid} = 0. In this way, the maximum and minimum CL voltage stress could be calculated in (6).

$$V_{max\_cl} = 0.5V_{dc},\ V_{min\_cl} = 0.5V_{dc} - V_{ac} \tag{6}$$

In this case, the required SM number in this HMMR could be determined in (7).

$$N_{SM} = \frac{\max\{V_{max\_cl}, |V_{min\_cl}|\}}{V_{SM}} \tag{7}$$

As for the diode, the blocking voltage is sinusoidal, which means the series connection challenge is not so difficult. Besides, the maximum diode voltage stress could be,

$$V_{max\_diode} = V_{ac} \tag{8}$$

The constraint of the positive CL current is closely related to the modulation index. According to (4), i_{pa} equals i_a in the positive cycle, which means this constraint is met naturally. As for the negative cycle, the constraint indicates,

$$I_{ac}\sin(\omega t) + I_{dc} \cdot (\omega t - \pi) \Big/ \left(\frac{\pi}{3}\right) > 0,\ \ \omega t \in [\pi, 4\pi/3) \tag{9}$$

Combined with the power balance between ac and dc side in (10), it can be proven that the modulation index $M = 2V_{ac}/V_{dc}$ could satisfy (11) to meet the constraint.

$$V_{dc}I_{dc} = 3 \cdot \frac{V_{ac}I_{ac}}{2} \tag{10}$$

The minimum point of (9) could be derived through the differential which locates at ωt = π + acos(9M/4π). Therefore, the limit of modulation index could be obtained in (11), which matches the step-down rectifier application.

$$M \geqslant \frac{4\pi}{9} \tag{11}$$

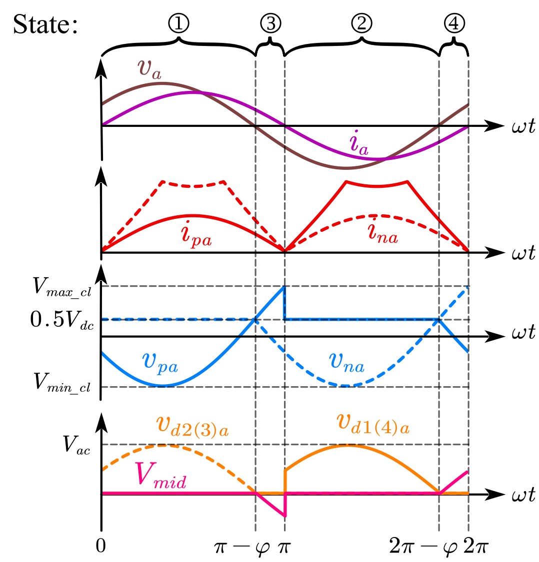


Fig. 9 Single-phase waveforms using state 3 and 4 during the transition at non-unity PF.

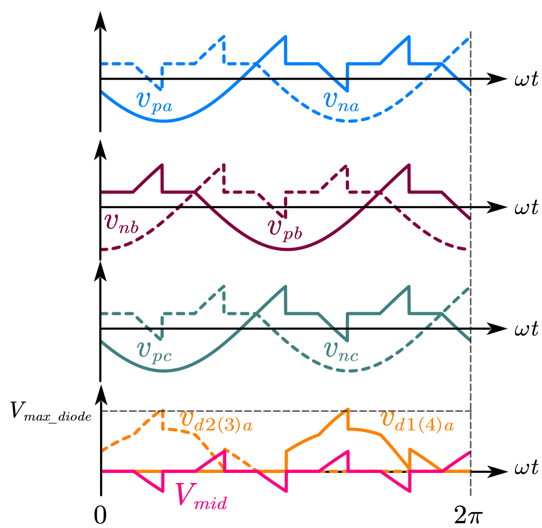


Fig. 10 CL voltage and midpoint voltage for three-phase HMMR.

D. Non-unity PF Operation and Working Range

In the case of non-unity PF, there is a non-overlap period where the polarity of ac side current and voltage is opposite. Obviously, the midpoint voltage V_{mid} cannot maintain at 0 anymore during this period. To solve that, states 3 or 4 should be utilized during the transition, and the midpoint voltage V_{mid} should shift to ac voltage. It means that the CL voltage should be modified accordingly.

An example of a current lagging case with $\varphi < \pi/6$ is presented in Fig. 9. In this case, state 1 is still effective between the range of $\omega t \in (0, \pi - \varphi)$. However, when the v_a becomes negative while i_a is positive during $(\pi - \varphi, \pi)$, the diode D_{2a} is forced to be on if the midpoint voltage V_{mid} is still 0. As a result, V_{mid} should shift to be the same as the ac voltage of v_a, which matches with state 3. Similarly, state 2 is applied during the range of $(\pi, 2\pi - \varphi)$, while state 4 is applied in the range of $(2\pi - \varphi, 2\pi)$.

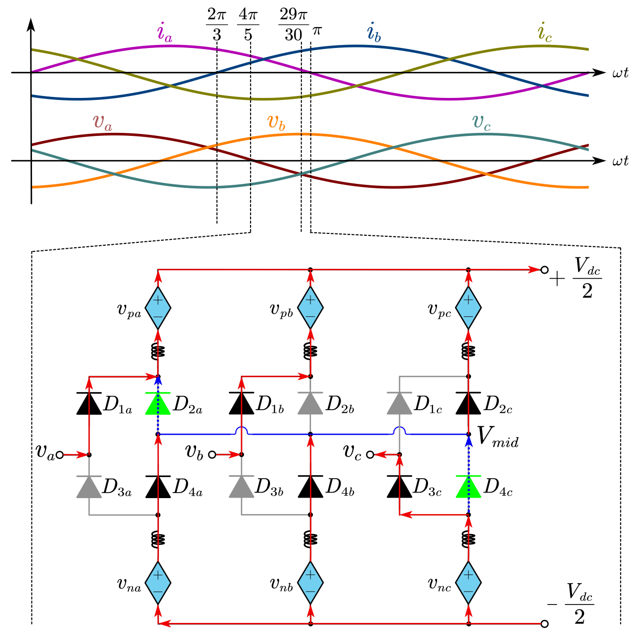


Fig. 11 Example of diode conduction conflict when $\varphi > \pi/6$.

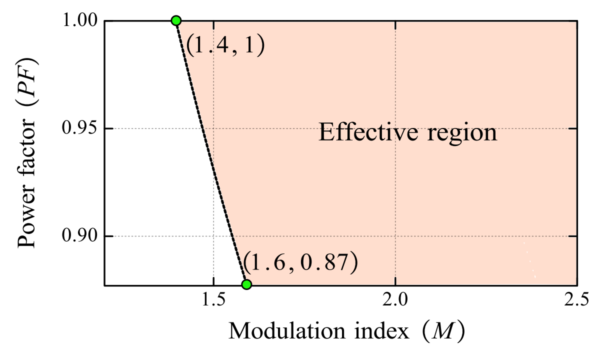


Fig. 12 Limitation of minimum modulation index for HMMR at non-unity PF.

After shifting the midpoint voltage V_{mid}, the minimum CL voltage $V_{\text{min\_cl}}$ keeps the same, while the maximum CL voltage $V_{\text{max\_cl}}$ becomes larger as expressed in (12).

$$V_{max\_cl} = 0.5V_{dc} + V_{ac}\sin\varphi \tag{12}$$

Since the three-phase midpoints are connected together, three-phase CL voltages should change simultaneously through (3) when V_{mid} shifts to one phase ac voltage. The corresponding waveforms are presented in Fig. 10. The CL voltage stress does not change, but the diode voltage stress becomes higher, which is derived in (13).

$$V_{max\_diode} = \max\left\{V_{ac},\ V_{ac}\left[\sin\left(\frac{\pi}{3}+|\varphi|\right)+\sin(|\varphi|)\right]\right\} \tag{13}$$

Besides, it should be noted that the state 3 and 4 used in non-unity PF is feasible when φ is lower than $\pi/6$. Otherwise, the conflict of two diode conduction will make this topology work improperly.

Taking $\varphi = \pi/5$ as an example, the three-phase connection and the current phase are shown in Fig. 11. In the range of $(4\pi/5, 29\pi/30)$, state 3 still works for phase a. However, when v_c is larger than v_a, the D_{4c} will be on and V_{mid} will shift to v_c instead of v_a. On the other hand, D_{2a} will be forced on as V_{mid}

$= v_c > v_a$. Since D_{1a} is on at the same time, the conflict between D_{1a} and D_{2a} implies that this topology cannot work properly. Therefore, there is a minimum PF limitation of 0.87.

In addition, the variable PF will also influence the lower limit of the modulation index M. Their relationship is given in Fig. 12 using (14).

$$M \geqslant \frac{4\pi}{9\cos\varphi} \tag{14}$$

E. Control of HMMR

The overall control structure for HMMR is shown in Fig. 13. The key idea is determining the ac and dc components of arm current reference i_{cl}^* in (4). The ac component $i_{a,b,c}^*$ could charge the total energy stored in the SM capacitor. Therefore, the feedforward component i_{d_ff} through the power calculation plus the sum energy balancing block output yields the current reference i_d^* in d axis.

$$i_d^* = \left(k_{p1} + \frac{k_{i1}}{s}\right)\left(V_{SM}^* - \frac{\sum v_{Ccl}}{6N}\right) + i_{d\_ff} \tag{15}$$

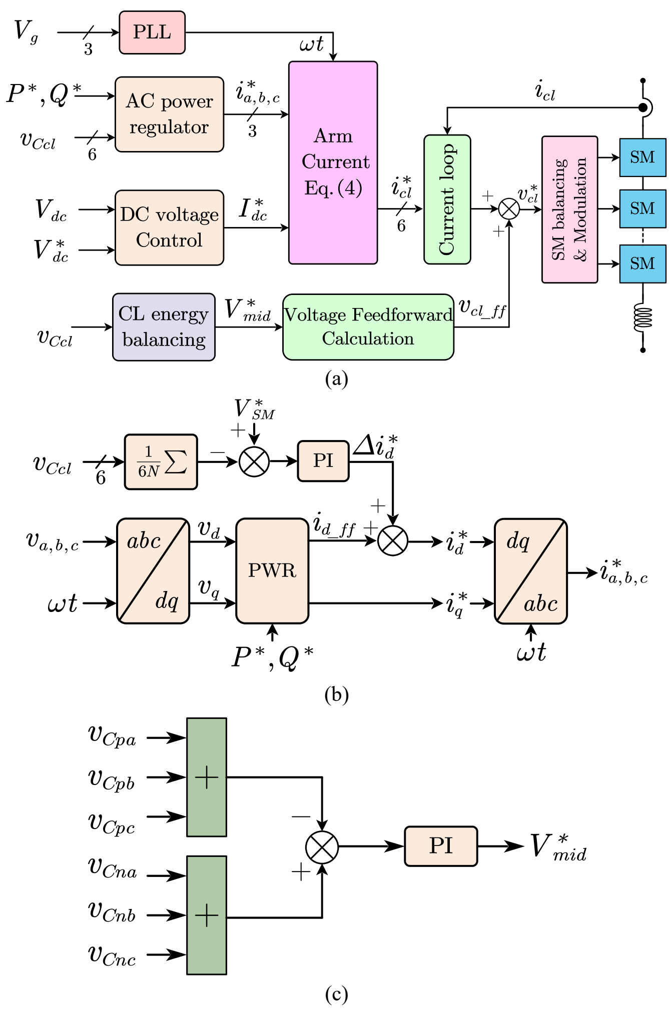


Fig. 13 (a) Overall control structure of HMMR, (b) AC side power control block and sum energy balancing, (c) upper and lower CL energy balancing.

Where k_{p1} and k_{i1} are the parameters of the PI controller. While the dc component I_{dc}^* should maintain the output voltage constant. Then the current loop regulator could track the synthesized current reference from (4). Although this current reference is not sinusoidal, it is still a periodic wave. Therefore, the repetitive control could be used here to track the current reference. The controller parameters for stability and dynamic performance has been analyzed in [29].

Another important aspect is the upper and lower CL capacitor energy balancing, which could employ the midpoint voltage V_{mid}. Except the transition period, V_{mid} could be shifted from 0 to a certain value so that the energy could be exchanged between upper three and lower three arms. The control methods are given in (16) and shown in Fig. 13(c).

$$V_{mid}^* = \left(k_{p2} + \frac{k_{i2}}{s}\right)\left(v_{Cna} + v_{Cnb} + v_{Cnc} - v_{Cpa} - v_{Cpb} - v_{Cpc}\right) \tag{16}$$

Instead of controlling the current, the midpoint voltage could be controlled easily by changing the CL voltage directly in HMMR. Taking the first segment of (0, π/6) in Fig. 6 as an example, the midpoint voltage could be controlled to the desired value of V_{mid}* by assigning the CL feedforward voltage in (17).

$$\begin{aligned} v_{na\_cl} &= 0.5V_{dc}^* + V_{mid}^* \\ v_{pb\_cl} &= 0.5V_{dc}^* - V_{mid}^* \\ v_{nc\_cl} &= 0.5V_{dc}^* + V_{mid}^* \end{aligned} \tag{17}$$

Adding the current loop output and the feedforward CL voltage yields the total CL voltage reference. Then the low-level control is responsible for the multilevel modulation and individual capacitor voltage balancing. This method has been widely applied in MMC [29], thus not discussed here.

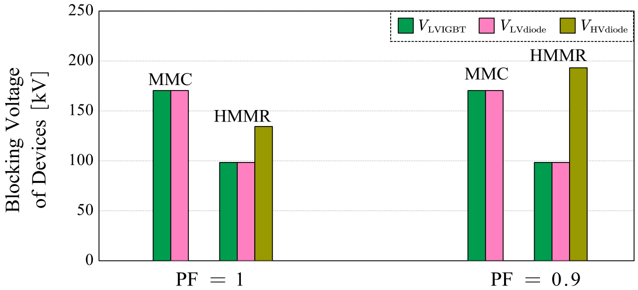
TABLE I
Specifications of HMMR-based MV AFE

Description	Symbol	Value
Input three-phase Line-voltage (RMS)	$V_{LL\ rms}$	13.8 kV
Input frequency	f_{in}	60 Hz
Output DC bus voltage	V_{dc}	6 kV
Rated power	S	2 MVA
PF	PF	0.9~1
SM capacitor voltage	V_{SM}	1 kV
SM capacitor ripple	ε	10%

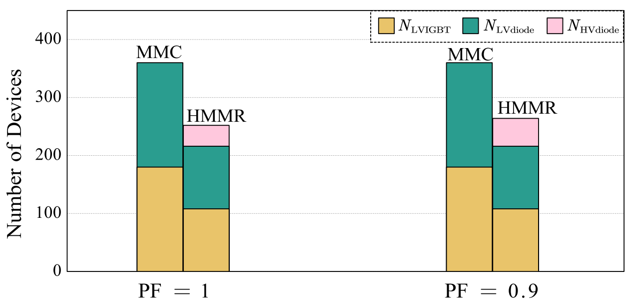
III. Comparison Between FB-MMC and HMMR

As mentioned earlier, such step-down HMMR is well suited for the AFE in the FCS, because it could reduce the number of back-end dc/dc converters and M/HFT. Another feasible step-down rectifier solution is FB-MMC [7], which is selected as the benchmark to evaluate the performance of the proposed HMMR in terms of device number, capacitor energy storage as well as efficiency. A medium voltage case of 13.8 kV ac and 6 kV dc is conducted below to demonstrate the comparison, and the electrical parameters are listed in Table I.

According to [37], the AFE should take current from the unity grid at high PF and low THD to maintain the IEEE-519 standards [38]. Nevertheless, the adjustable non-unity PF operation is a good feature for the AFE to support the grid or compensate the grid. This is not feasible for the traditional



(a)



(b)

Fig. 14 (a) Total blocking voltage and, (b) number of devices for MMC and HMMR at PF of 1 and 0.9.

multi-pulse rectifier. Considering the PF limitation of proposed HMMR, the PF range between 0.9 and 1 is selected here for comparison.

A. CL voltage and Device Number

Arm voltage stress is directly related to the device number used in HMMR. Since the FB-MMC has the unipolar arm current as well, the UCH-SM is selected for both topologies. The total blocking voltage for LV IGBT, LV diode and HV diode are calculated and given in Fig. 14(a). It can be found the HMMR is replacing the LV device in MMC with the HV-diode to save the volume and cost. In the unity PF, the total blocking voltage of HMMR is also slightly lower than MMC.

Then the device number could also be calculated with the specific device. The chopper module (FD300R17KE4P) [39] from Infineon is used for the SM power device, which features a maximum collector-emitter voltage of 1.7 kV and a continuous DC collector current of 300 A. As for the diode stack, 7.2 kV press-pack diode W0790LG720 [40] from IXYS is selected to minimize the number of devices.

The number of SMs in each arm is selected so that the dc link capacitor voltage V_{SM} does not exceed 1 kV, and the FB SM number should be sufficient to provide the negative voltage.

$$N_{MMC} = \frac{0.5V_{dc} + V_{ac}}{V_{SM}} \tag{18}$$

As for the HMMR, the SM number is determined by (7), while the diode requirement is related to the total blocking voltage V_{br_HMMR} at the off state and the reverse voltage V_{rv}. Supposing a blocking utilization factor of 70%, the diode number could be expressed in (19). Compared to the active switch with possible gate mismatch issue, the voltage sharing issue for diode will become much easier with passive method.

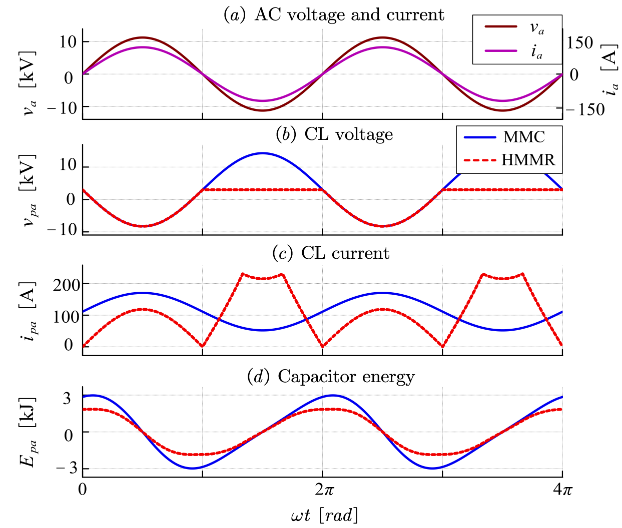
$$N_{diode\_HMMR} = \frac{V_{br\_HMMR}}{V_{rv} * 70\%} \tag{19}$$

Therefore, the device number at the PF =1 and PF = 0.9 is given in Fig. 14(b). It can be seen that the SM number of HMMR is only 40% lower than that of MMC, which saves the cost significantly. The SM number does not change when PF reduces and only a few HV diodes are required. Compared to MMC, the HV diode does not need gate driver units as well as auxiliary power, thus simplifying the system a lot.

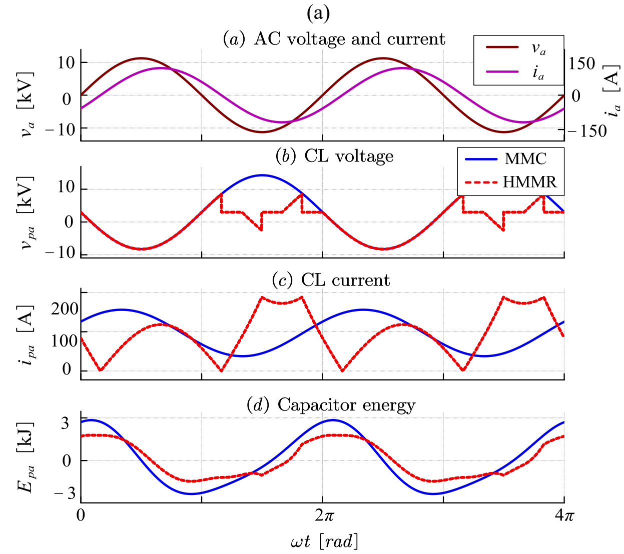
B. Capacitor Size

Capacitors in MMC are one of the important factors directly affecting power density and cost. HMMR could reduce the SM number successfully, but the capacitance value is still unknown. The capacitor energy storage requirement per unit apparent power E_{unit} is related to the energy deviation ΔE and capacitor voltage ripple coefficient ε.

$$E_{unit} = 6N\frac{C_{SM}{V_{SM}^{*}}^{2}}{2S} = \frac{3\Delta E}{2\varepsilon S} \tag{20}$$



(a)



(b)

Fig. 15 Ideal waveforms of MMC and HMMR at (a) PF = 1 and (b) PF = 0.9.

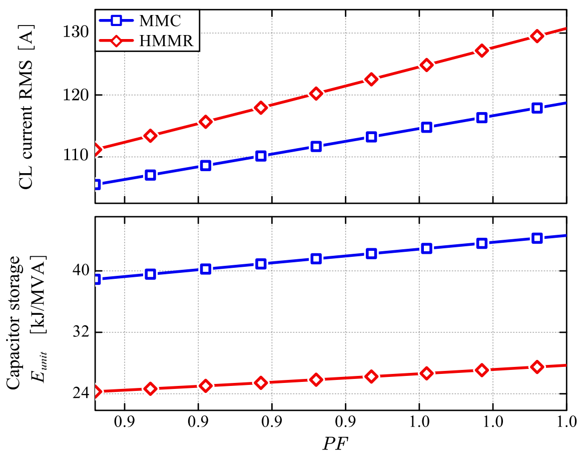
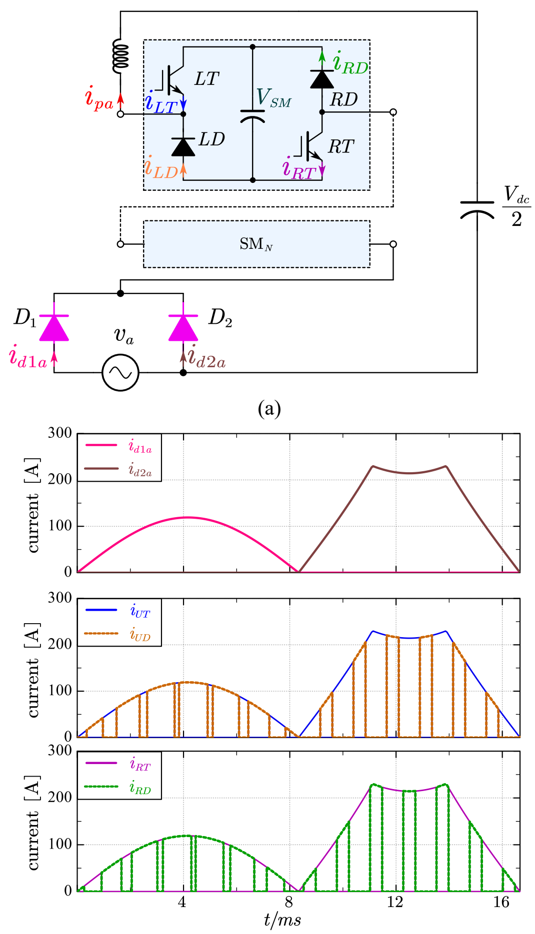


Fig. 16 Arm current and energy ripple versus PF.



(b)

Fig. 17 (a) Current definition of HMMR diode stack and SM, (b) Current distribution waveforms.

To present the CL voltage stress, currents as well as capacitor energy variation of two topologies, the ideal waveforms are plotted in Fig. 15 with PF of 1 and 0.9. It can be observed that CL current rms value of HMMR is higher than MMC, while its capacitor energy ripple is relatively lower. The relationship between these variables and PF is also given in Fig. 16, which demonstrates a monotonous tendency

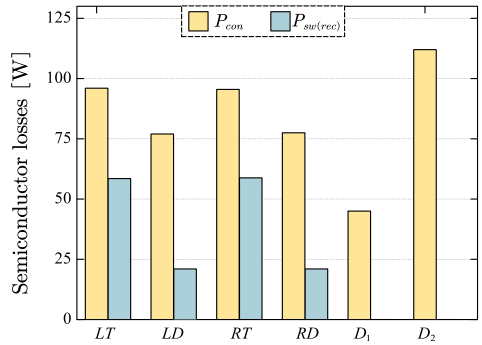


Fig. 18 Semiconductor losses distribution for single UCH-SM and HV diode in HMMR at unity PF.

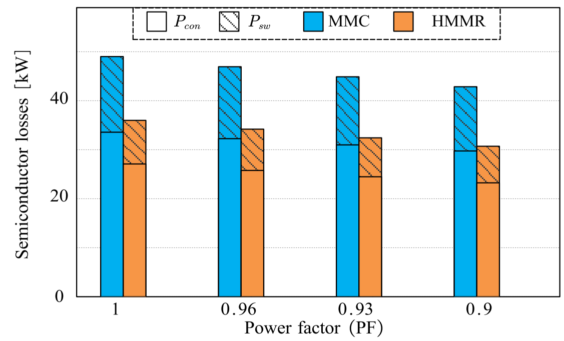


Fig. 19 Power losses in MMC and HMMR with two methods.

for both topologies. When PF is closer to 1, the current rms value and the capacitor energy ripple are also larger. In the whole range, the capacitor energy storage requirement for HMMR is around 38% lower than MMC. Whereas the rms value of CL current, which affects the power losses of the devices, has a 10% difference between two topologies.

C. Semiconductor Losses

Another important aspect is efficiency, whose major part are the conduction and switching losses of the power devices. The characteristics (e.g., V_{ce}, E_{on}, and E_{off}) of IGBTs and diodes are obtained from the datasheet provided by the manufacturer with linear interpolation. Then the detailed calculation methods have been discussed a lot in [33] and [42], which are omitted in this paper.

Using these methods, the SM conduction losses distribution could help to optimize the thermal design of UCH-SM. The current definition of diode stack and SM of HMMR is shown in Fig. 17(a). The upper arm current i_{pa} flows out of two diode stacks and flows in to the UCH-SM, which has four parts: the left leg IGBT i_{LT} and diode i_{LD}, and right leg IGBT i_{RT} and diode i_{RD}. Since the CL voltage and current reference are known, the current distribution of four components inside one UCH-SM over one line cycle could be derived as shown in Fig. 17(b).

In this way, the semiconductor losses distribution for single UCH-SM and HV diode in HMMR at unity PF is calculated and presented as Fig. 18. Obviously, the left and right leg have almost same losses distribution, while LV IGBT shows higher losses compared to the LV diode. Besides, the conduction losses for extra 7.2 kV diode D_1 and D_2 are not high, which contributes to the lower total losses of HMMR.

The evaluation results in Fig. 19 indicate that the loss of HMMR at full-load and unity PF is 22% lower than that of MMC, even though it has a higher CL current rms value. This higher efficiency should be attributed to the smaller number of SMs and the natural commutation of the HV diode in HMMR.

The performance comparison between step-down HMMR and FB-MMC is summarized in Table II. The former could save around 40% SM number, 38% capacitor energy storage and 22% losses at unity PF. According [43], the system volume could be normalized to conventional FB-MMC with the expression below,

$$\begin{gathered} V = V_\alpha \frac{S_{sem(HMMR)}}{S_{sem(MMC)}} + V_\beta \frac{E_{HMMR}}{E_{MMC}} + V_\gamma \frac{N_{sm(HMMR)}}{N_{sm(MMC)}} \\ V_\alpha + V_\beta + V_\gamma = 100\% \end{gathered} \tag{21}$$

The corresponding weight coefficients for semiconductors, capacitors and accessory components are denoted as V_α, V_β and V_γ, respectively. These values vary in different voltage and power levels, and are selected as $V_\alpha = 30\%$, $V_\beta = 55\%$ and $V_\gamma = 15\%$ in this study based on the empirical data. Therefore, the total volume could be reduced to 0.63 p.u. at unity PF and 0.65 p.u. at PF of 0.9.

The system cost could be evaluated through similar method in (22).

$$\begin{gathered} C = C_\alpha \frac{S_{sem(HMMR)}}{S_{sem(MMC)}} + C_\beta \frac{E_{HMMR}}{E_{MMC}} + C_\gamma \frac{N_{sm(HMMR)}}{N_{sm(MMC)}} \\ C_\alpha + C_\beta + C_\gamma = 100\% \end{gathered} \tag{22}$$

In this study these coefficients are selected as $C_\alpha = 40\%$, $C_\beta = 37.5\%$ and $C_\gamma = 22.5\%$, respectively. As a result, the cost of HMMR normalized to FB-MMC could be calculated to be 0.64 p.u. at unity PF and 0.68 p.u. at PF of 0.9.

Above all, the proposed HMMR could improve the power density, efficiency and construction cost compared to the traditional FB-MMC for such step-down power conversion.

TABLE II
Overall converter comparison between step-down HMMR and FB-MMC

PF	1		0.9	
Topology	**MMC**	**HMMR**	**MMC**	**HMMR**
Device number	1 p.u.	0.6 p.u. (CL) + 0.1 p.u. (diode)	1 p.u.	0.6 p.u. (CL) + 0.13 p.u. (diode)
Capacitor	1 p.u.	0.62 p.u.	1 p.u.	0.62 p.u.
Device losses	1 p.u.	0.78 p.u.	1 p.u.	0.69 p.u.
Volume	1 p.u.	0.63 p.u.	1 p.u.	0.65 p.u.
Cost	1 p.u.	0.64 p.u.	1 p.u.	0.68 p.u.

D. AC Low Voltage Ride Through and Dc Fault Ride Through

Despite the diode structure, the step-down HMMR belongs to VSC. Therefore, it does not require a strong grid and can ride through the ac low voltage and dc faults.

In the traditional boost rectifier, the dc voltage keeps constant during the ac low voltage ride through. However, the modulation index requirement should always be maintained for such step-down HMMR as discussed in Section II. One simple strategy is turning off all SMs to isolate the severe ac fault. Another strategy is reducing the dc side voltage accordingly to meet the minimum modulation index requirement if ac sag occurs. Since the dc bus voltage is reduced, some ISOP connected back-end dc/dc converters could be bypassed to ensure a small variation of the voltage conversion ratio. Alternatively, a diode can be connected between the HMMR and back-end dc/dc to withstand voltage during this transient. In this case, the operation of ISOP will not be affected.

Due to the utilization of UCH-SM, HMMR has the dc fault ride-through capability [41], [42]. It is well known that traditional boost rectifiers can only isolate the dc fault. On the contrary, the step-down HMMR is capable to ride through the dc fault by changing the dc output voltage reference to 0. Therefore, a soft voltage startup process could be achieved easily after the dc fault is cleared.

If the ac voltage is too high and exceeds the total CL capacitor voltage, the SM capacitor voltage V_{SM_dcf} will be charged to (23) with two series CL blocking the ac voltage.

$$V_{SM\_dcf} = \frac{\sqrt{3}V_{ac}}{2N_{SM}} \tag{23}$$

Taking the parameters in Table I as an example, V_{SM_dcf} of this HMMR will become 1.08 kV after the dc fault. If the SM capacitor voltage is charged too high in some extreme cases, then more SM should be added to block the pole-to-pole fault fully.

IV. Simulation and Experimental Results

A. Simulation Results

In order to validate the feasibility of the proposed step-down HMMR and the control method, a simulation model in Fig. 20 is built with the parameters listed in Table I. The ac side of HMMR connects to a three-phase voltage source, while the dc side connects to the resistor load without a dc filter.

Fig. 21 shows the steady-state unity PF operation results of HMMR. It can be seen that the ripple of dc side voltage V_{dc} in Fig. 21(c) is pretty small even without the dc filter. The trapezoidal current waveforms are given in Fig. 21(d), which are always positive and match the current constraint. The multilevel arm chain-link voltage is presented in Fig. 21(e), which helps to shape the ac side sinusoidal currents. It should be noted that the CL voltage fluctuation is due to the current loop output, which equals the voltage drop across the arm

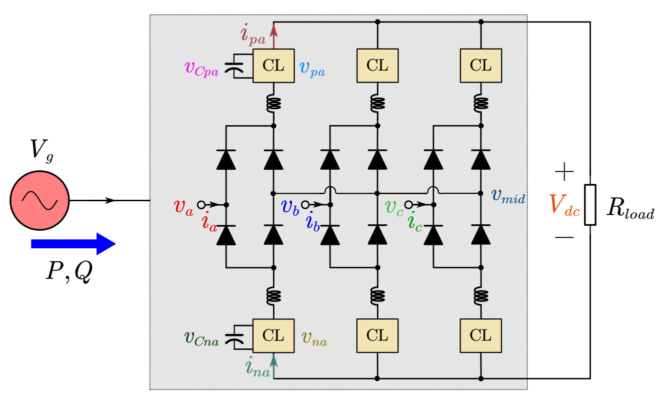


Fig. 20 Simulation model of HMMR with 13.8 kV grid and resistor load.

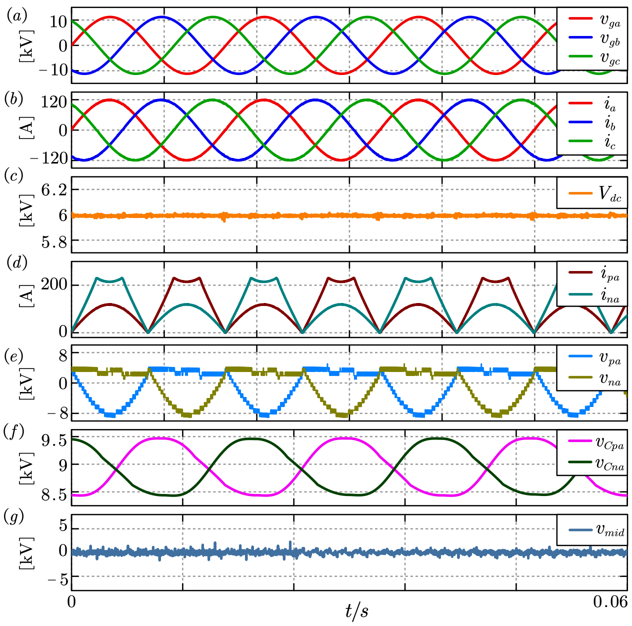


Fig. 21 Steady-state simulation waveforms of HMMR at unity PF, (a) ac grid side voltages, (b) ac side currents, (c) dc voltage, (d) phase *a* upper and lower arm currents, (e) phase *a* upper and lower CL output voltages, (f) phase *a* upper and lower CL capacitor voltage sums, (g) midpoint voltage potential.

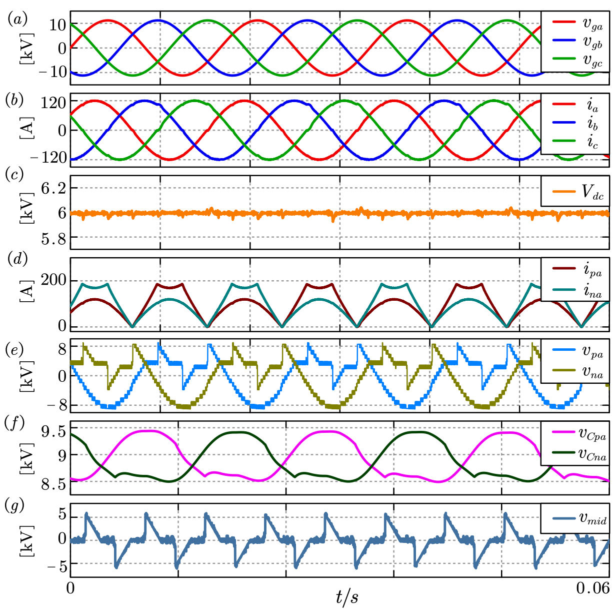


Fig. 22 Steady-state simulation waveforms of HMMR at non-unity PF, (a) ac grid side voltages, (b) ac side currents, (c) dc voltage, (d) phase *a* upper and lower arm currents, (e) phase *a* upper and lower CL output voltages, (f) phase *a* upper and lower CL capacitor voltage sums, (g) midpoint voltage potential.

inductor. Moreover, the voltage difference between two levels in Fig. 21(e) is same, which can reflects the SM capacitor voltage balancing inside one CL. Due to the balancing control, the CL capacitor voltage is balanced pretty well as shown in Fig. 21(f). As discussed earlier, the midpoint voltage V_{mid} is controlled to be 0 in unity PF and can be reflected in Fig. 21(g).

To validate the operation principle of HMMR at non-unity PF, a case with PF of 0.9 is performed as shown in Fig. 22. In

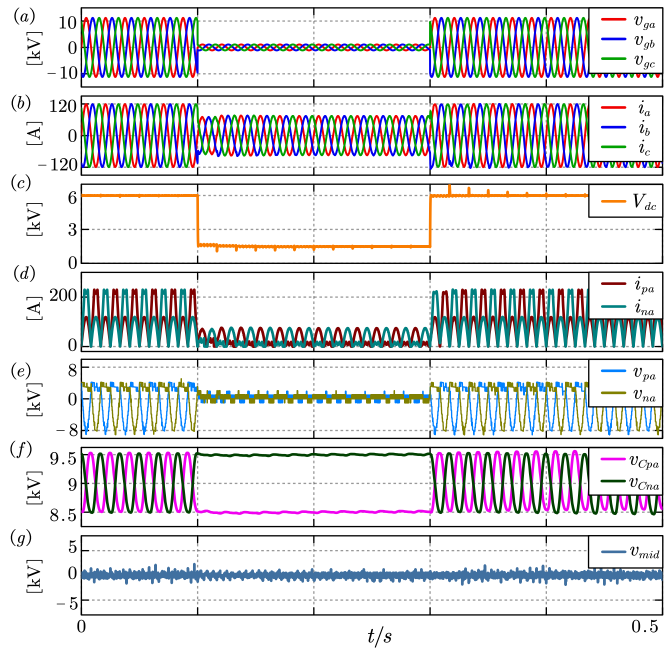


Fig. 23 Waveforms during the ac fault, (a) ac grid side voltages, (b) ac side currents, (c) dc voltage, (d) phase *a* upper and lower arm currents, (e) phase *a* upper and lower CL output voltages, (f) phase *a* upper and lower CL capacitor voltage sums, (g) midpoint voltage potential.

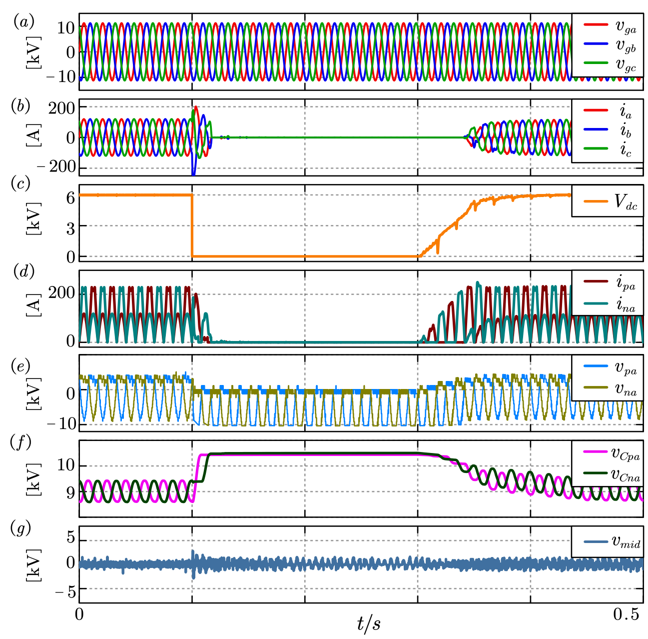


Fig. 24 Waveforms during the dc fault, (a) ac grid side voltages, (b) ac side currents, (c) dc voltage, (d) phase *a* upper and lower arm currents, (e) phase *a* upper and lower CL output voltages, (f) phase *a* upper and lower CL capacitor voltage sums, (g) midpoint voltage potential.

this case, states 3 and 4 should be used and the midpoint voltage V_{mid} in Fig. 22(g) changes to the phase voltage. In this case, the maximum CL voltage in Fig. 22(e) becomes higher and the SM number is still enough so that the over-modulation does not occur. The upper and lower CL currents in Fig. 22(d) are still positive and the dc voltage ripple in Fig. 22(c) is quite small, too.

To evaluate the ac low voltage ride-through capability, a symmetrical ac sag is applied at t = 0.1 s and cleared after 0.2 s as illustrated in Fig. 23. The grid voltage amplitude reduces to 0.1 p.u. in Fig. 23(a), and the dc output voltage reference also changes to 0.25 p.u. to follow the modulation index requirement. Since the dc load resistor does not change, the ac current amplitude is determined by the total active power and becomes lower. Besides, the capacitor voltage ripple in Fig. 23(f) becomes much smaller. After fault clearance t = 0.3 s, the power transmission resumes and the system autonomously restores normal operation. During the whole process, the midpoint voltage Fig. 23(g) keeps around 0.

Another important case is the dc fault ride-through as shown in Fig. 24. The dc fault is applied at t = 0.1 s and the ride through strategy is activated after 1 ms, so that the ac side over current may occur. During the dc fault, the ac voltage exceeds two series maximum CL voltage as shown in Fig. 24(e), so the SM capacitor is charged higher than the rated value in Fig. 24(f). As long as this voltage does not exceed the FB device blocking voltage, it is still acceptable. After fault clearance at t = 0.3 s, the dc voltage in Fig. 24(c) starts to increase gradually and a soft start-up could be achieved.

B. Experimental Results

A sub-scale medium voltage prototype as shown in Fig. 25(a) was built to validate the operation of a step-down HMMR. The schematic for single-phase and three-phase configuration are shown in Fig. 25(b) and Fig. 25(c), respectively. And the corresponding parameters are listed in Table III. The FB SM is built with the 1.7 kV discrete SiC MOSFET (G3R20MT17K) due to high switching frequency capability to reduce current ripple. All four PWM signals, one SM fault signal as well as the SM capacitor voltage information are transmitted between the controller and each SM. To reduce the fiber number, the serial communications interface (SCI) protocol is adopted here to send back the SM capacitor voltage. In order to suppress the arm current ripple with single SM per arm, the 2 mH arm inductor is used in this setup.

The setup controller is established by using the DSP (TMS320F28379D from TI) + FPGA (5CEFA4F23C8N from Altera) structure. The DSP should also manage all the fault feedback signals including the SM faults, the IGBT module

TABLE III
Electrical parameters of step-down HMMR system.

Parameters	Symbol	Values	
		Single-phase	Three-phase
Ac peak to peak amplitude	$V_{pk\ to\ pk}$	1.4 kV	850 V
Rated ac frequency	f_{ac}	60 Hz	60 Hz
Dc bus voltage	V_{dc}	350 V	300 V
Dc load resistor	R_o	117 Ω	11.3 Ω
Arm inductance	L_{arm}	2 mH	2 mH
SM voltage	V_{SM}	400 V	350 V
SM capacitance	C_{SM}	0.66 mF	1 mF
Number of FB SM per arm	N_f	2	1
Carrier frequency	f_c	20 kHz	20 kHz
Power factor	PF	1	1/0.9
Power density	-	2.75 kW/m^3	6.55 kW/m^3
Power efficiency	-	95.2%	96.9%

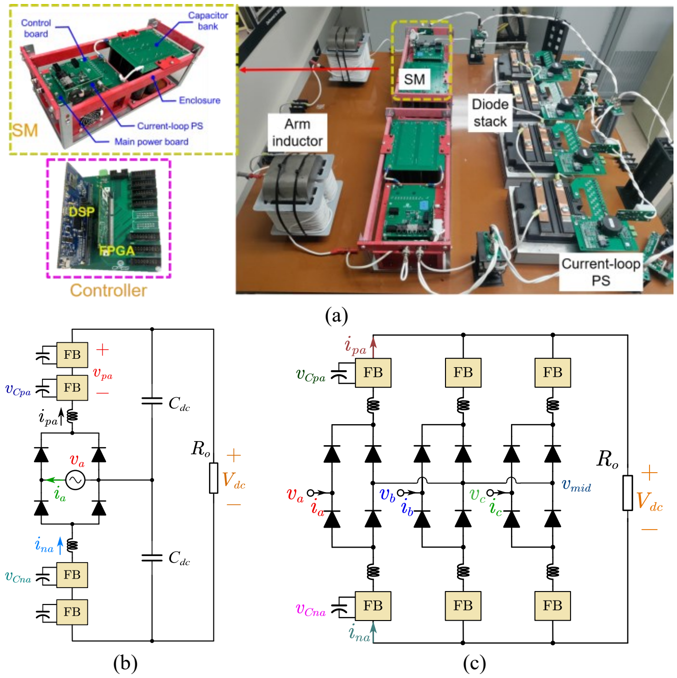


Fig. 25 (a) Picture of one layer of three-phase HMMR setup, (b) schematic of single-phase HMMR test setup, (b) schematic of three-phase HMMR test setup.

faults, as well as the over-current/voltage faults. As for the FPGA, it is responsible for many duplicated jobs, including the SM PWM signals generation, SCI communication with different sensors, and receiving all fault signals. FPGA receives all the measurement data, which is then passed to the DSP for the closed-loop algorithm and generation of the SM duty cycle.

For the HMMR, the floating DC link capacitor needs to be charged to the rated value before normal operation. As shown in Fig. 26, the relay K is opened, and limiting resistor R_{limit} could be inserted. In this way, a charging current path is generated as the red dashed line when the ac voltage v_a is positive. The corresponding negative cycle charge path could be derived similarly. It should be noted that the dc output voltage will be discharged to 0 quickly due to the load resistor R_o. And the steady-state capacitor voltage could be calculated according to (23). Then the soft startup could be designed with a ramp reference for the output dc voltage.

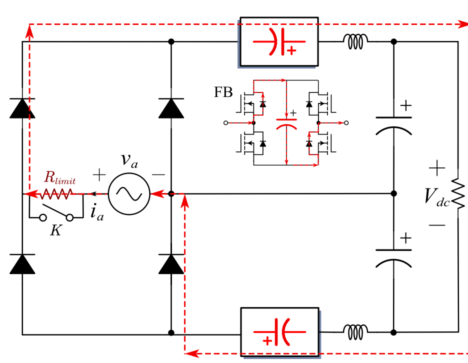


Fig. 26 One precharge path for the single-phase HMMR.

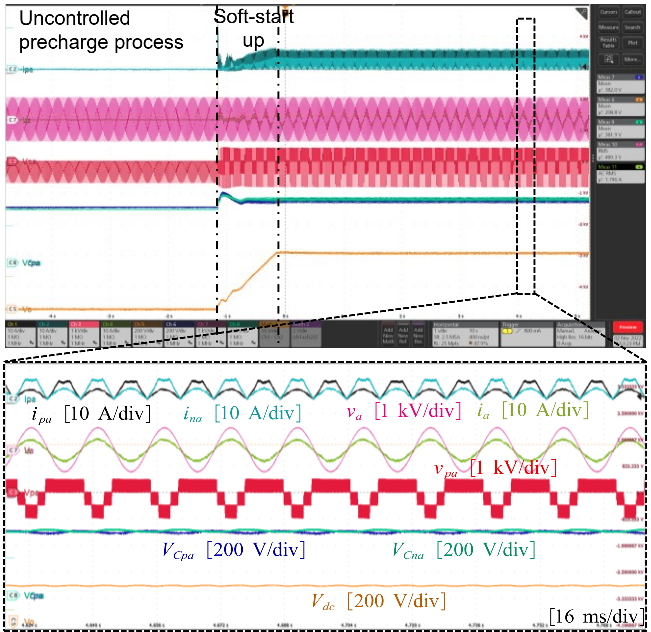


Fig. 27 Startup process of single-phase HMMR and the steady-state operation waveforms.

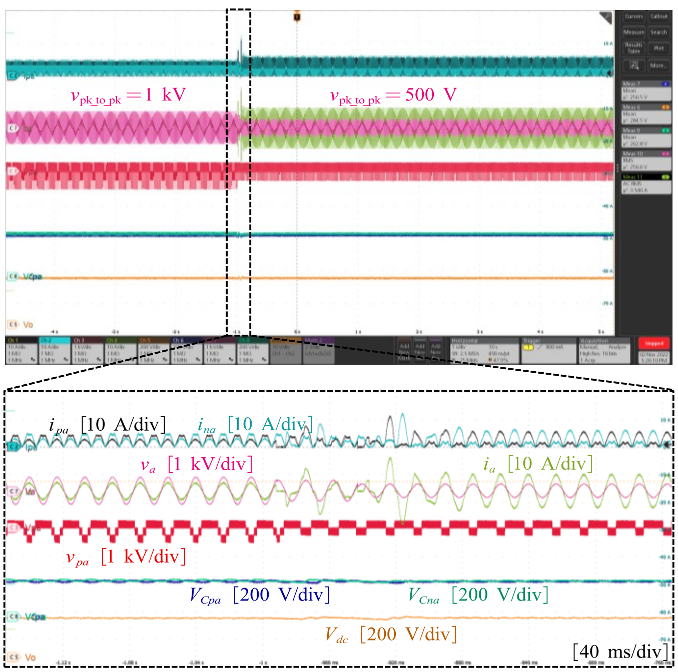


Fig. 28 The dynamic waveforms with the ac voltage changing from 1 kV to 500 V.

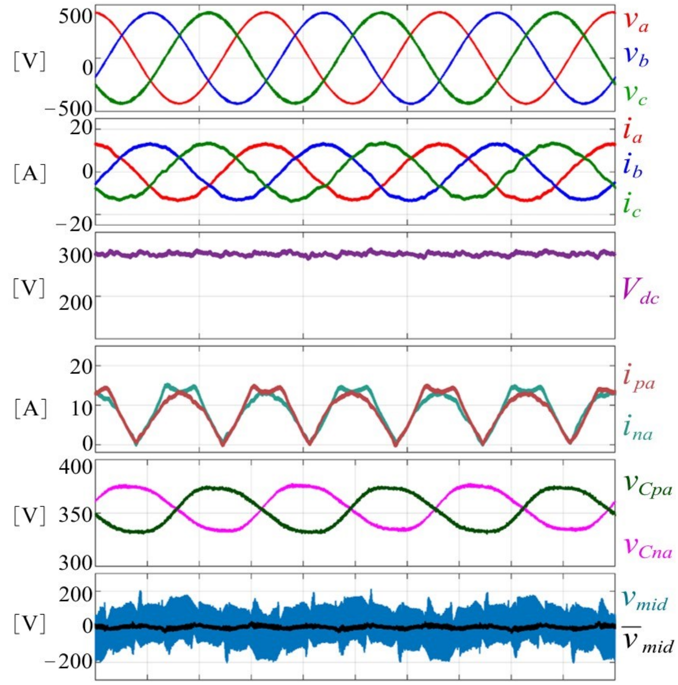


Fig. 29 Three-phase test waveforms of HMMR at unity PF.

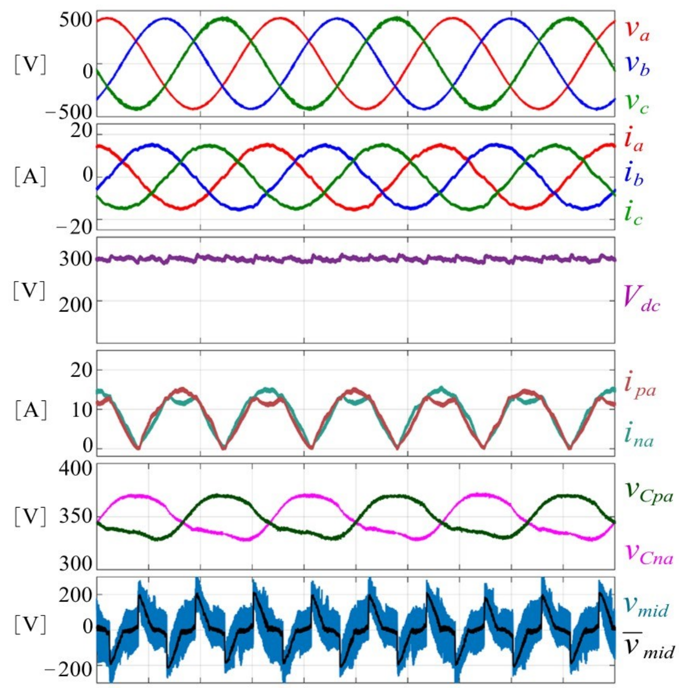


Fig. 30 Three-phase test waveforms of HMMR at PF of 0.9.

The single-phase test results are given in Fig. 27. It can be seen that the startup process matches the analysis. The steady-state zoomed-in waveforms demonstrate a good ac side current waveform and the stable SM floating capacitor voltage as well as the dc output voltage. The upper and lower arm currents are always positive and have the same shape in Fig. 8. Since two FB SMs are used in each arm, 4-level waveform is generated through the upper CL. Moreover, the same voltage level indicates the good SM voltage balancing between 2 SMs of upper CL.

To evaluate the performance of the control scheme during transients, the input ac voltage $v_{pk\_to\_pk}$ decreases from 1 kV to 500 V and key waveforms obtained are presented in Fig. 28. During the transient, it can be observed that the ac side current recovers to the sinusoidal shape after several cycles. This is owing to the response time of the phase-locked loop (PLL), and the ac source needs to change to 750 V before changing to 500V directly. The SM capacitor voltage ripple becomes smaller due to the smaller active power. The arm voltage level changes from 4-level to 3-level and the dc output voltage always keeps constant.

In order to validate the three-phase operation, the three-phase HMMR with one SM per arm was built, too. The corresponding waveforms of PF = 1 and 0.9 are given in Fig. 29 and Fig. 30, respectively. Without any dc side capacitor, the dc output voltage is stable and has a small ripple due to the designed trapezoidal current allocation. The difference between the two cases is the midpoint voltage V_{mid}, which needs to shift to the ac side voltage during the non-overlap period.

VI. Conclusions

In this paper, we propose a new step-down HMMR as a unidirectional AFE suitable for EV FCS and data center applications. By incorporating a HV diode, our proposed HMMR offers improved power density and efficiency over traditional FB-MMC, making it a competitive choice for applications requiring MVac to LVdc power conversion.

In the specific case of converting 13.8 kV ac to 6 kV dc, our proposed HMMR achieves approximately 40% reduction in the number of SMs, a 38% decrease in capacitor energy storage, and a 22% reduction in losses when compared to MMCs. This reduction in components not only contributes to cost savings but also enhances overall system power density.

Furthermore, HMMR offers an additional notable benefit of dc fault ride-through capability, which enables zero dc output startup. This feature expands the potential applications of our proposed HMMR to include motor drive systems.

Overall, our research demonstrates the advantages of the proposed HMMR as a high-performance and efficient AFE solution for EV FCS, data centers, and motor drive applications.

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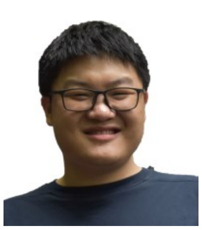
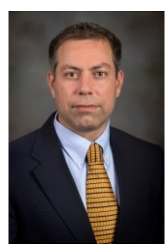


Jian Liu (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from Zhejiang University, Hangzhou, China, in 2016 and 2019, respectively. He is currently working toward the Ph.D. degree in the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA.

His current researches are in the areas of multilevel converters and Hybrid DC circuit breaker.

Mr. Liu is the recipient of the best paper award of ECCE-Asia 2020 and the outstanding presentation award of APEC 2021.

Jayesh Kumar Motwani (Student Member, IEEE) received the Integrated Dual Degree (B.Tech. in electrical engineering and M.Tech. in power electronics) from the Department of Electrical Engineering, Indian Institute of Technology (B.H.U.), Varanasi, India, in 2020. He is currently working toward a Ph.D. degree at the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA. He was a Visiting Scholar with the Politecnico di Milano, Milan, Italy, and Duke University, Durham, NC, USA, in 2018 and 2019, respectively, where he worked on modular converters. His research interests include modeling large power-electronic systems, control of modular power converters, integration of renewable energy systems, and wide-bandgap semiconductor applications. Mr. Motwani is the recipient of 3rd Prize Paper Award at IEEE International Power Electronics Conference, 2022.



Rolando Burgos (S'96–M'03–SM'20) received the B.S. on Electronics Engineering, the Electronics Engineering Professional Degree, and the M.S. and Ph.D. degrees in Electrical Engineering from the University of Concepción, Chile, in 1995, 1997, 1999, and 2002 respectively. In 2002 he joined, as Postdoctoral Fellow, the Center for Power Electronics Systems (CPES) at Virginia Tech, in Blacksburg, VA, becoming Research Scientist in 2003, and Research Assistant Professor in 2005. In 2009 he joined ABB Corporate Research in Raleigh, NC, where he was Scientist (2009–2010), and Principal Scientist (2010–2012). In 2010 he was appointed Adjunct Associate Professor in the Electrical and Computer Engineering Department at North Carolina State University at the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center. In 2012 he returned to Virginia Tech as associate professor in The Bradley Department of Electrical and Computer Engineering, where he earned his tenure in 2017, was promoted to professor in 2019. Since 2021 he has been the Director of CPES. His research interests include high power density wide-bandgap semiconductor-based power conversion—low voltage and medium voltage applications, packaging and integration, electromagnetic interference (EMI) and electromagnetic compatibility (EMC), multi-phase multi-level power converters, modeling and control, grid power electronics systems, and the stability of ac and dc power systems.

Dr. Burgos is Member of the IEEE Power Electronics Society where he currently serves as Associate Editor of the IEEE Transactions on Power Electronics, and the IEEE Journal of Emerging and Selected Topics in Power Electronics. He is the past Chair of the Technical Committee on Power and Control Core Technologies. Dr. Burgos is also a member of the IEEE Industry Applications Society, the IEEE Industrial Electronics Society, and the IEEE Power and Energy Society.

Dong Dong (S'09–M'12–SM'20) received the B.S. degree from Tsinghua University, China, in 2007, and the M.S. and Ph.D. degrees from Virginia Tech, Blacksburg, VA, USA, in 2009 and 2012, both in electrical engineering.

From 2012 to 2018, he was with GE Global Research Center (GRC), Niskayuna, NY, USA, as an Electrical Engineer. At GE, he participated in and led multiple technology programs including MV/HVDC power distribution and power delivery, SiC high-frequency high-power conversion systems, solid-state transformers, and energy storage system. He received multiple technology awards including GE silver and gold medallion patent awards and GE technology transition awards. Since 2018, he has been with the Bradley Department of Electrical and Computer Engineering, Virginia Tech. He has published over 45 referred journal publications and more than 100 IEEE conference publications. He currently holds 34 granted US patents. His research interests include wide-band-gap power semiconductor-based high frequency power conversion, soft-switching and resonant converters, high-frequency transformers, and MV and HV power conversion system for grid, renewable, and transportation applications. Dr. Dong is currently an Associate Editor for IEEE Transactions on Power Electronics. He received two Transaction Prize Paper Awards from the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, William Portnoy Prize Paper Award and Transportation Systems Prize Paper Award from IEEE IAS, and NSF CAREER award. He served as the Vice Chair of IEEE Industry Application Society Schenectady Region Chapter in 2017 and General Chair of IEEE International Conference on DC Microgrids in 2021.