# 10 kV $Ga_2O_3$ Charge-Balance Schottky Rectifier Operational at 200 °C

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***Abstract*—This work demonstrates a lateral $Ga_2O_3$ Schottky barrier diode (SBD) with a breakdown voltage (*BV*) over 10 kV, the highest *BV* reported in $Ga_2O_3$ devices to date. The 10 kV SBD shows good thermal stability up to 200 °C, which is among the highest operational temperatures reported in multi-kilovolt $Ga_2O_3$ devices. The key device design for achieving such high *BV* is a reduced surface field (RESURF) structure based on the p-type nickel oxide (NiO), which balances the depletion charges in the n-$Ga_2O_3$ channel at high voltage. At *BV*, the charge-balanced $Ga_2O_3$ SBD shows an average lateral electric field (E-field) over 4.7 MV/cm at 25 °C and over 3.5 MV/cm at 200 °C, both of which exceed the critical E-field of GaN and SiC. The 10 kV SBD shows a specific on-resistance of 0.27 Ω·cm² and a turn-on voltage of 1 V; at 200 °C, the former doubles and the latter reduces to 0.7 V. These results suggest the good potential of $Ga_2O_3$ devices for medium- and high-voltage, high-temperature power applications.[1]**

***Index Terms*— power electronics, ultra-wide bandgap, gallium oxide, Schottky diode, nickel oxide, RESURF, high voltage.**

## I. Introduction

Medium-voltage (MV, >1 kV) power devices are widely used in electric grid, motor drive, and renewable energy processing. Today's commercial MV devices are dominated by bipolar Si devices up to 6.5 kV, which suffer from slow switching speed. Wide-bandgap (WBG) materials have enabled fast, unipolar MV devices [1]. SiC devices are commercialized up to 3.3 kV with industrial samples available up to 10 kV [2]. GaN devices recently reached the 10 kV milestone [3], [4].

Ultra-wide bandgap (UWBG) materials hold superior limits for MV devices [1]. While UWBG devices have not reached 10 kV, gallium oxide ($Ga_2O_3$) is approaching. Breakdown voltage (*BV*) from 3 kV up to 8.56 kV has been reported in $Ga_2O_3$-based lateral [5], [6] and vertical diodes [7]–[11] as well as lateral MOSFETs [12]–[15]. Additionally, the availability of high-quality 4-inch wafers [16] and the reports of high-performance packaging, device robustness, and converter applications [17] all consolidate the promise of $Ga_2O_3$ for power electronics.

Upscaling *BV* in power devices hinges on the suppression of crowded electric field (E-field) at the edge or surface and the reduction of charge density in the drift region. The p-n junction is the major structure to achieve such functionality in 10 kV SiC [18] and GaN [3] devices. It can also enable high thermal stability [19] and robustness [20]. As the p-type conductivity is not available in $Ga_2O_3$, a heterojunction between n-$Ga_2O_3$ and p-type, WBG nickel oxide (NiO) have been deployed in many MV devices [6], [8], [9], [11], [21]. However, very few high-temperature operations have been reported in multi-kilovolt $Ga_2O_3$ devices, hindering their adoption in practical power applications in which devices are required to reliably operate under a junction temperature of at least 150-175 °C.

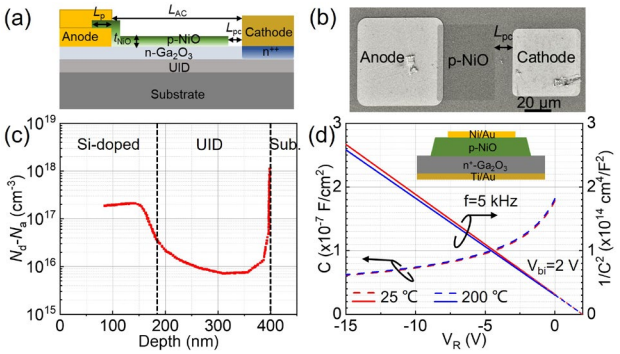


Fig. 1. (a) Cross-view schematic diagram and (b) top-view SEM image of the fabricated lateral $Ga_2O_3$ RESURF SBD. (c) The $N_d$-$N_a$ depth profile of the $Ga_2O_3$ epi layers (the initial depletion of the Schottky contact is ~85 nm). (d) C-V and $1/C^2$-V characteristics of the vertical NiO/$Ga_2O_3$ diode at 25 °C and 200 °C.

This work demonstrates a new lateral $Ga_2O_3$ Schottky barrier diode (SBD) with *BV* >10 kV at high temperatures up to 200 °C. Distinct from prior lateral NiO/$Ga_2O_3$ p-n diodes [6], this SBD deploys NiO to form a charge-balance RESURF structure while retaining the low turn-on voltage ($V_{on}$) of SBDs. Under reverse bias, the NiO RESURF structure enables nearly zero net charge in the lateral drift region, boosting the average E-field and *BV*. The $Ga_2O_3$ SBDs fabricated with various NiO thicknesses ($t_{NiO}$) and anode-to-cathode lengths ($L_{AC}$) validate the critical role of charge balance in achieving the high *BV*. As compared to the prior RESURF $Ga_2O_3$ MOSFETs with a *BV* up to 1.36 kV [22], [23], our device highlights a careful tailoring of charge balance and thereby achieves a much higher *BV*.

## II. Device Design and Fabrication

Fig. 1(a) and (b) show the cross-view schematic and top-view scanning electron microscope (SEM) image of the fabricated $Ga_2O_3$ RESURF SBD, respectively. Most of the fabricated SBDs have a $L_{AC}$ of 30 μm or 50 μm, and fewer have a $L_{AC}$ of 17 μm. A gap between the p-NiO layer and cathode is designed to prevent the possible leakage current and punch-through in NiO. The length of this gap ($L_{pc}$) is designed to be 7 μm, 10 μm

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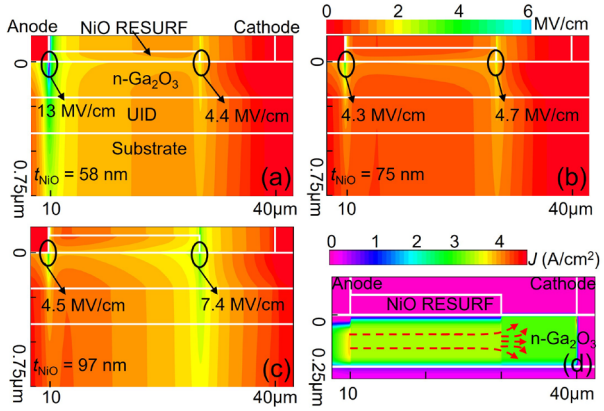


Fig. 2. Simulated E-field contour of $Ga_2O_3$ RESURF SBDs with $t_{NiO}$ of (a) 58 nm, (b) 75 nm, and (c) 97 nm, all at the 4 kV reverse bias. (d) Simulated current density contour of the 75-nm-NiO RESURF SBD at the 2 V forward bias. This simulated RESURF SBD has a $L_{AC}$ of 30 μm and $L_{pc}$ of 10 μm.

and 15 μm for the devices with $L_{AC}$ of 17 μm, 30 μm and 50 μm, respectively, rendering a similar ratio between the lengths of the $Ga_2O_3$ channel and NiO layer for different $L_{AC}$.

To achieve the charge balance, the net donor concentration ($N_d$-$N_a$) in $Ga_2O_3$ and acceptor concentration ($N_a$) in NiO need to be accurately measured at various temperatures. The $Ga_2O_3$ sample comprises a ~180 nm n-type layer and an unintentional doped (UID) layer grown on a (010) semi-insulating substrate by molecular-beam epitaxy. The $N_d$-$N_a$ depth profile is obtained by the electrochemical C-V (ECV) technique, as shown in Fig. 1(c). The $N_d$-$N_a$ integral along the depth reveals a total charge density ($\sigma_n$) of $3.8\times10^{12}$ $cm^{-2}$ in n-$Ga_2O_3$. The temperature-dependent C-V measurements on a test structure fabricated on the n-$Ga_2O_3$ layer reveal a minimal change in $\sigma_n$ up to 200 °C.

To extract the $N_a$, a NiO/$Ga_2O_3$ p-n diode is fabricated on a (001) $n^+$-$Ga_2O_3$ substrate with $N_d$ of $8.3\times10^{18}$ $cm^{-3}$ (Fig. 1(d)). A relative thick NiO with a thickness of 400 nm is used in this test structure to avoid the NiO punch-through at low reverse bias. To reduce the impact of $t_{NiO}$ variation on charge balance and enable a larger process latitude, a lower $N_a$ is preferred. Recent studies revealed that the $N_a$ of the sputtered NiO can be reduced by lowering the $O_2$ partial pressure during the sputtering [24], [25]. In this work, the NiO is sputtered in a pure Ar atmosphere at room temperature and annealed at 275 °C in $N_2$. At a reverse bias ($V_R$), the capacitance of the NiO/$Ga_2O_3$ diode is [24]

$$C = \left[\frac{q\varepsilon_n\varepsilon_p\varepsilon_0 N_d N_a}{2(\varepsilon_n N_d+\varepsilon_p N_a)}\right]^{1/2}(V_{bi}-V_R)^{-1/2} \quad (1)$$

where $\varepsilon_0$, $\varepsilon_n$ and $\varepsilon_p$ are the vacuum permittivity and the relative permittivity of $Ga_2O_3$ and NiO, respectively; $V_{bi}$ is the built-in potential of the NiO/$Ga_2O_3$ junction (~2 V). Based on (1), $N_a$ is extracted to be $8\times10^{17}$ $cm^{-3}$ at 25 °C from $1/C^2$-V characteristics, and it show a very small change at 200 °C (Fig. 1(d)).

For practical fabrication of the RESURF SBD, if a charge imbalance margin is kept below 15%, the $t_{NiO}$ range can be estimated to be 69-92 nm, 61-82 nm, and 58-78 nm for $L_{AC}$ of 17, 30, and 50 μm, respectively, using the following relation

$$0.85 < Q_p/Q_n = N_a t_{NiO}(L_{AC}-L_{pc})/\sigma_n L_{AC} < 1.15 \quad (2)$$

where $Q_p$ and $Q_n$ are depletion charges in the p-NiO RESURF layer and the n-$Ga_2O_3$ channel, respectively.

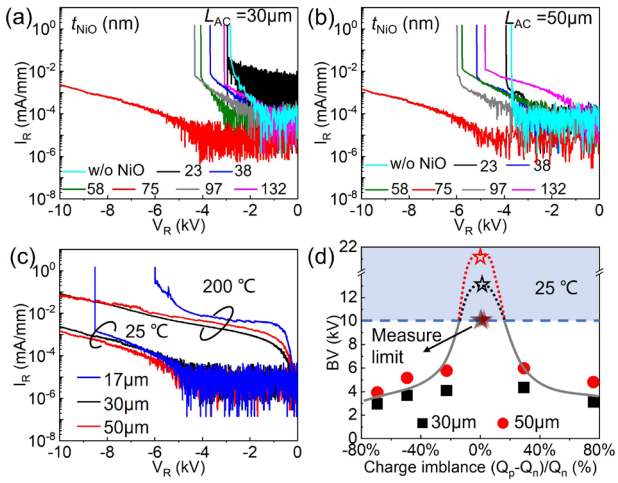


Fig. 3. Reverse I-V characteristics of the non-RESURF SBDs and RESURF SBDs with $L_{AC}$ of (a) 30 μm and (b) 50 μm, both with various $t_{NiO}$ from 23 nm to 132 nm. The measurement limit is 10 kV. (c) Reverse I-V characteristics of the 75-nm-NiO RESURF SBDs with three $L_{AC}$ at 25 °C and 200 °C. (d) $BV$ of $Ga_2O_3$ RESURF SBDs at 25 °C as a function of the charge imbalance percentage. The hollow symbols show the projected $BV$ of the 75-nm-NiO RESURF SBDs.

TCAD simulations are performed to verify the device design. Fig. 2(a)-(c) show the simulated E-field contours of RESURF SBDs with $t_{NiO}$ of 58, 75 and 97 nm. The insufficient and excessive $Q_p$ lead to E-field crowding at the anode and the NiO edge, respectively. The 75 nm $t_{NiO}$ allows for a balanced E-field at the two spots. Fig. 2(d) shows the simulated current density contour at a forward bias. The depletion effect of the forward-biased, vertical p-n junction shrinks the effective cross-section for current conduction, leading to a higher on-resistance ($R_{on}$).

The device fabrication starts with a Si implantation in the cathode region followed by a 925 °C activation in $N_2$. The cathode Ohmic contact is formed using the Ti/Au (30/150 nm) stack with a 470 °C annealing. Nitrogen implantation is then carried out for device isolation. The anode Schottky contact is formed using the Ni/Au (150/150 nm) stack. The p-NiO RESURF layer is sputtered with various $t_{NiO}$ and a common extension length ($L_p$) of 5 μm onto the anode. The sputtering is performed using a NiO target under the 60 sccm Ar, 3 mTorr pressure, and 100 W RF power. To form the Ohmic contact between anode and NiO, a second Ni/Au stack is deposited on top of the anode. A 275 °C post annealing is performed to stabilize $N_a$ in NiO and reduce the NiO/$Ga_2O_3$ interface states [25]. The device is passivated in a photoresist similar to [12], [13]. A control $Ga_2O_3$ SBD without the p-NiO RESURF layer is also fabricated.

## III. Device Characterization

Fig. 3(a) and (b) show the reverse I-V characteristics of the RESURF $Ga_2O_3$ SBDs with various $t_{NiO}$ for $L_{AC}$ of 30 μm and 50 μm, respectively. These two sets of devices show a similar $BV$ dependence on $t_{NiO}$. $BV$ increases with the increasing $t_{NiO}$, reaching >10 kV (the measurement limit of our test setup) at $t_{NiO}$ = 75 nm, and starts to decrease at larger $t_{NiO}$. This behavior manifests the critical role of charge balance. For RESURF $Ga_2O_3$ SBDs with $L_{AC}$ = 30 μm, the charge-balanced NiO RESURF design boosts the $BV$ from 2.8 kV to >10 kV,

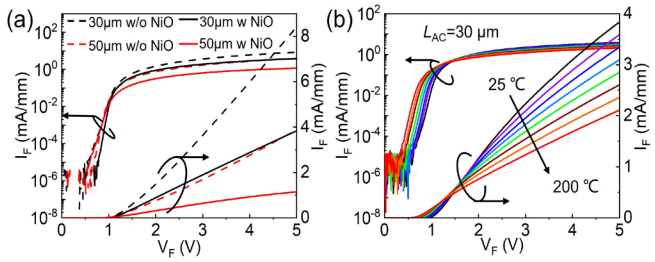


Fig. 4. (a) Forward I-V characteristics of the non-RESURF SBDs and RESURF SBDs, both with $L_{AC}$=30 μm and 50 μm. (b) Forward I-V characteristics of the 75-nm-NiO RESURF SBD with $L_{AC}$ = 30 μm at temperatures of 25 °C to 200 °C at a step of 25 °C. The data are plotted in both semi-log and linear scales.

rendering a high average lateral E-field ($E_{ave}$) over 3.3 MV/cm ($E_{ave}$=$BV/L_{AC}$).

Fig. 3(c) shows the reverse I-V characteristics of the 75-nm-NiO RESURF $Ga_2O_3$ SBDs at 25 °C and 200 °C for three $L_{AC}$. RESURF SBDs with $L_{AC}$=30 μm and 50 μm can be swept repeatedly up to 10 kV at both 25 °C and 200 °C. At 25 °C, $Ga_2O_3$ SBDs show a leakage current of $2\times10^{-6}$ A/mm at 10 kV, which is 10 times lower than that reported in 10 kV GaN SBDs [3]. At 200 °C, the leakage current increase at the 10 kV bias is less than 100 times, revealing the excellent thermal stability of RESURF $Ga_2O_3$ SBDs at high voltage.

To probe the $E_{ave}$ limit, the 75-nm-NiO RESURF SBDs with a shorter $L_{AC}$ of 17 μm are measured to destructive breakdown, revealing a $BV$ > 8 kV at 25 °C ($E_{ave}$ > 4.7 MV/cm) and 6.1 kV at 200 °C ($E_{ave}$ > 3.5 MV/cm). The $BV$'s negative temperature coefficient ($\eta_T$) suggests the lack of avalanche breakdown and implies a trap-assisted breakdown mechanism. The traps in bulk materials or at the heterogeneous interfaces could induce additional leakage current and form fixed charges. The excessive leakage current can lead to power (or thermal) limited breakdown at a lower voltage. The fixed charges could impair the charge balance that is key to high $BV$, resulting in early breakdown. Moreover, such trapping dynamics are usually more active at high temperatures, which explains the $BV$'s negative $\eta_T$.

Despite the temperature dependence, the $E_{ave}$ is higher than the critical E-field of GaN and SiC as well as the $E_{ave}$ (~1 MV/cm) reported in 10 kV lateral GaN devices [3], [4], manifesting one advantage of UWBG $Ga_2O_3$ devices.

For devices with $L_{AC}$ of 30 and 50 μm and various $t_{NiO}$, Fig. 3(d) plots their $BV$ as a function of the charge imbalance percentage calculated from (2), where the $BV$ of 75-nm-NiO RESURF devices are projected assuming a breakdown $E_{ave}$ equal to 90% of the value measured from the shorter device. The inverter U-shape curve manifest the determining impact of charge balance on the $BV$.

Fig. 4(a) shows the forward I-V characteristics of the non-RESURF SBDs and 75-nm-NiO RESURF SBDs, both with $L_{AC}$=30 μm and 50 μm. The $V_{on}$, Schottky barrier height, and ideality factor of all devices are similar, being 1 V, 0.74 eV, and 1.2, respectively. The differential on-resistance ($R_{on}$) of RESURF SBDs is higher than non-RESURF SBDs, with the ratio being ~2 for $L_{AC}$ = 30 μm and ~2.5 for $L_{AC}$ = 50 μm. This can be explained by the simulation results in Fig. 2(d), verifying the RESURF structure's adverse impact on device $R_{on}$. Note that, despite a doubled $R_{on}$, the RESURF design boosts the $BV$ by at least 3.5 times, rendering at least 5 times improvement in the device's Baliga's figure of merit (FOM = $BV^2/R_{on}$).

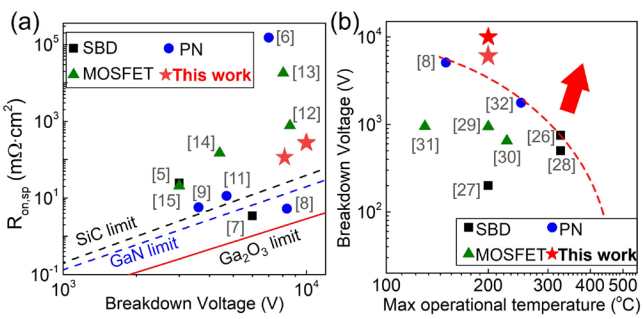


Fig. 5. (a) Benchmark of the differential $R_{on,sp}$ *vs.* $BV$ for our $Ga_2O_3$ RESURF SBD and the reported $Ga_2O_3$ SBDs, p-n diodes, and transistors with $BV$ >3 kV. (b) The $BV$ *vs.* max operational temperature benchmark for our device and the reported high-temperature $Ga_2O_3$ SBDs, p-n diodes, and transistors with $BV$ >100 V. The dotted line shows an approximate boundary of the prior data. The arrow shows the desirable target. Note that, in both sub-figures, the 10 kV $BV$ of the device fabricated in this work reflects the measurement limit instead of the device's intrinsic $BV$.

The specific $R_{on}$ ($R_{on,sp}$) of the 75-nm-RESURF SBDs with $L_{AC}$ = 30 μm is calculated to be 0.27 Ω·cm² using $R_{on,sp}$ = $R_{on}\cdot(L_{AC}+L_T+L_E)$, where $R_{on}$ in Ω·mm is extracted from the I-V curve, $L_T+L_E$ is the sum of the cathode contact transfer length and anode contact extension length (3 μm used here). Fig. 4(b) shows the forward I-V characteristics of this RESURF SBD at various temperatures. At 200 °C, $V_{on}$ is reduced to ~0.7 V, $R_{on}$ almost doubles, and the on/off ratio remains over $10^6$. The $R_{on,sp}$ of the 75-nm-NiO RESURF SBDs with $L_{AC}$=17 μm is 0.08 Ω·cm² at 25 °C and shows a similar temperature dependence.

Fig. 5(a) benchmarks the $R_{on,sp}$ versus $BV$ for our devices and the reported MV $Ga_2O_3$ SBDs [5], [7], p-n diodes [8]–[11], and MOSFETs [12]–[15] with $BV$ > 3 kV. Fig. 5(b) compares the $BV$ versus the maximum operational temperature reported for high-temperature $Ga_2O_3$ devices with $BV$ > 100 V [8], [26]–[32]. Our RESURF $Ga_2O_3$ SBDs show the highest $BV$, and the operational temperature is among the highest in multi-kilovolt $Ga_2O_3$ devices. The Baliga's FOM of 17 μm-$L_{AC}$ devices is 906 MW/cm² at 25 °C. The FOM of the 200 °C-operational, 10 kV-class device ($L_{AC}$ =30 μm) is at least 370 MW/cm² at 25 °C (the true FOM is expected to be much higher due to $BV$ > 10 kV).

## IV. Summary

This work presents a new charge-balance, NiO-RESURF $Ga_2O_3$ SBD that has achieved a $BV$ over 10 kV, with thermally-stable 10 kV blocking up to 200 °C as well as an $E_{ave}$ over 4.7 MV/cm and 3.5 MV/cm at 25 °C and 200 °C, respectively. Key to the device design is the p-NiO RESURF layer that enables precise charge balance with the n-$Ga_2O_3$ channel at high bias. These results suggest the good potential of $Ga_2O_3$ devices for medium- and high-voltage, high-temperature applications.

## REFERENCES


[1] Y. Zhang, F. Udrea, and H. Wang, "Multidimensional device architectures for efficient power electronics," *Nat. Electron.*, vol. 5, no. 11, Art. no. 11, Nov. 2022, doi: 10.1038/s41928-022-00860-5.

[2] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193–8205, Oct. 2017, doi: 10.1109/TIE.2017.2652401.

[3] M. Xiao, Y. Ma, K. Liu, K. Cheng, and Y. Zhang, "10 kV, 39 mΩ·cm2 Multi-Channel AlGaN/GaN Schottky Barrier Diodes," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 808–811, Jun. 2021, doi: 10.1109/LED.2021.3076802.

[4] M. Xiao, Y. Ma, Z. Du, V. Pathirana, K. Cheng, A. Xie, E. Beam, Y. Cao, F. Udrea, H. Wang, and Y. Zhang, "Multi-Channel Monolithic-Cascode HEMT (MC2-HEMT): A New GaN Power Switch up to 10 kV," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2021, p. 5.5.1-5.5.4. doi: 10.1109/IEDM19574.2021.9720714.

[5] Z. Hu, H. Zhou, Q. Feng, J. Zhang, C. Zhang, K. Dang, Y. Cai, Z. Feng, Y. Gao, X. Kang, and Y. Hao, "Field-Plated Lateral β -Ga2O3 Schottky Barrier Diode With High Reverse Blocking Voltage of More Than 3 kV and High DC Power Figure-of-Merit of 500 MW/cm2," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1564–1567, Oct. 2018, doi: 10.1109/LED.2018.2868444.

[6] H.-H. Wan, J.-S. Li, C.-C. Chiang, X. Xia, F. Ren, H. N. Masten, J. S. Lundh, J. A. Spencer, F. Alema, A. Osinsky, A. G. Jacobs, K. Hobart, M. J. Tadjer, and S. J. Pearton, "NiO/β-(AlxGa1−x)2O3/Ga2O3 heterojunction lateral rectifiers with reverse breakdown voltage >7 kV," *J. Vac. Sci. Technol. A*, vol. 41, no. 3, p. 032701, Mar. 2023, doi: 10.1116/6.0002393.

[7] P. Dong, J. Zhang, Q. Yan, Z. Liu, P. Ma, H. Zhou, and Y. Hao, "6 kV/3.4 mΩ·cm2 Vertical β-Ga2O3 Schottky Barrier Diode With BV2/Ron,sp Performance Exceeding 1-D Unipolar Limit of GaN and SiC," *IEEE Electron Device Lett.*, vol. 43, no. 5, pp. 765–768, May 2022, doi: 10.1109/LED.2022.3160366.

[8] J. Zhang, P. Dong, K. Dang, Y. Zhang, Q. Yan, H. Xiang, J. Su, Z. Liu, M. Si, J. Gao, M. Kong, H. Zhou, and Y. Hao, "Ultra-wide bandgap semiconductor Ga2O3 power diodes," *Nat. Commun.*, vol. 13, no. 1, Art. no. 1, Jul. 2022, doi: 10.1038/s41467-022-31664-y.

[9] M. Xiao, B. Wang, J. Spencer, Y. Qin, M. Porter, Y. Ma, Y. Wang, K. Sasaki, M. Tadjer, and Y. Zhang, "NiO junction termination extension for high-voltage (>3 kV) Ga2O3 devices," *Appl. Phys. Lett.*, vol. 122, no. 18, p. 183501, May 2023, doi: 10.1063/5.0142229.

[10] J.-S. Li, C.-C. Chiang, X. Xia, H.-H. Wan, F. Ren, and S. J. Pearton, "7.5 kV, 6.2 GW cm−2 NiO/β-Ga2O3 vertical rectifiers with on–off ratio greater than 1013," *J. Vac. Sci. Technol. A*, vol. 41, no. 3, p. 030401, Apr. 2023, doi: 10.1116/6.0002580.

[11] J.-S. Li, C.-C. Chiang, X. Xia, T. J. Yoo, F. Ren, H. Kim, and S. J. Pearton, "Demonstration of 4.7 kV breakdown voltage in NiO/β-Ga2O3 vertical rectifiers," *Appl. Phys. Lett.*, vol. 121, no. 4, p. 042105, Jul. 2022, doi: 10.1063/5.0097564.

[12] S. Sharma, L. Meng, A. F. M. A. U. Bhuiyan, Z. Feng, D. Eason, H. Zhao, and U. Singisetti, "Vacuum Annealed β-Ga2O3 Recess Channel MOSFETs With 8.56 kV Breakdown Voltage," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2029–2032, Dec. 2022, doi: 10.1109/LED.2022.3218749.

[13] S. Sharma, K. Zeng, S. Saha, and U. Singisetti, "Field-Plated Lateral $Ga_2O_3$ MOSFETs With Polymer Passivation and 8.03 kV Breakdown Voltage," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 836–839, Jun. 2020, doi: 10.1109/LED.2020.2991146.

[14] A. Bhattacharyya, S. Sharma, F. Alema, P. Ranga, S. Roy, C. Peterson, G. Seryogin, A. Osinsky, U. Singisetti, and S. Krishnamoorthy, "4.4 kV β-Ga2O3 MESFETs with power figure of merit exceeding 100 MW cm−2," *Appl. Phys. Express*, vol. 15, no. 6, p. 061001, May 2022, doi: 10.35848/1882-0786/ac6729.

[15] A. Bhattacharyya, S. Roy, P. Ranga, C. Peterson, and S. Krishnamoorthy, "High-Mobility Tri-Gate β-Ga2O3 MESFETs With a Power Figure of Merit Over 0.9 GW/cm2," *IEEE Electron Device Lett.*, vol. 43, no. 10, pp. 1637–1640, Oct. 2022, doi: 10.1109/LED.2022.3196305.

[16] C.-H. Lin, K. Ema, S. Masuya, Q. T. Thieu, R. Sakaguchi, K. Sasaki, and A. Kuramata, "Uniformity improvement of thickness and net donor concentration in halide vapor phase epitaxial β-Ga2O3 wafers prepared on miscut angle substrates," *Jpn. J. Appl. Phys.*, vol. 62, no. SF, p. SF1005, Feb. 2023, doi: 10.35848/1347-4065/acb4fb.

[17] Y. Qin, Z. Wang, K. Sasaki, J. Ye, and Y. Zhang, "Recent progress of Ga2O3 power technology: large-area devices, packaging and applications," *Jpn. J. Appl. Phys.*, vol. 62, no. SF, p. SF0801, Feb. 2023, doi: 10.35848/1347-4065/acb3d3.

[18] W. Sung, E. Van Brunt, B. J. Baliga, and A. Q. Huang, "A New Edge Termination Technique for High-Voltage Devices in 4H-SiC–Multiple-Floating-Zone Junction Termination Extension," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 880–882, Jul. 2011, doi: 10.1109/LED.2011.2144561.

[19] P. G. Neudeck, D. J. Spry, L.-Y. Chen, G. M. Beheim, R. S. Okojie, C. W. Chang, R. D. Meredith, T. L. Ferrier, L. J. Evans, M. J. Krasowski, and N. F. Prokop, "Stable Electrical Operation of 6H–SiC JFETs and ICs for Thousands of Hours at 500 C," *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 456–459, May 2008, doi: 10.1109/LED.2008.919787.

[20] J. Liu, R. Zhang, M. Xiao, S. Pidaparthi, H. Cui, A. Edwards, L. Baubutr, C. Drowley, and Y. Zhang, "Surge Current and Avalanche Ruggedness of 1.2-kV Vertical GaN p-n Diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10959–10964, Oct. 2021, doi: 10.1109/TPEL.2021.3067019.

[21] H. H. Gong, X. H. Chen, Y. Xu, F.-F. Ren, S. L. Gu, and J. D. Ye, "A 1.86-kV double-layered NiO/β-Ga2O3 vertical p–n heterojunction diode," *Appl. Phys. Lett.*, vol. 117, no. 2, p. 022104, Jul. 2020, doi: 10.1063/5.0010052.

[22] Y. Wang, H. Gong, X. Jia, G. Han, J. Ye, Y. Liu, H. Hu, X. Ou, X. Ma, and Y. Hao, "First Demonstration of RESURF and Superjunction ß-Ga2O3 MOSFETs with p-NiO/n- Ga2O3 Junctions," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2021, p. 36.6.1-36.6.4. doi: 10.1109/IEDM19574.2021.9720500.

[23] Y. Wang, H. Gong, X. Jia, J. Ye, Y. Liu, H. Hu, X. Ou, X. Ma, R. Zhang, Y. Hao, and G. Han, "Demonstration of β-$Ga_2O_3$ Superjunction-Equivalent MOSFETs," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 2203–2209, Apr. 2022, doi: 10.1109/TED.2022.3152464.

[24] M. Xiao, Y. Ma, Z. Du, Y. Qin, K. Liu, K. Cheng, F. Udrea, A. Xie, E. Beam, B. Wang, J. Spencer, M. Tadjer, T. Anderson, H. Wang, and Y. Zhang, "First Demonstration of Vertical Superjunction Diode in GaN," in *2022 International Electron Devices Meeting (IEDM)*, Dec. 2022, p. 35.6.1-35.6.4. doi: 10.1109/IEDM45625.2022.10019405.

[25] B. Wang, M. Xiao, J. Spencer, Y. Qin, K. Sasaki, M. J. Tadjer, and Y. Zhang, "2.5 kV Vertical Ga2O3 Schottky Rectifier With Graded Junction Termination Extension," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 221–224, Feb. 2023, doi: 10.1109/LED.2022.3229222.

[26] X. Xia, M. Xian, P. Carey, C. Fares, F. Ren, M. Tadjer, S. J. Pearton, T. Q. Tu, K. Goto, and A. Kuramata, "Vertical β-Ga2O3 Schottky rectifiers with 750 V reverse breakdown voltage at 600 K," *J. Phys. Appl. Phys.*, vol. 54, no. 30, p. 305103, May 2021, doi: 10.1088/1361-6463/abfe37.

[27] K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "1-kV vertical Ga2O3 field-plated Schottky barrier diodes," *Appl. Phys. Lett.*, vol. 110, no. 10, p. 103506, Mar. 2017, doi: 10.1063/1.4977857.

[28] B. Wang, M. Xiao, X. Yan, H. Y. Wong, J. Ma, K. Sasaki, H. Wang, and Y. Zhang, "High-voltage vertical Ga2O3 power rectifiers operational at high temperatures up to 600 K," *Appl. Phys. Lett.*, vol. 115, no. 26, p. 263503, Dec. 2019, doi: 10.1063/1.5132818.

[29] Y. Wang, G. Han, W. Xu, T. You, H. Hu, Y. Liu, X. Zhang, H. Huang, X. Ou, X. Ma, and Y. Hao, "Recessed-Gate $Ga_2O_3$-on-SiC MOSFETs Demonstrating a Stable Power Figure of Merit of 100 mW/cm$^2$ Up to 200 °C," *IEEE Trans. Electron Devices*, vol. 69, no. 4, pp. 1945–1949, Apr. 2022, doi: 10.1109/TED.2022.3154340.

[30] W. Xu, Y. Wang, T. You, X. Ou, G. Han, H. Hu, S. Zhang, F. Mu, T. Suga, Y. Zhang, Y. Hao, and X. Wang, "First Demonstration of Waferscale Heterogeneous Integration of Ga2O3 MOSFETs on SiC and Si Substrates by Ion-Cutting Process," in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, p. 12.5.1-12.5.4. doi: 10.1109/IEDM19573.2019.8993501.

[31] K. Zeng, A. Vaidya, and U. Singisetti, "A field-plated Ga2O3 MOSFET with near 2-kV breakdown voltage and 520 mΩ · cm2 on-resistance," *Appl. Phys. Express*, vol. 12, no. 8, p. 081003, Jul. 2019, doi: 10.7567/1882-0786/ab2e86.

[32] W. Hao, Q. He, X. Zhou, X. Zhao, G. Xu, and S. Long, "2.6 kV NiO/Ga2O3 Heterojunction Diode with Superior High-Temperature Voltage Blocking Capability," in *2022 IEEE 34th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, May 2022, pp. 105–108. doi: 10.1109/ISPSD49238.2022.9813680.