

# 1 kV GaN-on-Si Quasi-Vertical Schottky Rectifier

Yuan Qin, Ming Xiao, Ruizhe Zhang, *Student Member, IEEE*, Qingyun Xie, *Student Member, IEEE*, Tomás Palacios, *Fellow IEEE*, Boyan Wang, *Student Member, IEEE*, Yunwei Ma, Ivan Kravchenko, Dayrl P Briggs, Dale K Hensley, Bernadeta R Srijanto, and Yuhao Zhang, *Senior Member, IEEE*

**Abstract**—This work demonstrates quasi-vertical GaN Schottky barrier diodes (SBDs) on 6-inch Si substrate with a breakdown voltage (BV) over 1 kV, the highest BV reported in vertical GaN-on-Si SBDs to date. The deep mesa inherently in quasi-vertical devices is leveraged to form a self-aligned edge termination, and the mesa sidewall is covered by the p-type nickel oxide (NiO) as a reduced surface field (RESURF) structure. This novel termination enables a parallel-plate junction electric field of 2.8 MV/cm, being close to the material limit for GaN. The device also shows a high on/off ratio of  $10^{10}$ , low turn-on voltage of 0.5 V, and low specific on-resistance of  $1.1 \text{ m}\Omega\cdot\text{cm}^2$ . Moreover, the device exhibits excellent overvoltage robustness under the continuous 800 V stress in the unclamped inductive switching test. These results show the good promise of the low-cost vertical GaN-on-Si power diodes.<sup>1</sup>

**Index Terms**—power electronics, wide bandgap, gallium nitride, vertical device, nickel oxide, breakdown voltage, reliability

## I. INTRODUCTION

Gallium nitride (GaN) has become a mainstream power semiconductor owing to its superior physical properties over silicon (Si) and silicon carbide (SiC) [1]. Lateral GaN devices have been commercialized from 15 V to 900 V [2] and demonstrated up to 10 kV [3], [4]. Vertical devices promise superior power capacity [5] and robustness [6] as compared to lateral devices. Vertical GaN devices are being commercialized globally [7], [8], but the GaN wafer on native substrate is still more costly as compared to SiC and Si wafers.

Vertical GaN-on-Si devices have gained increased attention with the promise to achieve the 10-fold lower material cost and larger-diameter processing [9]. Since the first demonstration in 2014 [10], GaN-on-Si quasi-vertical diodes [11]–[18], fully-vertical diodes [19]–[22], and MOSFETs [23], [24] have been demonstrated. Upscaling the breakdown voltage (BV) is critical to make this device technology competitive for 200–600 V class applications. Recently, the highest BV of GaN-on-Si p-n diodes reached 1.2 kV [18], but BV of Schottky barrier diodes (SBDs) and MOSFETs is still below 600 V [16], [24]. Due to the high turn-on voltage ( $V_{\text{ON}} > 3 \text{ V}$ ), GaN p-n diode is uncompetitive for direct use in power electronics applications.

As the GaN epitaxy thickness is limited below  $\sim 6 \mu\text{m}$  on Si substrate [9], edge termination design is critical for realizing high BV, and it is particularly challenging for SBDs due to the high surface electric field (E-field). The implanted guard rings were usually used in prior GaN-on-Si SBDs [15], [16], [25].

In this work, we leverage the deep mesa structure inherently in quasi-vertical devices for edge termination. Deep mesa was

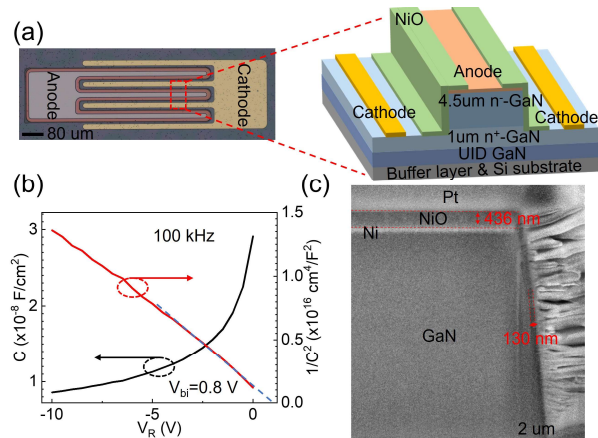


Fig. 1. (a) Top-view optical microscopy image of the fabricated device, and the 3D cross-section schematic of a device unit-cell. (b) C-V and  $1/C^2$ -V characteristics of the Ref. SBD. (c) FIB-SEM images of the RESURF SBD.

first deployed in Si devices as an effective termination; it can ideally eliminate the cylindrical/spherical junction curvatures if the electrode edge has a minimal gap with the mesa sidewall [26]. However, the effectiveness of practical mesa terminations is susceptible to the sidewall interface charges [27] and may require very careful passivation optimization [28]. In GaN, the dry etch is likely to produce N vacancies, which introduce high density of donor traps [29] and parasitic leakage [25].

To address this issue, besides optimizing the etch process, we cover the GaN sidewall with the p-type nickel oxide (NiO) to form a reduced-surface-field (RESURF) structure. The NiO has a bandgap of 3.4–4 eV [30], and the NiO/GaN heterojunction has been demonstrated on non-planar surfaces (e.g., deep trench [31]) to withstand high E-field [31]. Our RESURF quasi-vertical GaN-on-Si SBDs demonstrate a BV over 1 kV and a Baliga's figure of merit (FOM) near  $1 \text{ GW}/\text{cm}^2$ , as well as an excellent overvoltage robustness in inductive-load circuits.

## II. DEVICE FABRICATION

Fig. 1(a) shows the top-view microscopic image and the cross-section schematic of the fabricated RESURF SBD. The wafer consists of a  $4.5\text{-}\mu\text{m}$ -thick  $n^+$ -GaN drift layer, a  $1\text{-}\mu\text{m}$ -thick  $n^+$ -GaN (Si:  $\sim 5 \times 10^{18} \text{ cm}^{-3}$ ) current spreading layer, a  $0.5\text{-}\mu\text{m}$ -thick GaN layer, and a buffer layer, all grown on 6-inch Si substrate by Enkris Semiconductor Inc. A reference SBD (Ref. SBD) without NiO is used to extract the net donor concentration ( $N_D$ ) in  $n^+$ -GaN. As shown in Fig. 1(b),  $N_D$  is extracted to be  $1.4 \times 10^{16} \text{ cm}^{-3}$  from the C-V characteristics.

<sup>1</sup>Y. Qin, M. Xiao, R. Zhang, Y. Ma, B. Wang, and Y. Zhang are with the Center of Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA.

Q. Xie and T. Palacios are with the Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

I. Kravchenko, D. P. Briggs, D. K. Hensley, and B. R. Srijanto are with the Center for Nanophase Materials Sciences, Oak Ridge National Laboratory, Oak Ridge, Tennessee 37830, USA.

This work is in part supported by National Science Foundation under Grants ECCS-2230412 and ECCS-2045001 and by CPES Industry Consortium.

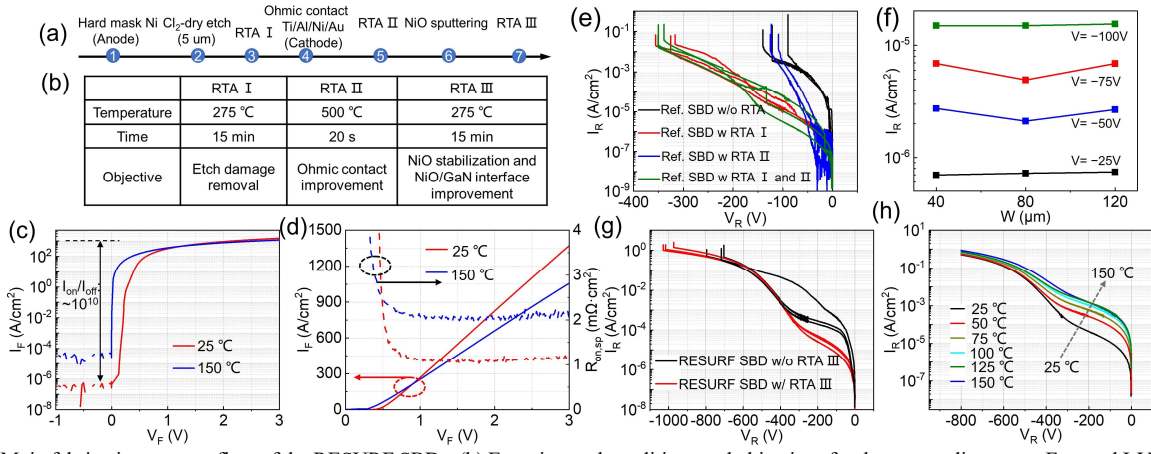


Fig. 2. (a) Main fabrication process flow of the RESURF SBDs. (b) Experimental conditions and objectives for three annealing steps. Forward I-V characteristics of the RESURF SBDs plotted in the (c) semi-log and (d) linear scale at 25 and 150 °C. (e) Reverse I-V curves of the Ref. SBDs without RTA, with RTA I, RTA II, and both RTA I and RTA II. (f) Leakage current density of the Ref. SBD after RTA I with different mesa finger widths ( $W = 40, 80, \text{ and } 120 \mu\text{m}$ ) and identical finger length at different reverse biases. Reverse I-V characteristics of (g) RESURF SBDs with and without the RTA III process and (h) the RESURF SBDs at different temperatures. The reverse characteristics of all the devices were measured in Fluorinert FC-70.

The fabrication starts with the deposition of a thick Ni layer (250 nm), which serves as the Schottky contact and the hard mask for dry etch. Cl<sub>2</sub>-based dry etch is then used to form the 5 μm-deep mesa. This self-aligned etch process enables minimal gap between the anode edge and the mesa sidewall. After dry etch, a rapid thermal annealing (RTA) in N<sub>2</sub> is performed at 275 °C for 15 min to heal the N vacancies [32]. Then the cathode Ohmic contact is formed on n<sup>+</sup>-GaN using the Ti/Al/Ni/Au stack with a 500 °C annealing. The p-type NiO is deposited by the RF magnetron sputtering at room temperature using NiO target in pure Ar atmosphere (60 sccm), followed by a final RTA at 275 °C in N<sub>2</sub> to stabilize the acceptor concentration ( $N_A$ ) [31], [33]. The  $N_A$  in NiO is extracted to be  $2\sim 3 \times 10^{17} \text{ cm}^{-3}$  from C-V measurement of a test structure in our prior work [33].

Fig. 1(c) shows the focused ion beam scanning electron microscope (FIB-SEM) images of the fabricated device. The thickness of NiO is 436 nm on the mesa top/bottom surface and ~130 nm at the sidewall, suggesting a lower sputter rate at the sidewall. The NiO extension lengths on the Schottky contact and the mesa bottom surface are 18 and 5 μm, respectively. In the multi-finger layout, the width of each mesa finger is 40 μm.

### III. DEVICE CHARACTERISTICS

Fig. 2(a) shows the main fabrication process of the RESURF SBD. There are three annealing steps in the fabrication process, and the corresponding annealing conditions as well as the objectives are presented in Fig. 2(b). Figs. 2(c) and (d) show the forward characteristics of the quasi-vertical RESURF SBD at 25 °C and 150 °C. The current is normalized to the area of anode. A high on/off ratio of  $10^{10}$  is extracted at +2/-1 V at 25 °C. The turn-on voltage ( $V_{ON}$ ) is 0.5 V, similar to the built-in voltage ( $V_{bi}$ ) extracted from the C-V measurement (Fig. 1(b)). The ideal factor is extracted to be 1.03, indicating the good Schottky behavior. The differential  $R_{on,sp}$  is  $1.1 \text{ m}\Omega \cdot \text{cm}^2$  ( $\sim 1.65 \text{ m}\Omega \cdot \text{cm}^2$  normalized to total active area in the multi-finger device). At 150 °C, the on/off ratio remains above  $10^8$ , the  $V_{ON}$  is reduced to 0.3 V, and the differential  $R_{on,sp}$  increases by 2 times.

Fig. 2(e) shows the blocking characteristics of the Ref. SBDs without/with the RTA I and II process. The RTA I effectively

reduces the leakage current along the sidewall, probably due to the reduction of the etch-produced N vacancies [32]. As shown in Fig. 2(f), the leakage current density after RTA I exhibits almost no dependence on the finger width ( $W$ ). This suggests the sidewall leakage is insignificant in total leakage current; otherwise, the leakage current will be perimeter proportional, and the leakage current density will be  $W$  dependent. Fig. 2(g) shows the reverse I-V characteristics of the RESURF SBDs with and without the RTA III process. The RTA III reduces the leakage current and increases  $BV$ , which can be attributed to the GaN/NiO interface improvement. The NiO RESURF structure enables the strongest improvement, allowing  $BV$  increase from ~350 V in the Ref. SBDs to >1000 V in the RESURF SBDs.

The breakdown is destructive, occurring at the anode edge or in the NiO layer, suggesting it is E-field limited. The leakage current density at  $BV$  is about  $1 \text{ A/cm}^2$ , similar to that reported in GaN-on-Si p-n diodes [18]. Based on the punch-through model,  $BV = E_{peak}t - qN_D t^2/2\epsilon$  ( $t$  is the n<sup>-</sup>-GaN thickness

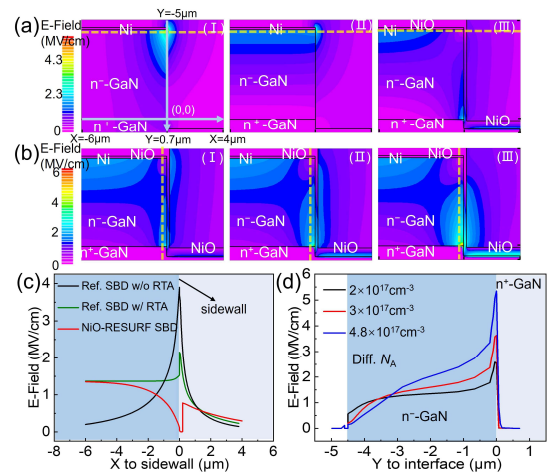


Fig. 3. Simulated E-field contours near the sidewall region of the (a) Ref. SBDs (I) with and (II) without the N vacancy, as well as (III) the RESURF SBD, all at  $V_R = -300 \text{ V}$ . (b) Simulated E-field contours near the sidewall region of the RESURF SBDs with  $N_A$  of (I)  $2 \times 10^{17} \text{ cm}^{-3}$ , (II)  $3 \times 10^{17} \text{ cm}^{-3}$ , and (III)  $4.8 \times 10^{17} \text{ cm}^{-3}$ , all at  $V_R = -500 \text{ V}$ . The origin of X- and Y-axis are defined at the GaN sidewall and n<sup>-</sup>/n<sup>+</sup>-GaN interface, respectively, which are illustrated in (a)-(I). (c) E-field profiles along the lateral cutlines shown in (a). (d) E-field profiles along the vertical cutlines shown in (b).

and  $\epsilon$  the GaN relative permittivity (10.4 for the c-axis)), the parallel-plane junction field ( $E_{\text{peak}}$ ) at  $BV$  is  $\sim 2.8$  MV/cm. This shows the effectiveness of our edge termination.

Temperature-dependent reverse I-V characteristics of the RESURF SBD are shown in Fig. 2(h). The leakage current's temperature dependence is significant below 400 V and shrinks at higher bias. This can be explained by a transition in leakage current mechanism in the depletion region, from the variable-range-hopping towards the trap-assisted space-charge-limited current (SCLC) [10]. The I-V data at high bias can be fitted by a power law relation, further supporting the SCLC [22]. At very low reverse voltage, the leakage current is dominated by thermionic-emission (TFE) transport mechanism. The leakage current at 800 V shows good thermal stability and is below 1 A/cm<sup>2</sup> at 150 °C. The device shows no parametric shifts after repetitive I-V sweeps up to 800 V at 150 °C.

TCAD simulation was performed to understand the impacts of the RTA process and NiO structure on device  $BV$ . NiO material properties are based on [34]. Fig. 3(a) shows the simulated E-field contours in SBDs with and without the donor traps at the sidewall (typical trap density  $4 \times 10^{12}$  cm<sup>-2</sup> [29]) as well as with NiO covering the sidewall. Fig. 3(b) shows the simulated E-field contours in SBDs with  $N_A$  of 2, 3,  $4.8 \times 10^{17}$  cm<sup>-3</sup> in NiO at the sidewall. The extracted surface E-field profiles along the lateral cutline at the depth of 50 nm below Schottky junction for Fig. 3(a) are shown in Fig. 3(c). Here the inclusion/exclusion of donor traps correspond to the fabrication without/with RTA I. The simulation shows that, at high reverse bias, donor traps are ionized, leading to serious E-field crowding at the mesa edge. This explains the improved  $BV$  after the RTA. In contrast, p-NiO depletes the interface states and the n-GaN near the sidewall, eliminating the surface E-field crowding and moving the peak E-field into bulk GaN, whilst reducing the peak E-field magnitude.

Simulations in Fig. 3(b) also reveal the impact of the charge density ( $\sigma_A$ ) in NiO on the device  $BV$ . Fig. 3(d) shows the extracted sidewall E-field profiles along the vertical cutline 50 nm away from the GaN sidewall in Fig. 3(b). A higher  $N_A$  (and  $\sigma_A$ ) can continuously reduce the peak E-field at the top surface, but result in an increased E-field near the mesa foot, as the NiO there may not be fully depleted. At  $N_A$  of  $3 \times 10^{17}$  cm<sup>-3</sup> ( $\sigma_A$  of  $4 \times 10^{12}$  cm<sup>-2</sup>), the peak E-field near the mesa foot approaches the critical E-field of GaN, making it an upper limit.

Unclamped inductive switching (UIS) test is widely used to evaluate the overvoltage and surge-energy robustness of power devices [35]. An on-wafer UIS test setup is developed in this work (Fig. 4(a)). The UIS circuit board is directly connected to the probes in contact with the bare-die device. In the UIS test, the inductive energy produces a capacitive voltage overshoot in the device. Fig. 4(b) shows the waveforms of the RESURF SBD voltage and the main loop current under a UIS pulse with a peak device voltage of 800 V. The device was then stressed under the continuous 800 V UIS tests for thousands of pulses at the 2 kHz frequency (Fig. 4(c)) and exhibited no degradation after the stress (Fig. 4(d)). This result suggests the potential of rating the RESURF SBD as a 600/650 V device, as devices with such a rating are usually used in converters with 400 V bus voltage with overvoltage robustness evaluated up to 800 V.

Fig. 5 benchmarks the trade-off between differential  $R_{\text{ON,SP}}$  and  $BV$  for vertical GaN-on-Si p-n diodes, SBDs and FETs. Our

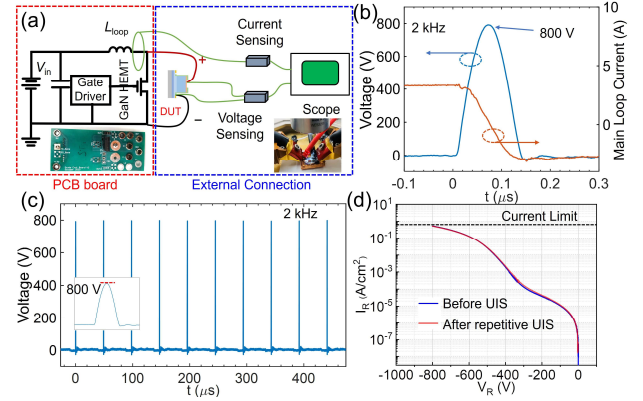


Fig. 4. (a) Schematic of the on-wafer UIS test setup. Inset shows photos of the UIS board and the probes on device. The loop inductance ( $L_{\text{loop}}$ ) is 5  $\mu$ H, and the commercial GaN HEMT is 650 V rated with  $BV > 1$  kV. (b) The UIS waveforms of the SBD voltage and the main loop current. (c) Repetitive UIS waveforms with the 800 V peak voltage. (d) Reverse I-V characteristics of the RESURF SBD before and after the repetitive UIS test.

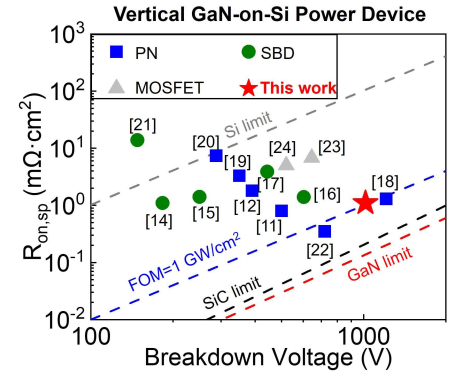


Fig. 5. Benchmark of the (differential)  $R_{\text{ON,SP}}$  versus  $BV$  of vertical GaN-on-Si SBDs, PN diodes, and MOSFETs. The Si, SiC and GaN limits of 1-D power devices, as well as the 1 GW/cm<sup>2</sup> FOM limit, are also shown.

RESURF SBD demonstrates a record Baliga's FOM near 1 GW/cm<sup>2</sup> in vertical GaN-on-Si SBDs. At the same time, the  $V_{\text{ON}}$  of our SBD (0.5 V) is much lower than that of p-n diodes ( $> 3$  V), enabling a forward voltage ( $V_F$ ) of 1.1 V extracted at 300 A/cm<sup>2</sup> that is much lower than  $V_F$  of p-n diodes (4.5 V [18]). This suggests a much lower conduction loss and a superior switching FOM ( $V_F \cdot Q$  [1]). Finally, 800 V UIS robustness is reported for the first time in vertical GaN-on-Si devices.

#### IV. SUMMARY

This work demonstrates quasi-vertical GaN-on-Si SBDs with a novel edge termination comprising the self-aligned deep mesa and the NiO RESURF structure. This termination enables a  $BV$  over 1 kV, the highest  $BV$  in vertical GaN-on-Si SBDs. The device is stable at 150 °C and shows a good overvoltage robustness in 800 V repetitive UIS tests. The device's Baliga's FOM approaches 1 GW/cm<sup>2</sup>. These results show the great potential of the low-cost vertical GaN-on-Si devices for power electronics applications.

#### ACKNOWLEDGEMENT

Device manufacturing and SEM inspection was conducted as part of a user project at the Center for Nanophase Materials Sciences (CNMS), which is a US Department of Energy, Office of Science User Facility at Oak Ridge National Laboratory. The VT authors thank discussions with Prof. Hongyu Yu's group at SUSTech and the GaN-on-Si wafer provided by them.

## REFERENCES

- [1] Y. Zhang, F. Udrea, and H. Wang, "Multidimensional device architectures for efficient power electronics," *Nat. Electron.*, vol. 5, no. 11, Art. no. 11, Nov. 2022, doi: 10.1038/s41928-022-00860-5.
- [2] K. J. Chen, O. Häberlen, A. Lidow, C. Lin Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017, doi: 10.1109/TED.2017.2657579.
- [3] M. Xiao, Y. Ma, K. Liu, K. Cheng, and Y. Zhang, "10 kV, 39 mΩ·cm<sup>2</sup> Multi-Channel AlGaN/GaN Schottky Barrier Diodes," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 808–811, Jun. 2021, doi: 10.1109/LED.2021.3076802.
- [4] M. Xiao, Y. Ma, Z. Du, V. Pathirana, K. Cheng, A. Xie, E. Beam, Y. Cao, F. Udrea, H. Wang, and Y. Zhang, "Multi-Channel Monolithic-Cascode HEMT (MC<sup>2</sup>-HEMT): A New GaN Power Switch up to 10 kV," in *2021 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2021, p. 5.5.1-5.5.4. doi: 10.1109/IEDM19574.2021.9720714.
- [5] Y. Zhang and T. Palacios, "(Ultra)Wide-Bandgap Vertical Power FinFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 3960–3971, Oct. 2020, doi: 10.1109/TED.2020.3002880.
- [6] J. Liu, R. Zhang, M. Xiao, S. Pidaparathi, H. Cui, A. Edwards, L. Baubut, C. Drowley, and Y. Zhang, "Surge Current and Avalanche Ruggedness of 1.2-kV Vertical GaN p-n Diodes," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 10959–10964, Oct. 2021, doi: 10.1109/TPEL.2021.3067019.
- [7] T. Oka, "Recent development of vertical GaN power devices," *Jpn. J. Appl. Phys.*, vol. 58, no. SB, p. SB0805, Apr. 2019, doi: 10.7567/1347-4065/ab02e7.
- [8] J. Liu, M. Xiao, R. Zhang, S. Pidaparathi, H. Cui, A. Edwards, M. Craven, L. Baubut, C. Drowley, and Y. Zhang, "1.2-kV Vertical GaN Fin-JFETs: High-Temperature Characteristics and Avalanche Capability," *IEEE Trans. Electron Devices*, vol. 68, no. 4, pp. 2025–2032, Apr. 2021, doi: 10.1109/TED.2021.3059192.
- [9] Y. Zhang, A. Dadgar, and T. Palacios, "Gallium nitride vertical power devices on foreign substrates: a review and outlook," *J. Phys. Appl. Phys.*, vol. 51, no. 27, p. 273001, 2018, doi: 10.1088/1361-6463/aac8aa.
- [10] Y. Zhang, M. Sun, D. Piedra, M. Azize, X. Zhang, T. Fujishima, and T. Palacios, "GaN-on-Si Vertical Schottky and p-n Diodes," *IEEE Electron Device Lett.*, vol. 35, no. 6, pp. 618–620, Jun. 2014, doi: 10.1109/LED.2014.2314637.
- [11] Y. Zhang, D. Piedra, M. Sun, J. Hennig, A. Dadgar, L. Yu, and T. Palacios, "High-Performance 500 V Quasi- and Fully-Vertical GaN-on-Si pn Diodes," *IEEE Electron Device Lett.*, vol. 38, no. 2, pp. 248–251, Feb. 2017, doi: 10.1109/LED.2016.2646669.
- [12] X. Zhang, X. Zou, X. Lu, C. W. Tang, and K. M. Lau, "Fully- and Quasi-Vertical GaN-on-Si p-i-n Diodes: High Performance and Comprehensive Comparison," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 809–815, Mar. 2017, doi: 10.1109/TED.2017.2647990.
- [13] R. Abdul Khadar, C. Liu, L. Zhang, P. Xiang, K. Cheng, and E. Matioli, "820-V GaN-on-Si Quasi-Vertical p-i-n Diodes With BFOM of 2.0 GW/cm<sup>2</sup>," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 401–404, Mar. 2018, doi: 10.1109/LED.2018.2793669.
- [14] Y. Li, M. Wang, R. Yin, J. Zhang, M. Tao, B. Xie, Y. Hao, X. Yang, C. P. Wen, and B. Shen, "Quasi-Vertical GaN Schottky Barrier Diode on Silicon Substrate With 10<sup>10</sup> High On/Off Current Ratio and Low Specific On-Resistance," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 329–332, Mar. 2020, doi: 10.1109/LED.2020.2968392.
- [15] X. Guo, Y. Zhong, J. He, Y. Zhou, S. Su, X. Chen, J. Liu, H. Gao, X. Sun, Q. Zhou, Q. Sun, and H. Yang, "High-Voltage and High-I<sub>ON</sub>/I<sub>OFF</sub> Quasi-Vertical GaN-on-Si Schottky Barrier Diode With Argon-Implanted Termination," *IEEE Electron Device Lett.*, vol. 42, no. 4, pp. 473–476, Apr. 2021, doi: 10.1109/LED.2021.3058380.
- [16] X. Guo, Y. Zhong, Y. Zhou, S. Su, X. Chen, S. Yan, J. Liu, X. Sun, Q. Sun, and H. Yang, "Nitrogen-Implanted Guard Rings for 600-V Quasi-Vertical GaN-on-Si Schottky Barrier Diodes With a BFOM of 0.26 GW/cm<sup>2</sup>," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5682–5686, Nov. 2021, doi: 10.1109/TED.2021.3108951.
- [17] R. M. A. Khadar, A. Floriduz, T. Wang, and E. MATIOLI, "p-NiO junction termination extensions for GaN power devices," *Appl. Phys. Express*, Jun. 2021, doi: 10.35848/1882-0786/ac09ff.
- [18] X. Guo, Y. Zhong, Y. Zhou, X. Chen, S. Yan, J. Liu, X. Sun, Q. Sun, and H. Yang, "1200-V GaN-on-Si Quasi-Vertical p-n Diodes," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2057–2060, Dec. 2022, doi: 10.1109/LED.2022.3219103.
- [19] X. Zou, X. Zhang, X. Lu, C. W. Tang, and K. M. Lau, "Fully Vertical GaN p-i-n Diodes Using GaN-on-Si Epilayers," *IEEE Electron Device Lett.*, vol. 37, no. 5, pp. 636–639, May 2016, doi: 10.1109/LED.2016.2548488.
- [20] S. Mase, Y. Urayama, T. Hamada, J. J. Freedman, and T. Egawa, "Novel fully vertical GaN p-n diode on Si substrate grown by metalorganic chemical vapor deposition," *Appl. Phys. Express*, vol. 9, no. 11, p. 111005, Nov. 2016, doi: 10.7567/APEX.9.111005.
- [21] K. Zhang, S. Mase, K. Nakamura, T. Hamada, and T. Egawa, "Demonstration of fully vertical GaN-on-Si Schottky diode," *Electron. Lett.*, vol. 53, no. 24, pp. 1610–1611, Oct. 2017, doi: 10.1049/el.2017.3166.
- [22] Y. Zhang, M. Yuan, N. Chowdhury, K. Cheng, and T. Palacios, "720-V/0.35-mΩ·cm<sup>2</sup> Fully Vertical GaN-on-Si Power Diodes by Selective Removal of Si Substrates and Buffer Layers," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 715–718, May 2018, doi: 10.1109/LED.2018.2819642.
- [23] C. Liu, R. A. Khadar, and E. Matioli, "GaN-on-Si Quasi-Vertical Power MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 71–74, Jan. 2018, doi: 10.1109/LED.2017.2779445.
- [24] R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, "Fully Vertical GaN-on-Si power MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 443–446, Mar. 2019, doi: 10.1109/LED.2019.2894177.
- [25] Y. Zhang, M. Sun, H. Wong, Y. Lin, P. Srivastava, C. Hatem, M. Azize, D. Piedra, L. Yu, T. Sumitomo, N. A. de Braga, R. V. Mickevicius, and T. Palacios, "Origin and Control of OFF-State Leakage Current in GaN-on-Si Vertical Diodes," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2155–2161, Jul. 2015, doi: 10.1109/TED.2015.2426711.
- [26] C. Park, N. Hong, D. J. Kim, and K. Lee, "A new junction termination technique using ICP RIE for ideal breakdown voltages," in *Proceedings of the 14th International Symposium on Power Semiconductor Devices and Ics*, Jun. 2002, pp. 257–260. doi: 10.1109/ISPSD.2002.1016220.
- [27] T. T. H. Nguyen, M. Lazar, J. L. Augé, H. Morel, L. V. Phung, and D. Planson, "Vertical Termination Filled with Adequate Dielectric for SiC Devices in HVDC Applications," *Mater. Sci. Forum*, vol. 858, pp. 982–985, 2016, doi: 10.4028/www.scientific.net/MSF.858.982.
- [28] H. Fukushima, S. Usami, M. Ogura, Y. Ando, A. Tanaka, M. Deki, M. Kushimoto, S. Nitta, Y. Honda, and H. Amano, "Vertical GaN p-n diode with deeply etched mesa and the capability of avalanche breakdown," *Appl. Phys. Express*, vol. 12, no. 2, p. 026502, Feb. 2019, doi: 10.7567/1882-0786/aafdb9.
- [29] H. Kim, "Reactive ion etching damage in n-GaN and its recovery by post-etch treatment," *Electron. Lett.*, vol. 44, no. 17, pp. 1037–1039, Aug. 2008, doi: 10.1049/el:20081771.
- [30] J. A. Spencer, A. L. Mock, A. G. Jacobs, M. Schubert, Y. Zhang, and M. J. Tadjer, "A review of band structure and material properties of transparent conducting and semiconducting oxides: Ga<sub>2</sub>O<sub>3</sub>, Al<sub>2</sub>O<sub>3</sub>, In<sub>2</sub>O<sub>3</sub>, ZnO, SnO<sub>2</sub>, CdO, NiO, CuO, and Sc<sub>2</sub>O<sub>3</sub>," *Appl. Phys. Rev.*, vol. 9, no. 1, p. 011315, Mar. 2022, doi: 10.1063/5.0078037.
- [31] M. Xiao, Y. Ma, Z. Du, Y. Qin, K. Liu, K. Cheng, F. Udrea, A. Xie, E. Beam, B. Wang, J. Spencer, M. Tadjer, T. Anderson, H. Wang, and Y. Zhang, "First Demonstration of Vertical Superjunction Diode in GaN," in *2022 International Electron Devices Meeting (IEDM)*, Dec. 2022, p. 35.6.1-35.6.4. doi: 10.1109/IEDM45625.2022.10019405.
- [32] Q. Zhou, M. O. Manasreh, M. Pophristic, S. Guo, and I. T. Ferguson, "Observation of nitrogen vacancy in proton-irradiated AlxGa1-xN," *Appl. Phys. Lett.*, vol. 79, no. 18, pp. 2901–2903, Oct. 2001, doi: 10.1063/1.1415422.
- [33] B. Wang, M. Xiao, J. Spencer, Y. Qin, K. Sasaki, M. J. Tadjer, and Y. Zhang, "2.5 kV Vertical Ga<sub>2</sub>O<sub>3</sub> Schottky Rectifier With Graded Junction Termination Extension," *IEEE Electron Device Lett.*, vol. 44, no. 2, pp. 221–224, Feb. 2023, doi: 10.1109/LED.2022.3229222.
- [34] H. Zhou, S. Zeng, J. Zhang, Z. Liu, Q. Feng, S. Xu, J. Zhang, and Y. Hao, "Comprehensive Study and Optimization of Implementing p-NiO in β-Ga<sub>2</sub>O<sub>3</sub> Based Diodes via TCAD Simulation," *Crystals*, vol. 11, no. 10, p. 1186, Sep. 2021, doi: 10.3390/cryst11101186.
- [35] R. Zhang, J. P. Kozak, M. Xiao, J. Liu, and Y. Zhang, "Surge-Energy and Overvoltage Ruggedness of P-Gate GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13409–13419, Dec. 2020, doi: 10.1109/TPEL.2020.2993982.