NiO Junction Termination Extension for Ga_2O_3 Devices: High Blocking Field, Low Capacitance, and Fast Switching Speed

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***Abstract*—This work investigates the blocking electric field, capacitance, and switching speed of the p-type NiO based junction termination extension (JTE) for vertical Ga_2O_3 devices. The JTE comprises multiple NiO layers sputtered on the surface of Ga_2O_3 drift region, the acceptor concentration and length of which are carefully optimized. This NiO JTE enabled a breakdown voltage over 3 kV in vertical Ga_2O_3 diodes with a parallel-plate junction field of 4.2 MV/cm. Large-area Ga_2O_3 p-n diodes with a current over 1 A were fabricated to evaluate the JTE's capacitance and switching characteristics. The JTE accounts for only ~11% of the junction capacitance of this 1 A diode, and the percentage is expected to be even smaller for higher-current diodes. The turn-ON/OFF speed and reverse recovery time of the diode are comparable to commercial SiC Schottky barrier diodes. These results show the good promise of NiO JTE as an effective edge termination for Ga_2O_3 power devices.**

Keywords—ultra-wide bandgap, gallium oxide, nickel oxide, junction termination extension, reverse recovery, switching tests

I. Introduction

The advances in power semiconductor devices rely on the combined innovations in semiconductor materials and device architectures [1]. Gallium oxide (Ga_2O_3) is a promising ultra-wide bandgap (UWBG) material for power devices due to its high critical electric field, controllable doping, and availability of large-diameter wafers [2], [3]. Up to now, Ga_2O_3 is the only UWBG material that has met several key milestones for power semiconductor development, including the 6-inch wafer, high-current (>100 A) device, packaging, electrothermal ruggedness, and converter applications [4], [5].

A critical challenge for Ga_2O_3 power devices is the lack of p-type doping in Ga_2O_3, which, in particular, makes the edge termination design very difficult. Prior Ga_2O_3 edge terminations mainly rely on the field plate [6], implantation [7], and trench structures [8]. Recently, an alternative WBG p-type material, nickel oxide (NiO), is found to be able to form high-quality hetero-PN junction with Ga_2O_3 [9], [10] and GaN [11], [12].

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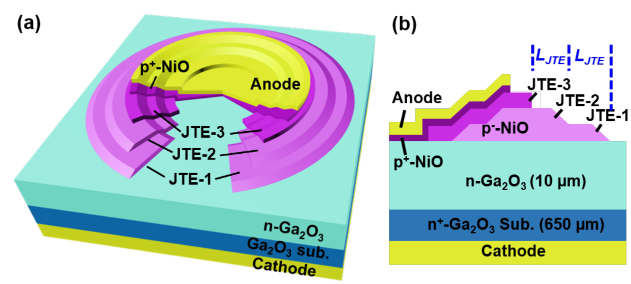

Fig. 1. (a) 3-D schematic of the Ga_2O_3 PND with NiO JTE (part of the anode, p^+-NiO and JTEs are removed to show the internal device structure). (b) Schematic of the JTE region.

NiO has also been used to form a single-zone junction termination extension (JTE) for Ga_2O_3 devices [13]. However, the effectiveness of the single-zone JTE is known to be sensitive to the charge density.

Recently, we proposed a multi-layer NiO JTE, in which the lengths of NiO layers decrease from the bottom towards the top to enable a graded decrease in charge density away from the device active area [14], [15]. This NiO JTE has broad design window, large process latitude, and high effectiveness. It has been applied to vertical Ga_2O_3 Schottky barrier diodes (SBDs) [14] and p-n diodes [15] to achieve the multi-kilovolt breakdown voltage (*BV*).

This work extends our prior works into evaluating the blocking electric field (E-field), capacitance, and switching characteristics of the graded NiO JTE technology. Low parasitic capacitance and high switching speed are critical requirement for any edge terminations of power devices. However, such studies have not been reported in Ga_2O_3 devices. This work fills this gap by fabricating large-area NiO/Ga_2O_3 p-n diodes with the graded NiO JTE to evaluate the JTE's characteristics. A double-pulse test (DPT) setup for on-wafer devices is developed for testing the switching characteristics of the JTE p-n diode (PND).

II. JTE Design and Fabrication

The NiO JTE comprises two layers of p^--NiO (JTE-1 and -2) and one layer of p-NiO (JTE-3) sputtered on the surface of

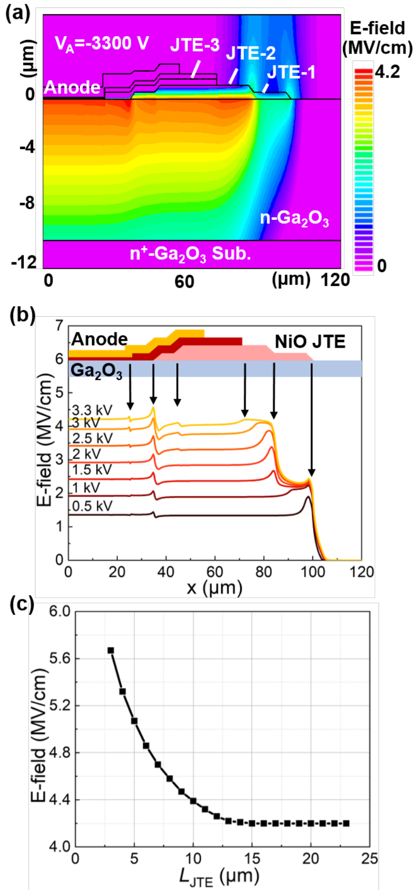

Fig. 2. (a) Simulated E-field contour in the PND at a reverse bias of 3.3 kV. (b) The E-field profile in Ga_2O_3 at the PND blocking voltage increased from 0.5 to 3.3 kV. (c) The simulated junction field at 3.3 kV as a function of L_{JTE}.

the Ga_2O_3 drift region (Fig. 1). An p$^+$-NiO is sputtered below the anode to enable low p-layer resistance in the PND active region. The thickness and acceptor concentration (N_A) of p$^-$-NiO, p-NiO and p$^+$-NiO layers are 400 nm and ~3×10^{17} cm^{-3}, 350 nm and ~10^{18} cm^{-3}, and 250 nm and >10^{19} cm^{-3}, respectively. The N_A of NiO is controlled by modulating the Ar/O_2 gas ratio in the sputtering process, as elaborated in our prior work [12]. The two p$^-$-NiO layers are designed to be fully depleted at the device BV. Hence, their total thickness (t_{NiO}) can be roughly determined according to $t_{NiO}N_A \approx E_M\varepsilon_{GaO}$, where E_M is the junction field in Ga_2O_3 at BV and ε_{GaO} is the Ga_2O_3's permittivity [14].

The detailed simulations on the JTE's design space, trade-off, and design window are illustrated in [15]. Fig. 2(a)-(b) show the simulated E-field contour in the p-n diode at the increased reverse bias up to 3.3 kV. The E-field crowding is effectively suppressed. Fig. 2(c) show the peak E-field as a function of the incremental JTE length (L_{JTE}), revealing a saturation effect in the peak E-field decrease as L_{JTE} increases.

The wafer used in this work is the 2-inch Ga_2O_3 wafer with a drift region thickness of 10 μm and a net donor concentration of 1.3×10^{16} cm^{-3}. Fig. 3(a) shows the main device fabrication steps. The fabrication starts with the cathode Ohmic contact formation, followed by the sputtering and lift-off of two p$^-$-NiO

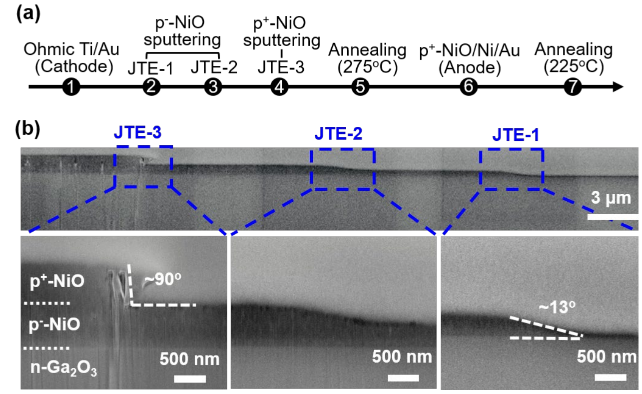

Fig. 3. (a) Main fabrication steps of the Ga_2O_3 JTE-PND. (b) Cross-sectional SEM images of the entire and each JTE region of the fabricated NiO/Ga_2O_3 PND.

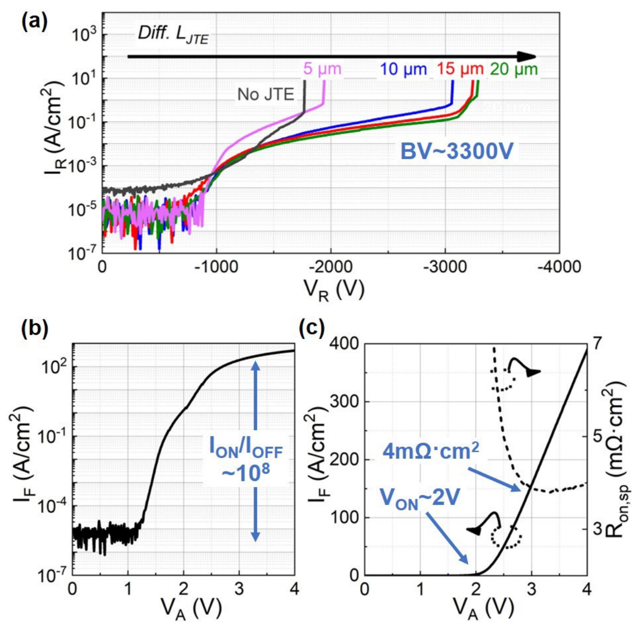

Fig. 4. (a) Reverse I-V characteristics of the PNDs without the JTE and the JTE-PNDs with different L_{JTE} of 5, 10, 15, and 20 μm. Forward I-V characteristics in (b) semi-log and (c) linear scales.

JTE layers and a p$^+$-NiO JTE layer. After a post-sputter annealing, the p$^+$-NiO anode layer and Ni/Au Ohmic contact are deposited, followed by a final annealing. Fig. 3(b) shows the cross-sectional SEM image of the fabricated JTE region.

III. Static and Switching Characteristics

Fig. 4 shows the characteristics of the fabricated p-n diodes with JTE (JTE-PNDs), revealing a BV up to 3.3 kV and a differential specific on-resistance ($R_{ON,SP}$) of 4 mΩ·cm^2. Fig. 5 (a)-(b) show the characteristics of the large-area JTE-PNDs with a forward current >1 A. Fig. 5(c) shows the C-V characteristics of the large-area JTE-PNDs. The capacitance associated with the JTE region is calculated by subtracting the active-area junction capacitance from the measured capacitance. Note that this calculation can overestimate the JTE-related capacitance, as it also accounts for the diffusion capacitance and other parasitics.

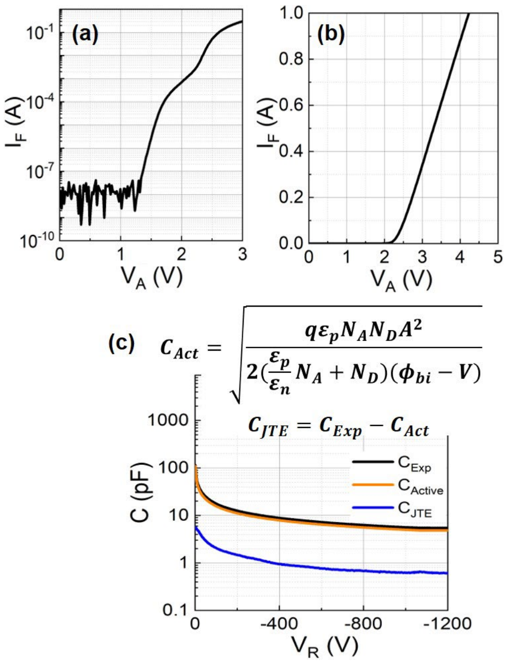

Fig. 5. Forward I-V characteristics of large-area JTE-PNDs in (a) semi-log and (b) linear scales. (c) C-V characteristics and the model to separate the active-region capacitance (C_{Act}) and JTE region capacitance (C_{JTE}) in the total experimental capacitance (C_{Exp}). N_D and N_A are the net donor/acceptor concentration in Ga_2O_3 and NiO. ε_n and ε_p is the permittivity of Ga_2O_3 and NiO, respectively. Φ_{bi} is the built-in potential of the NiO/Ga_2O_3 hetero-junction.

Under this overestimation scenario, JTE capacitance accounts for only ~11% of the device capacitance. This percentage is expected to continuously decrease in devices with larger current ratings, as the main area capacitance scales with the device area while the JTE capacitance scales with the device perimeter.

The switching characteristics of the JTE-PNDs are measured by a custom DPT setup for on-wafer device characterizations. As shown in Fig. 6(a)-(c), the setup connects a DPT board with the probe. This switching test setup obviates the need for device packaging at the price of higher circuit parasitics (from the probe-board connection) than the full board-level circuit test.

Fig. 6(d)-(e) shows the 3A/800V turn-OFF/ON waveforms of the Ga_2O_3 JTE-PNDs and a commercial SiC SBD (IDH02G120C5). The Ga_2O_3 JTE-PNDs show a reverse recovery time of 43 ns and the rise/fall time of ~12/14 ns, both being similar to the SiC SBD tested under the same setup. This suggests the NiO JTE does not limit the switching speed of Ga_2O_3 devices.

IV. Benchmark and Summary

Fig. 7 benchmarks the *BV vs.* differential-$R_{ON,SP}$ of our JTE-PND with other Ga_2O_3 diodes. Thanks to the effectiveness of the JTE, the performance of our JTE-PND is comparable to the state-of-the-art Ga_2O_3 diodes. Table I compares our graded NiO JTE with the representative reports of other termination technologies for Ga_2O_3 devices, including the combinations of implantation and field plate (FP) [7], trench and FP [8], as well as high-*k* dielectric FP [16]. Our graded NiO JTE features the concurrent realization of high parallel-plate junction E-field of 4.2 MV/cm, low parasitic capacitance, and fast switching speed.

In summary, this work presents comprehensive studies of the static and switching characteristics of a new NiO-based JTE for vertical Ga_2O_3 devices. Large-area Ga_2O_3 p-n diodes with the JTE were fabricated. In addition to the static I-V and C-V characteristics, an on-wafer DPT set-up was developed to measure the switching waveforms of the JTE-PND. Under the same measurement set-up, the Ga_2O_3 JTE-PND shows similar switching speed compared to the commercial SiC SBDs. These

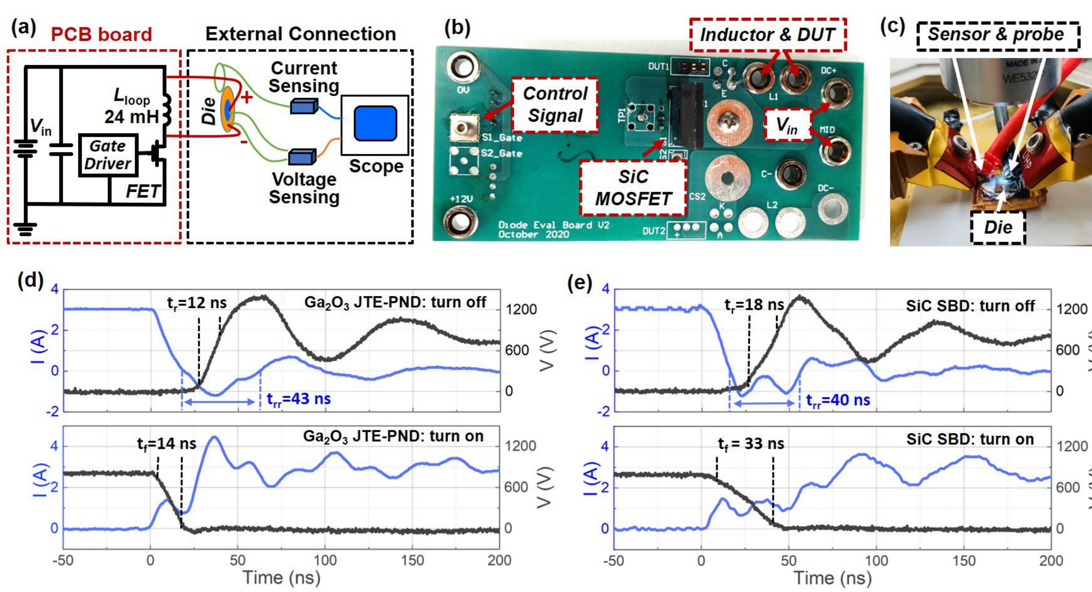

Fig. 6. (a) Schematic of the custom DPT setup for on-wafer Ga_2O_3 diodes, in which a circuit board is connected to the probes. Photos of the (b) test board and (c) the two high-current probes for on-wafer device test. The 800V/3A turn-off and turn-on waveforms of (a) Ga_2O_3 JTE-PNDs and (b) commercial SiC SBDs. The reverse recovery time (t_{rr}) of both diodes are similar. The rise time (t_r) and fall time (t_f) of SiC SBDs are higher due to the higher current rating (larger charges) than the Ga_2O_3 JTE-PNDs.

Table I. Comparison of the edge termination technologies for Ga_2O_3 diodes.

Edge termination	Diode	Ref	Junction field (MV/cm)	JTE Capacitance	Switching metrics	Diff. $R_{ON,SP}$ ($m\Omega\cdot cm^2$)	BV (V)
Multi-layer NiO JTE	PND	This work	4.2	Low (11% of a ~1A device)	small rise/fall /reverse-recovery time	4	3300
N implant + FP	SBD	[7]	2.45	-	-	4.7	1430
Trench + FP	SBD	[8]	4	-	-	8.8	2890
High-*k* FP	SBD	[16]	5.45	-	-	0.32	687

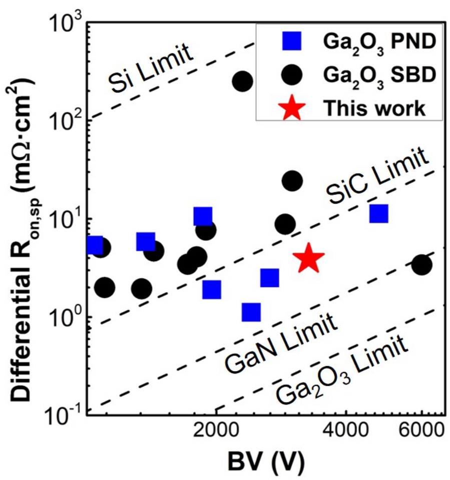

Fig. 7. $R_{ON,SP}$ vs. BV benchmark of the fabricated Ga_2O_3 JTE-PND with other Ga_2O_3 power diodes.

results provide useful references for advancing the Ga_2O_3 devices towards power electronics applications.

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