NiO junction termination extension for high-voltage (>3 kV) Ga_2O_3 devices

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Edge termination is the enabling building block of power devices to exploit the high breakdown field of wide bandgap (WBG) and ultra-wide bandgap (UWBG) semiconductors. This work presents a heterogeneous junction termination extension (JTE) based on p-type nickel oxide (NiO) for gallium oxide (Ga_2O_3) devices. Distinct from prior JTEs usually made by implantation or etch, this NiO JTE is deposited on the surface of Ga_2O_3 by magnetron sputtering. The JTE consists of multiple NiO layers with various lengths to allow for a graded decrease in effective charge density away from the device active region. Moreover, this surface JTE has broad design window and process latitude, and its efficiency is drift-layer agnostic. The physics of this NiO JTE is validated by experimental applications into NiO/Ga_2O_3 p-n diodes fabricated on two Ga_2O_3 wafers with different doping concentrations. The JTE enables a breakdown voltage over 3.2 kV and a consistent parallel-plate junction field of 4.2 MV/cm in both devices, rendering a power figure of merit of 2.5~2.7 GW/cm^2. These results show the great promise of the deposited JTE as a flexible, near ideal edge termination for WBG and UWBG devices, particularly those lacking high-quality homojunctions.

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Power electronics are advancing rapidly driven by deployment of wide bandgap (WBG) and ultra-wide bandgap (UWBG) semiconductors and the associated device innovations.[1] Gallium oxide (Ga_2O_3) has recently emerged as a promising UWBG power semiconductor, due to its high critical breakdown electric field (E_C), controllable doping, and the availability of large diameter wafers.[2,3] In addition to the demonstration of high breakdown voltage (BV) over 8 kV[4] and high current over 100 A,[5] Ga_2O_3 devices have also been packaged[6,7] and switched in power converters.[8,9]

For power devices, edge termination holds the key for exploiting the high E_C of WBG/UWBG materials.[10] The junction termination extension (JTE) is a successful edge termination widely used in industrial WBG devices.[11,12] The JTE is based on p-n junctions, where the oppositely doped region compensates the charge of the drift region and thereby weakens the surface electric field (E-field). Despite the JTE's success in Si and WBG devices, the development of Ga_2O_3 JTE is hindered by the lack of p-type doping.[13] Existing edge terminations in Ga_2O_3 devices rely on field plates,[14–16] implanted traps,[4,17,18] deep mesa,[19] and trench structures.[20] Whereas, the studies in WBG devices have revealed that JTE can enable the superior efficiency[21] (i.e., the device BV over the ideal BV) and robustness[22] as compared to the non-junction-based termination such as field plate.

Nickel oxide (NiO) is an alternative p-type WBG material (bandgap 3.4~4 eV[13]). Recently, NiO has been applied to form heterogenous p-n junction in GaN[23–26] and Ga_2O_3 devices. Since the first report,[27] NiO/Ga_2O_3 p-n diodes have achieved multi-kilovolt BV with a low differential specific on-resistance ($R_{ON,SP}$).[4,8,28–31] Most of these diodes have a natural NiO termination with relatively high doping concentration. The efficiency of such highly-doped, single-layer termination is very sensitive to the NiO doping and thickness.[32–34] Improved JTE designs demonstrated in WBG devices include the multizone JTE,[32–34] graded JTE,[11] and etched JTE,[35] the common feature of which is a graduate decrease in charge density away from the active region.

In this work, we present a NiO-based JTE comprising multiple NiO layers deposited on the surface of the Ga_2O_3 drift region. The NiO JTE is lightly doped and has graded decrease in sheet charge density, both enabling broad design window and process latitude. In addition, this deposited JTE differs from the prior JTEs that are formed by implantation, diffusion, or etching. The surface deposition process has minimal damage to Ga_2O_3 as compared to the dry etching and obviates the high-temperature activation usually required for implantation. Moreover, the efficiency of this deposited NiO JTE is independent of the doping and thickness of the Ga_2O_3 drift region.

In this letter, the JTE's physics is first presented by simulations. Subsequently, NiO/Ga_2O_3 p-n diodes are used as the demonstrative vehicle for the JTE's experimental demonstration and evaluation. To show the JTE's wide applicability, Ga_2O_3 diodes are fabricated on two wafers with different donor concentration (N_D) in the drift region, and their BV and junction blocking field are compared. Note that the reason of choosing p-n diode over Schottky barrier diode (SBD) to experimentally evaluate the JTE's capability is to avoid the leakage-induced premature breakdown widely reported in Ga_2O_3 SBDs.[36-38]

As shown in Fig. 1(a) and (b), the proposed NiO JTE comprises lightly-doped p$^-$-NiO and highly-doped p-NiO layers. The p$^-$-NiO layers are fully depleted at the device *BV* to compensate the depletion charge in Ga_2O_3, thereby spreading out the crowded E-field at the device edge and reducing the surface E-field. To produce a graded charge profile, the lengths of p$^-$-NiO layers decrease from the bottom to the top with an identical incremental length (L_{JTE}) for each layer. The sidewall angle of each p$^-$-NiO layer is preferable to be small to avoid abrupt changes in charge density. This charge transition can be also smoothened by increasing the number of p$^-$-NiO layers. For simplicity, a bi-layer p$^-$-NiO region (i.e., JTE-1 and -2) with small sidewall angles is studied in this work, which could achieve near ideal performance with optimal designs. While p$^-$-NiO layers fulfill the main JTE functionality, the p-NiO layer interfaces the p$^-$-NiO JTE with the anode layer (i.e., p$^+$-NiO in the p-n diode). At *BV*, this p-NiO cover is only partially depleted, thereby confining the high E-field within itself. Meanwhile, this partially-depleted p-NiO layer can still reduce the E-field at the top surface of p$^-$-NiO similar to some counterparts in p-GaN,[10,39] thereby serving as a weak JTE (i.e., JTE-3). As an illustration of the practical JTE, Fig. 1(c) shows the cross-sectional scanning electron microscopy (SEM) images of the fabricated NiO JTE (the fabrication details will be elaborated later).

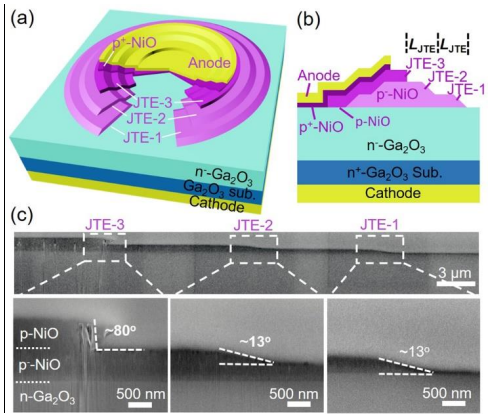

FIG. 1. (a) 3-D and (b) cross-sectional schematics of the NiO/Ga_2O_3 p-n diode with the proposed NiO JTE. (c) Cross-sectional SEM images of the entire JTE region fabricated in this work and the edge of each JTE layer.

Three parameters are critical to the JTE functionality, the acceptor concentration (N_A) and thickness (t_{JTE}) of each p$^-$-NiO layer, as well as the L_{JTE}. Considering a simplified 1-D model in the vertical direction: according to Gauss's law, the optimal sheet charge density in p$^-$-NiO can be derived from the full p$^-$-NiO depletion at the device *BV*[11]

$$qnN_A^{opt}t_{JTE}^{opt} = E_M\varepsilon_N \qquad (1)$$

where n is the number of p$^-$-NiO JTE layers, N_A^{opt} and t_{JTE}^{opt} are the optimal N_A and t_{JTE}, E_M is the surface E-field in Ga_2O_3 at the device *BV* ($E_M \le E_C$), and ε_N is the Ga_2O_3 permittivity. To probe the E-field distribution, TCAD simulations are performed

based on the calibrated models for Ga_2O_3 devices.[6,15] Fig. 2(a) and (b) show the simulated E-field contour and the Ga_2O_3 surface E-field profile in a JTE design satisfying (1). Here n=2, N_A^{opt}=3×10^{17} cm^{-3}, t_{JTE}^{opt}=430 nm, E_M ≈4.2 MV/cm at 3.3 kV, and the Ga_2O_3 drift layer thickness (t_{GaO}) and donor concentration (N_D) are 10 μm and 1.3×10^{16} cm^{-3}, respectively. As shown in Fig. 2(b), the p$^-$-NiO JTE-1 and JTE-2 are successively depleted at ~1 and ~3 kV, respectively. After each depletion, the peak E-field at the outer edge of the respective JTE (i.e., E1 and E2) is suppressed and barely increases further with the bias. At 3.3 kV, the E_M along the Ga_2O_3 surface is nearly constant, and the peak E-field is slightly higher (~4.35 MV/cm) located at E5. From Fig. 2(a), it is verified that the p-NiO JTE-3 is partially depleted with an E-field dropped to zero within itself.

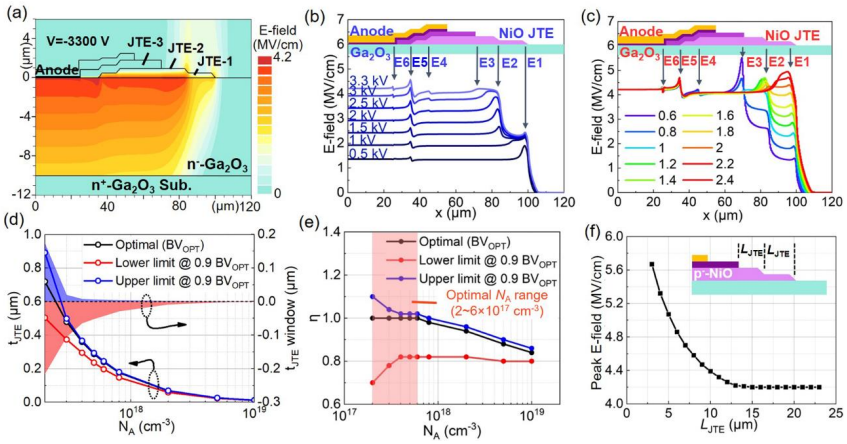

FIG. 2. (a) Simulated E-field contour in a Ga_2O_3 p-n diode with an optimal NiO JTE design biased at -3.3 kV. (b) Surface E-field profile in Ga_2O_3 at the reverse biases increased from 0.5 to 3.3 kV. (c) Surface E-field profile in Ga_2O_3 at -3.3 kV for various N_A ranging from $0.6N_A^{opt}$ to $2.4N_A^{opt}$ while keeping $t_{JTE} = t_{JTE}^{opt}$ in the p$^-$-NiO layers. (d) The t_{JTE} for the highest BV (BV_{OPT}), as well as the upper and lower limits of t_{JTE} and the associated t_{JTE} window for 90% of the BV_{OPT}, for several N_A ranging from 10^{17} to 10^{19} cm^{-3}. (e) The η of three t_{JTE} leading to BV_{OPT} and 90%BV_{OPT} as a function of N_A. (f) Peak E-field as a function of L_{JTE} based on the design in (a)-(b).

Next, we explore the design window of N_A and t_{JTE}, which determines the JTE's process latitude. Here we define a ratio between the JTE's sheet charge density and its 1-D optimal value given by (1), i.e., $\eta = N_A t_{JTE}/(N_A^{opt} t_{JTE}^{opt})$. Fig. 2(c) shows the Ga_2O_3 surface E-field profile at 3.3 kV for various N_A ranging from $0.6N_A^{opt}$ to $2.4N_A^{opt}$ while keeping $t_{JTE} = t_{JTE}^{opt}$. The peak E-fields at the JTE's outer edges (E1~E3) are found to be sensitive to η, while those at the inner edges (E4~E6) changes minimally. When η < 1, the peak E-field grows below the JTE-3's outer edge (E3); when η > 1, the E-field between E1 and E2 ramps up, and the peak E-field location migrates to the JTE-1's outer edge. Subsequently, simulations are performed to traverse a large design space of N_A and t_{JTE}. The t_{JTE}'s lower and upper limits to reach 90% of the optimal (highest) BV (BV_{OPT}) are identified for several N_A in the range of 10^{17}~10^{19} cm^{-3}. Here the BV is extracted when the peak E_M at E1~E3 reaches a pre-

selected compliance of 4.2 MV/cm. While in theory this compliance selection can be arbitrary up to E_C, here the 4.2 MV/cm is based on experimental devices (to be illustrated later). As shown in Fig. 2(d), the t_{JTE} window for a 10% BV_{OPT} tolerance quickly drops as N_A increases, from 390 nm at 2×10^{17} cm^{-3} to 29 nm at 10^{18} cm^{-3} and 0.9 nm at 10^{19} cm^{-3}. This suggests the low N_A is key to enabling a broad process latitude for t_{JTE} in experimental devices.

Simulations are also used to examine if the 1-D design by (1) indeed leads to the highest efficiency in the 2-D JTE structure. As shown in Fig. 2(e), $\eta = 1$ and t_{JTE}^{opt} leads to BV_{OPT} when $N_A \leqslant 6\times10^{17}$ cm^{-3}; however, at higher N_A, the t_{JTE} for BV_{OPT} is smaller than t_{JTE}^{opt}, reaching ~$0.97t_{JTE}^{opt}$ at 10^{18} cm^{-3} and $0.84t_{JTE}^{opt}$ at 10^{19} cm^{-3}. This is because, the 1-D model in (1) represents the optimal design for the bi-layer p$^-$-NiO region and not necessarily for the JTE-1's outer extension. At higher N_A, the sharper peak E-field could emerge in the JTE-1 and JTE-2's outer edge region (i.e., E1 and E2), which has to be suppressed by a smaller t_{JTE}. This $t_{JTE} < t_{JTE}^{opt}$ design actually compromises the JTE efficiency due to a smaller E_M in the bi-layer p$^-$-NiO region according to (1). This trade-off further illustrates the importance of using low N_A to fulfill the full JTE capability. Fig. 2(e) also shows the η window for the 90% BV_{OPT}, revealing a generally narrower window for the excessive t_{JTE} than the insufficient t_{JTE}.

Finally, the impact of L_{JTE} is shown in Fig. 2(f). the peak E-field first reduces as L_{JTE} increases and then nearly saturates. An L_{JTE} range of 10~15 µm can achieve a good trade-off between the JTE's efficiency and real estate. Note that, in the above design and optimization (e.g., eqn. (1)), the t_{GaO} and N_D of the Ga_2O_3 drift region are not involved. Simulations confirms the independence of the JTE's efficiency on the Ga_2O_3 drift region assuming that the identical E_M is realized at the junction.

To verify the JTE's physics, experimental p-n diodes are fabricated on two 2-inch Ga_2O_3 wafers with an identical t_{GaO} of 10 µm and different N_D of 1.3×10^{16} cm^{-3} (wafer A) and 8×10^{15} cm^{-3} (wafer B) grown by Novel Crystal Technology. The diameter of the anode main p-n junction (p$^+$-NiO/Ga_2O_3 area) is 100 µm. These N_D are extracted by C-V measurements of the SBDs fabricated on two wafers. Fig. 3(a) shows the main process flow for NiO/Ga_2O_3 p-n diodes. After the formation of backside cathode, two p$^-$-NiO layers are deposited to the desirable t_{JTE} by the RF magnetron sputtering at room temperature using the NiO target. After forming JTE-1 and JTE-2, p-NiO layer is sputtered to form JTE-3, followed by a post-sputter annealing at 275 ºC in N_2 to stabilize the N_A in NiO and improve the NiO/Ga_2O_3 interface quality. The anode layer p$^+$-NiO and anode contact are then formed, followed by a final annealing. Note that a bilayer resist[35] is used for NiO lift-off, and the undercut length of the bottom resist can be used to tune the NiO sidewall angle formed in the sputtering process (the longer the undercut, the more pronounced lateral deposition, and the smaller the sidewall angle). As shown in Fig. 1(c), a sidewall angle of ~13º and ~80º is formed for the JTE-1/2 and JTE-3, respectively.

The hole concentration in NiO is known to positively correlate to the oxygen partial pressure in sputtering,[40] and our recent works show such correlation also holds for N_A.[26] Hence, the p$^-$-NiO is sputtered in the pure Ar atmosphere (60 sccm), while p-

NiO and p^+-NiO are sputtered in the Ar/O_2 mixture with an increased O_2 partial pressure (60/3 sccm and 40/20 sccm, respectively). Other sputtering conditions, including the NiO target (99.9% purity target from Kurt J. Lesker), pressure (3 mTorr), RF power (100 W), and temperature (25 °C), are identical for various NiO layers. The N_A in p^--NiO at high E-field is key for the designs of *BV* and t_{JTE}, but its accurate characterization is difficult due to the possible field-dependent ionization. Note that N_A is expected to also differ significantly from the hole concentration. Here, instead of characterizing N_A, we employ a single-layer p^--NiO JTE (i.e., n =1) to directly determine the optimal t_{JTE} in multi-layer JTEs.

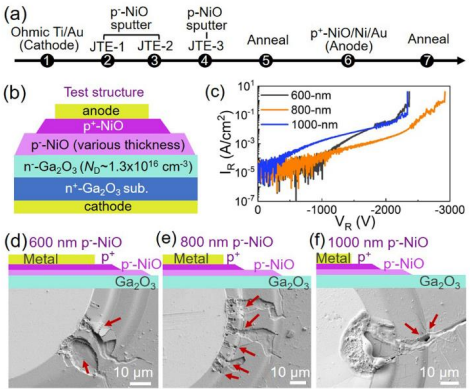

FIG. 3. (a) Main fabrication steps for the Ga_2O_3 p-n diodes with the NiO JTE. (b) Schematic of the test device structure to determine the optimal p^--NiO thickness experimentally. (c) Reverse I-V characteristics of the test devices with three p^--NiO thicknesses, and (d) the SEM images of the breakdown spots at the edge of these three test devices. The red arrows suggest the breakdown locations.

Fig. 3(b) shows a Ga_2O_3 p-n diode test structure with the blanket p^--NiO under the anode, the termination of which is equivalently a single-layer p^--NiO JTE. The *BV* of three such diodes with the p^--NiO thickness of 0.6, 0.8 and 1 μm are shown in Fig. 3(c), with the SEM images of the breakdown spots shown in Fig. 3(d). Despite the large burning trace, deep holes usually correspond to the initial percolation paths and the breakdown location. The *BV* of the diode with 0.8 μm p^--NiO is higher than the other two diodes. In addition, when the thickness increases to 1 μm, the breakdown location moves from the inner edge to the outermost edge, signifying the p^--NiO starts to become partially depleted rather than fully depleted. These results suggest the optimal thickness of a single-layer p^--NiO JTE to be ~0.8 μm. According to (1), the optimal t_{JTE} of each layer in a bi-layer p^--NiO JTE (n=2) is ~0.4 μm, which is used in experimental device fabrication. The thickness of p-NiO and p^+-NiO is not critical to the JTE functionality and is selected as 600 nm and 180 nm, respectively.

Fig. 4(a) shows the reverse I-V characteristics of the p-n diodes fabricated on the wafers A and B, revealing a *BV* of ~3.3 kV and ~3.6 kV, respectively. The *BV* is higher than the p-n diodes without any JTE [see Fig. 4(a)] and with a single-layer JTE [see Fig. 3(c)], verifying the superior efficiency of the multi-layer NiO JTE. To probe if the *BV* distinction on the wafers A and

B is due to N_D or the JTE efficiency, the ideal parallel-plate junction E-field (i.e., the average E_M) is calculated based on the punch-through E-field profile [see Fig. 4(b)]:

$$BV = E_M t_{GaO} - qN_D\, t_{GaO}^2/(2\varepsilon_N) \qquad (2)$$

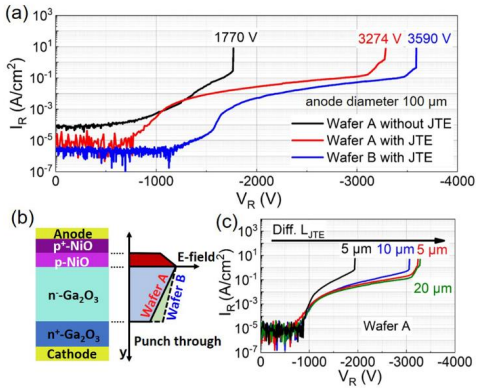

FIG. 4. (a) Reverse I-V characteristics of the Ga_2O_3 p-n diodes with the optimal JTE fabricated on the wafers A and B as well as a diode without JTE on the wafer A. (b) Illustration of the E-field profile in the diodes on two wafers. (c) Reverse I-V characteristics of the diodes with different L_{JTE} of 5, 10, 15, and 20 µm.

The average E_M calculated for diodes on two wafers is found to be both ~4.2 MV/cm. This validates the independence of the JTE efficiency on the Ga_2O_3 drift region. With this consistent E_M in Ga_2O_3, we estimate the N_A in p$^-$-NiO to be ~3×10^{17} cm^{-3} based on (1). According to simulation results in Fig. 2(d), the t_{JTE} window for the 10% *BV* tolerance is predicted to be ~125 nm at this N_A, being ~30% of its optimal value. This validates the large process latitude of the proposed JTE implemented with a low N_A. In addition, the *BV* of the fabricated diodes with different L_{JTE} are also measured. As shown in Fig. 4(c), *BV* first increases with L_{JTE} and then saturates after L_{JTE} exceeds 10 µm. This trend is consistent with the simulation results in Fig. 2(f).

Finally, the JTE has minimal impact on device $R_{ON,SP}$ and allows for the superior trade-off between *BV* and $R_{ON,SP}$. Fig. 5(a) and (b) show the forward I-V characteristics of the Ga_2O_3 p-n diodes on the wafers A and B, revealing a differential $R_{ON,SP}$ of 3.9 mΩ·cm^2 and 5.7 mΩ·cm^2, respectively. The on/off ratio of both diodes is over 10^9, and their turn-on voltage is identical. The $R_{ON,SP}$ of both diodes are dominated by the drift region, and their difference is attributable to the N_D distinction. The p$^+$-NiO anode layer contributes very little to $R_{ON,SP}$. This is confirmed by characterization of the reference SBDs with the same JTE and anode area, the $R_{ON,SP}$ of which was found to be nearly identical to p-n diodes fabricated on the same wafer. Hence, this p$^+$-NiO layer showcases a viable design to integrate the surface-deposited NiO JTE to the active device region for future diodes and transistors. Fig. 5(c) benchmarks the trade-off between *BV* and the differential $R_{ON,SP}$ of our diodes on two wafers

and other Ga_2O_3 diodes in the literature.[4,8,14,15,18,20,28,30,31,41–50] Our diodes show a power figure of merit ($BV^2/R_{ON,SP}$) of 2.5~2.7 GW/cm^2 that has surpassed the 1-D SiC limit and is comparable to the state of the art of Ga_2O_3 diodes.

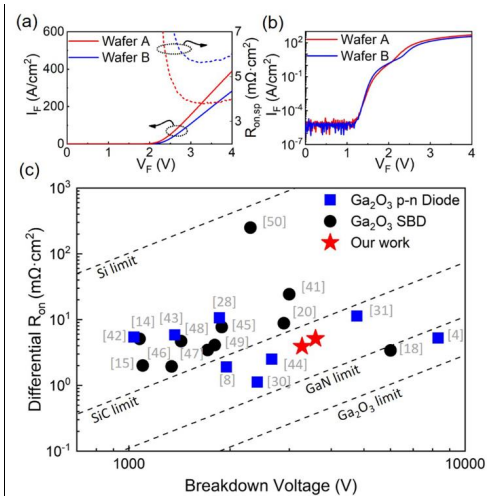

FIG. 5. Forward I-V characteristic of Ga_2O_3 diodes on the two wafers in (a) linear and (b) semi-log scale. (c) Differential $R_{ON,SP}$ versus BV trade-off of Ga_2O_3 p-n diodes and SBDs with BV > 1 kV.

In summary, this work presents the physics and experimental demonstration of a near-ideal NiO JTE for Ga_2O_3 devices. The JTE consists of multiple lowly-doped NiO layers deposited on the surface of Ga_2O_3 drift region, the geometry of which enables a graded charge decrease away from the active region. The fabrication of this surface NiO JTE is implantation- and etch-free and holds broad process latitude. The functionality of this NiO JTE is drift region agnostic. BV over 3.3 kV and a parallel-plate junction E-field of 4.2 MV/cm are demonstrated in the diodes fabricated on two Ga_2O_3 wafers. These results show the great promise of the NiO JTE as a flexible, effective building block for devices based on Ga_2O_3 and other WBG/UWBG materials lacking high-quality, selective-area homojunctions.

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Author Declarations

The authors have no conflicts to disclose.

Author Contributions

Y.Z., M.X. and B.W. conceived the device concept and planned the study. B.W. and M.X. led the device fabrication, data collection and analysis, and device simulations. Q.Y. and Y.M. contributed to device fabrication. J.S. and M.T. contributed to the data analysis. M.P. and Y.W. contributed to the simulation. K.S. grew the Ga_2O_3 wafers. Y.Z. and M.X. wrote the manuscript. All the authors discussed the results and reviewed the manuscript.

Data Availability

The data that support the findings of this study are available within the article.

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