Improved SEED Modeling of an ESD Discharge to a USB Cable

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***Abstract*—Integrated circuits (ICs) connected to a universal serial bus (USB) interface require robust electrostatic discharge (ESD) protection strategies due to the nature of the high-speed interface and the regular access by users. System-efficient ESD design (SEED) simulations can help predict the level of ESD stress seen by the IC when protected by a transient voltage suppressor (TVS). In the following paper, previously developed models were improved to predict the voltage and current seen by a TVS and an on-chip protection diode when an ESD gun was discharged to one USB cable pin. Models were improved, in part, by accurately modeling the conductivity modulation within the behavioral TVS model and by using a measured equivalent source to represent the complex interaction between the ESD gun, USB cable, and enclosure. The response of the TVS and on-chip diode was studied in simulation and measurement for several cable configurations and when adding passive components between the TVS and on-chip diode. Simulations predicted peak and quasi-static voltages and currents at the TVS and on-chip diode within 30% of those seen in measurements. The proposed modeling process can help engineers to evaluate and optimize the effectiveness of their ESD protection strategies under complicated test conditions.**

***Index Terms*—Electrostatic discharge (ESD), modeling, system-efficient ESD design (SEED), system-level ESD, transient voltage suppressor (TVS), universal serial bus (USB).**

I. Introduction

PROTECTION devices such as transient voltage suppressor (TVS) diodes are often added to a circuit to improve its immunity to electrostatic discharge (ESD). TVS devices are used to shunt most ESD current away from sensitive ICs during a transient overvoltage event. Ensuring the TVS turns ON during an ESD event, and the on-chip ESD protection does not take the entire charge can be challenging. Many on-chip ESD protection structures will turn-ON faster at lower voltages than the off-chip TVS. System efficient ESD design (SEED) is an approach for modeling the response of a system to an ESD event [1]. SEED has previously been used to predict the interaction between the TVS and diodes simulating on-chip ESD protection during a transmission-line pulse (TLP) event [2]. Models are developed in the following paper to predict the response of a TVS and on-chip diode to a particularly complicated scenario: when an ESD gun discharges to the pin of a universal serial bus (USB) cable connected to a test board that contains the IC and TVS.

The USB interface is one of the most commonly used high-speed interfaces on a wide range of electrical devices, with connectors that are easily accessible to users. Its high-speed nature and the high likelihood of seeing an ESD event make it especially susceptible to ESD. The 480 Mb/s data rate for USB 2.0 and 5 Gb/s for USB 3.0 interface carries substantial signal integrity requirements, making it even more challenging to build robust ESD protection. The high-speed requires on-chip ESD protection with low capacitance; however, the light doping required to achieve low-capacitance can cause high voltage overshoots during an ESD event [3]. Usually, external ESD protection with a low clamping voltage, a low dynamic resistance, and a low capacitance are required. A careful system-level ESD design is needed to ensure the protection is adequate, with a good understanding of the characteristics and limitations of the ESD protection devices, together with the PCB parasitics [4]. Thorough simulation in the early design stage is essential.

A number of SEED models for ESD protection structures have previously been developed. The static I-V curve of a TVS was modeled in [5]. The transient turn-ON behavior was modeled in [6] and [7] to account for the importance of the TVS turn-ON time in system-level ESD simulations. The TVS simulation framework was further improved in [8] and applied in [2] to investigate the interaction between a TVS and on-chip protection device during a TLP event. A number of models for ESD guns have also been developed, for either circuit-based or full-wave simulation, as summarized in [9]. System-level simulation of a system's response to an ESD event, however, is still challenging considering the many interactions between the ESD waveform and the protection circuits and the variations in the ESD pulse that occur due to interactions between the ESD gun and the surrounding environment—particularly when the injection occurs at the end of a cable and not to a ground plane.

Although several publications provide an analysis of ESD immunity with protection devices, less information is available

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on the impact of a cable on an ESD gun discharge event. It has been shown that a circuit simulation approach for modeling the ESD gun induced stress fails when the gun discharges to a cable that is at an electrical long distance from the reference plane [10]. The work in [11] shows the importance of modeling the USB cable, as the ESD stress differs significantly with the type and length of the USB cable. Cable discharge events with a USB cable were studied in [12], [13], and [14], though only the impact to the system was discussed without investigating the interaction between the off-chip and on-chip protection devices. Preliminary SEED models predicting the interaction between an ESD gun, USB cable, TVS, and on-chip diode were presented in [15], but these models could not accurately capture the peak and quasistatic voltages and currents seen by the on-chip ESD protection over a wide range of ESD levels.

The following paper presents improved models for predicting the ESD stress at a USB IC input/output (I/O) pin when an ESD gun is discharged to one pin of the USB cable. The models in [15] are improved, in part, by better representing the conductivity modulation using a physics-based nonlinear resistance, which solves the difficulty of accurately predicting TVS and on-chip diode response over a wide range of ESD stress. The performance of the models is also demonstrated on an actual USB cable rather than a USB cable surrogate. Although the complexity of cable configurations [15] was simplified with the circuit model in [16], it is not a general solution, requiring a very detailed understanding of the 3-D structure and the current path. In comparison, the proposed measurement-based equivalent current source (obtained when the ESD gun discharges to a 50 Ω load and the cable is placed in one of the configurations) is a simple, efficient solution and is suitable for more complex scenarios with much greater accuracy.

The TVS and on-chip diode transient models are developed in Section II and validated against TLP measurements. Section III describes the measurements characterizing the transient response of the ESD protection devices under different USB cable configurations. Simulation models of the system (the ESD gun, USB cable, test board, TVS, and on-chip diode) are presented in Section IV along with a discussion on the impact of the USB cable configuration. Discussion is presented in Sections V. Finally, Section VI concludes this article.

II. Transient Modeling of ESD Protection Devices

The diagram in Fig. 1 shows the test scenario to be investigated. A general system-level ESD protection strategy was implemented on a test board, including the off-chip (TVS) and on-chip ESD protection devices. The dual-diode structure represents the simplified ESD protection structure of the I/O on an IC.

The TVS was modeled using a behavioral model like the one in [17]. As depicted in Fig. 2, the TVS was modeled to capture its small-signal input parameters (e.g., inductance, resistance, capacitance), its IV characteristics (turn-ON voltage, snapback, on-resistance, etc.), and the transient behavior (conductivity

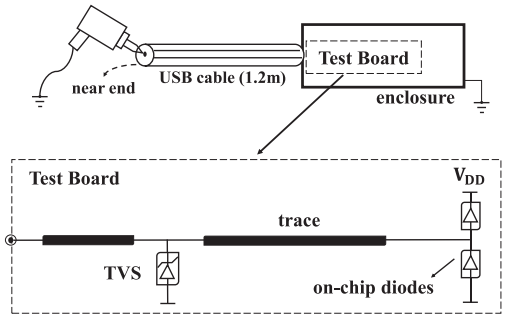

Fig. 1. Set up for characterizing the response of the TVS and on-chip diodes during an ESD discharge to a USB cable.

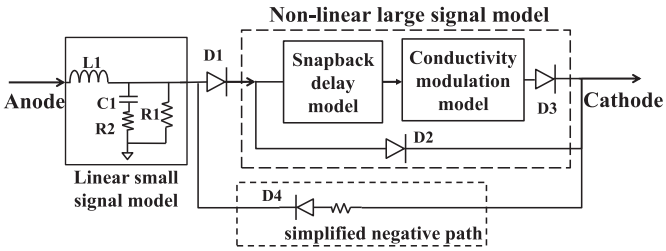

Fig. 2. TVS model framework.

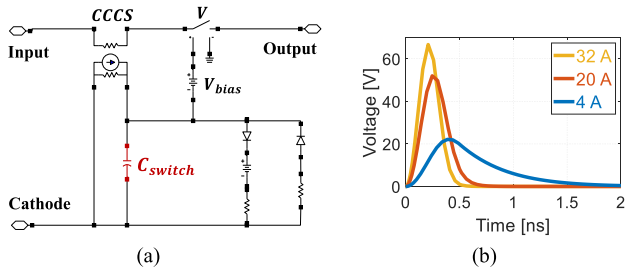

Fig. 3. Previous model of conductivity modulation. (a) Circuit model with a constant C_{switch}. (b) Voltage response at different injection levels.

modulation, turn-ON delay, etc.). The negative path was simplified using an ideal diode in series with a resistor. Characterization of the TVS was done by measuring the device response using a very fast TLP and then tuning the model to achieve a good match between the simulated and measured current and voltage waveforms in terms of their peak and steady-state values. Models were developed using a TLP injection rather than an ESD gun injection because of the lower complexity and better repeatability of the TLP.

The voltage across the TVS can be explained using the modeling framework shown in Fig. 2. In the first few nanoseconds the voltage is dominated by the voltage across the inductance "L1," the voltage across the snapback delay model, and the voltage across the conductivity modulation model. The conductivity modulation model contributes mostly to the voltage in the first nanoseconds. A circuit diagram of the conductivity modulation block is shown in Fig. 3 [8], [17]. Conductivity modulation is caused by the initially high resistance of the

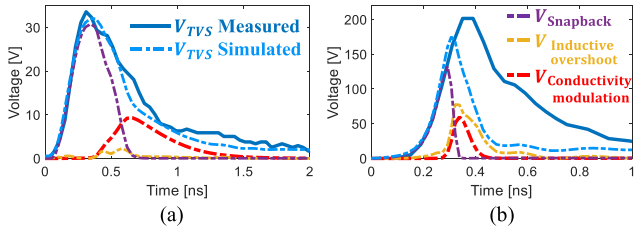

Fig. 4. Measured (blue solid line) and simulated (blue dashed line) TVS voltage with the reference TVS model when injected with an (a) 50 V and (b) 800 V TLP with 0.6 ns rise time. The voltage contributions (Fig. 2) from the snapback overshoot V_{Sanpback}, inductive overshoot $V_{\text{Inductive\_overshoot}}$, and conductivity modulation $V_{\text{Conductivity\_modulation}}$, are marked with puple, gold, and red dashed lines, respectively. (a) $V_{TLP} = 50$ V. (b) $V_{TLP} = 800$ V.

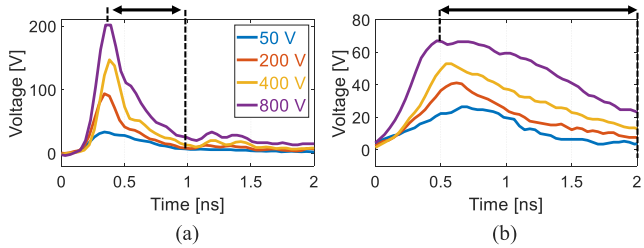

Fig. 5. Measured TVS voltage at TLP injection levels of 50, 200, 400, 800 V and with 0.6 ns and 1 ns rise times. (a) 0.6 ns rise time. (b) 1 ns rise time.

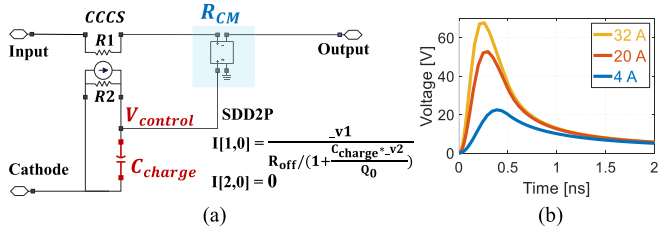

Fig. 6. Improved model of conductivity modulation using a physics-based charge dependent resistor. (a) circuit diagram. (b) Voltage response with different injeciton currents.

lightly doped regions of the TVS caused by a low minority carrier concentration at the beginning of an event. Resistance decreases, and conductivity increases as carriers are injected into the region [6], [18]. Previously, conductivity modulation was modeled with a switch and a capacitor [see Fig. 3(a)], where the switch resistance is initially set to a high value until a certain charge passes through the TVS (i.e., until a certain voltage is reached by the capacitor), at which point the switch resistance goes low. Correspondingly, the voltage response is shown in Fig. 3(b).

During the TVS modeling process, it was found that the range over which this model could accurately capture conductivity modulation was limited, leading to the poor performance after the overshoot. Two examples illustrate this observation. Fig. 4 shows results from TLP testing using a 0.6 ns rise time and 50 or 800 V pulse (when injected into a 50 Ω load). The simulation shows a good match at the low injection level (50 V), but substantially underestimates the peak and duration of the voltage waveform for the high injection level (800 V). The model fails to properly capture the conductivity modulation, which dominates the falling edge of the response after overshoot. Note that the falling edge is vital to the system-level simulation when used together with the on-chip ESD protection devices since the residual pulse [19] might be higher than the on-chip protection can withstand. For example, for the 800 V TLP injection [see Fig. 4(b)], the remaining TVS voltage in simulation is only tens of volts at 0.5 ns, suggesting that there will be minimal ESD stress at the on-chip protection device. The measured TVS voltage, however, is much higher—around 100 V—which may cause gate oxide failure of the IC. The current from 0.5–1 ns and energy through the on-chip protection device will similarly be underestimated.

The narrower voltage response (the voltage pulse across the conductivity modulation block) with increasing current injection [see Fig. 3(b)] of the conductivity modulation model leads to the underestimated TVS voltage after the overshoot. In addition, measurements suggest that the length of the conductivity modulation event should not change much with the injected current, as shown in Fig. 5. Accordingly, the conductivity modulation model was improved by better accounting for the physics behind the change in conductivity.

A. *Improved Conductivity Modulation Model—Charge Dependent Resistor*

An equation for the conductivity modulation resistance is presented in [18] and was used to model the conductivity modulation overshoot in [20]

$$R_{\text{CM}} = \frac{R_{\text{off}}}{1 + Q_C/Q_0} \tag{1}$$

where R_{CM} is the resistance of the lightly doped region, R_{off} is the resistance when the TVS is "OFF," and Q_C and Q_0 represent the total injected charge and the charge threshold needed to establish conduction, respectively.

The block representing conductivity modulation was modified to use this charge-dependent resistance, as shown in Fig. 6(a). The charge-controlled resistor R_{CM} was implemented in advanced design system as a symbolically defined resistor (1) whose value is controlled by the voltage V_{control} seen on the capacitor C_{charge}. Since C_{charge} is charged by the current flowing through the TVS, its voltage, V_{control}, is proportional to the total charge Q_C through the TVS. The voltage across this capacitor is given by

$$\begin{aligned} V_{\text{control}}(t) &= I_{\text{TVS}}(t) * \frac{1}{C_{\text{charge}}} e^{-\frac{t}{R_2 C_{\text{charge}}}} u(t) \\ &= \frac{1}{C_{\text{charge}}} \int_{-\infty}^{t} I_{\text{TVS}}(\alpha)\, e^{-\frac{t-\alpha}{R_2 C_{\text{charge}}}} d\alpha \end{aligned} \tag{2}$$

where α is a temporary variable used to integrate over time.

Assuming $I_{\text{TVS}} = 0$ for $t < 0$ and recognizing that $Q_C = C_{\text{charge}} V_{\text{control}}$

$$Q_C(t) = \int_{0}^{t} I_{\text{TVS}}(\alpha)\, e^{-\frac{t-\alpha}{R_2 C_{\text{charge}}}} d\alpha. \tag{3}$$

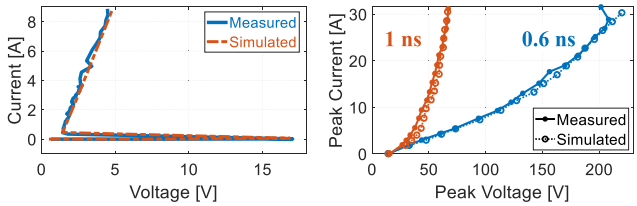

Fig. 7. TVS model performance. (a) Quasi-static *I–V* curve with 100 ns pulsewidth standard TLP injection. (b) Peak current versus peak voltage under 20 ns pulse width TLP injections with 0.6 ns and 1 ns rise times.

As R_2C_{charge} is typically set such that R_2C_{charge} is much larger than the length of the event

$$Q_C(t) \approx \int_0^t I_{\text{TVS}}(\alpha)d\alpha. \tag{4}$$

Ultimately, the resistance is modulated by the injected charge such that

$$R_{CM}(t) \approx \frac{R_{\text{off}}}{1 + \left(\int_0^t I_{\text{TVS}}(\alpha)d\alpha\right)/Q_0}. \tag{5}$$

Fig. 6(b) shows the voltage response of the improved conductivity modulation module. The response duration remains roughly constant across injection levels, which can help to improve the modeling of the falling edge after the overshoot (see Fig. 4).

B. Transient Response of the Improved TVS Model

The performance of the TVS model is summarized in Fig. 7. The quasi-static IV behavior of the model matches measurements well during snapback and after. The peak current and voltage seen by the model during its transient response are shown in Fig. 7(b) for TLP rise times of 0.6 ns and 1 ns. The simulation matches the measurement within about 5% over a wide range of injections.

Fig. 8 shows the measured and simulated transient voltage and current waveforms for the TVS under a low (50 V) injection and a high (800 V) injection, and for 0.6 and 1 ns rise times. Only the first 2 ns of the waveform is shown for a better view of the rising and falling edges following the overshoot, which is vital for system-level simulation with other ESD protection devices [19]. The underestimation of current [see Fig. 8(c)] is caused by imperfections in the model. Nevertheless, the underestimation issue of the falling edge in Fig. 4(b) has been fixed. The falling edge can now be modeled reasonably well over a wide range of injection levels.

To better demonstrate the improved modeling of the falling edge, a plot is given in Fig. 9 showing the TVS voltage 0.3 ns after the overshoot as a function of applied TLP voltage. Conductivity modulation should dominate in this region. Results are shown for rise times of 0.6 ns [see Fig. 9(a)] and 1 ns [see Fig. 9(b)]. Noticeable improvement was achieved with the physics-based conductivity modulation model. Simulations

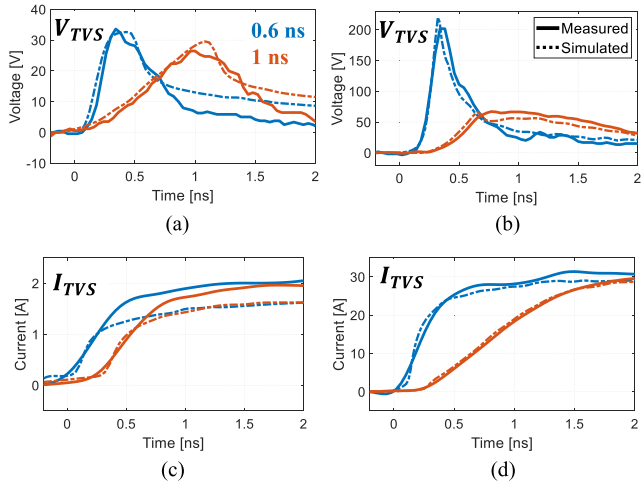

Fig. 8. Transient waveforms for the TVS under TLP injection with 0.6 ns and 1 ns rise time: (a) TVS voltage with TLP = 50 V; (b) TVS voltage with TLP = 800 V; (c) TVS current with TLP = 50 V; (d) TVS current with TLP = 800 V.

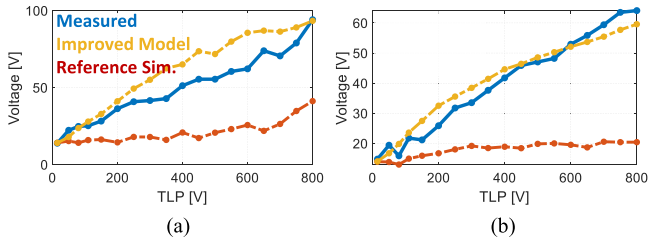

Fig. 9. TVS voltage 0.3 ns after the waveform peak, when the conductivity modulation dominates. Results are shown for TLP rise times of (a) 0.6 ns, (b) 1 ns. The reference simulation is based on [8], [17].

were also performed with 0.3 ns rise time, with similarly good results.

C. Transient Response of the On-Chip Diode Model

The transient model of the on-chip diode was built using a similar methodology as the TVS, but without the snapback module. Measured and simulated current and voltage waveforms for the on-chip diode are shown in Fig. 10, with TLP voltages of 20, 32, and 50 V, and with rise-times of 0.4, 2, and 5 ns. The on-chip diode is characterized at a low TLP level, considering the IC ESD protection structure is typical of low robustness—e.g., for a maximum 2 kV HBM event for a USB 3.1 repeater IC (the Diodes Inc. PI3EQX1002B1). The waveforms match within about 10% for each tested stimulation.

III. Experimental Setup

ESD experiments were performed using the setup shown in Fig. 1. An ESD gun was discharged to the D+ pin on one end of a 1.2 m long USB cable. The shield was connected at the other end to an enclosure. The other end of the D+ pin was either connected to a test board including the TVS and on-chip diodes characterized earlier or to a 50 Ω load. The other USB wires were left floating, as experiments showed little difference depending on their termination. The test board included probes

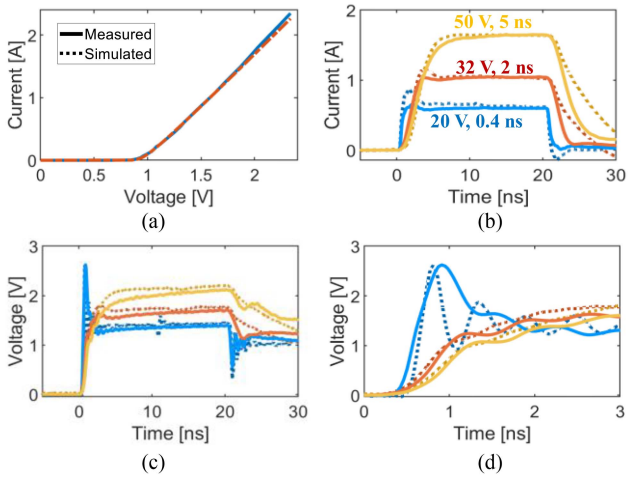

Fig. 10. Simulation performance of on-chip diode model. (a) Quasi-static *I–V* curve. (b) Transient currents durin a 20, 32, and 50 V TLP injection with 0.4, 2, and 5 ns rise time, respecitively. (c) Transient voltages. (d) Transient votage over 3 ns.

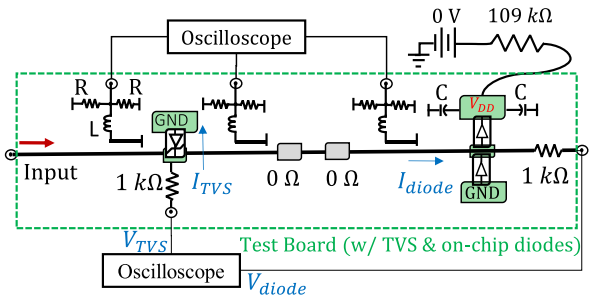

Fig. 11. Discharge to a test board connected to a 1.2 m long USB cable.

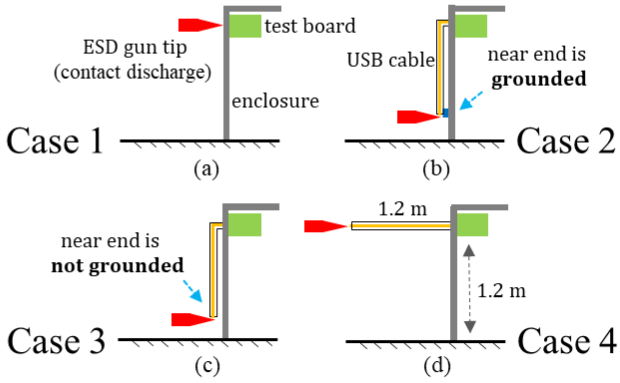

Fig. 12. USB cable configurations. (a) Case 1: No cable. (b) Case 2: Cable run along enclosure and shield connected at both ends. (c) Case 3: Cable run along enclosure and shield connected only at test board. (d) Case 4: cable run straight out from enclosure, parallel to and 1.2 m above the ground plane.

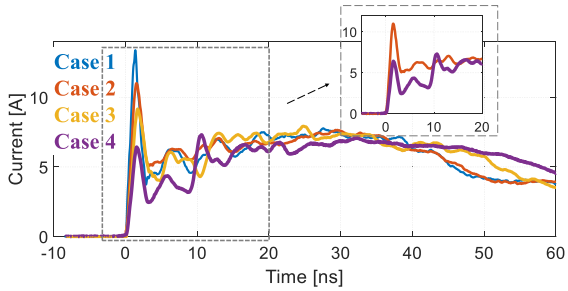

Fig. 13. Measured currents when discharging into a 50 Ω load for a 4 kV contact discharge to the D+ USB cable pin. The cases correspond to the four cable configurations shown in Fig. 12. The inset shows the current only for Cases 2 and 4 for comparison.

for measuring currents within the circuit and probe points for measuring voltages [2], [17].

The test board setup is shown in Fig. 11. The DC bias ($V_{\rm dd}$ in Fig. 1) was set to 0 V. 1 kΩ pick-up resistors were used to measure the voltage at the TVS and on-chip diodes. The voltages were measured by a Rohde & Schwarz RTO1024 oscilloscope with 2 GHz bandwidth and 10 GHz sampling rate. To determine the ESD current through the TVS and on-chip diodes, on-board current probes were placed along the trace [2]. Simultaneously, the voltages at the current probes were measured by a Tektronix DPO 70804 digital oscilloscope with 8 GHz bandwidth and 25 GHz sampling rate. The transient currents were reconstructed by calibrating each probe using the full *S*-parameter (characterized by a Keysight E5071C Vector Network Analyzer) with a frequency domain compensation technique [21].

Four cable configurations were studied, as shown in Fig. 12: a configuration with no USB cable where the ESD gun was directly discharged to the test board or load (Case 1), a configuration where the USB cable was run along the enclosure and the shield was connected to the enclosure at the discharge point (Case 2), a configuration where the USB cable was run along the enclosure and the shield was floating at the discharge point (Case 3), and a case where the USB cable was run straight out from the enclosure and parallel to the ground plane (Case 4). The USB cable shield was only connected where it met the enclosure for Case 4.

Fig. 13 shows the measured ESD current through a 50 Ω load terminating the USB cable inside the enclosure when the ESD gun was discharged to the USB cable D+ pin. The waveform for Case 4 is particularly interesting since it exhibits a "two peak" behavior that is significantly different from a typical ESD gun pulse, where the second peak is even larger than the first. These two peaks are caused by a complex interaction between the ESD gun, the cable, the cable shield, the enclosure, and the ground plane, as will be explained in Section IV.

IV. Simulation

In previous studies, the interactions between the ESD gun, cable, and enclosure were simulated using relatively complicated full-wave models, but these models could not fully capture the waveform observed by the DUT in measurements and simulation time and complexity was a concern [15]. To improve results, the interaction among these components was instead captured using a measured equivalent current source, as shown in Fig. 14.

The data defining the current source in Fig. 14(b), "ItDataset," is measured when the ESD gun discharged to a 50 Ω load and the cable is placed in one of the configurations in Fig. 12.

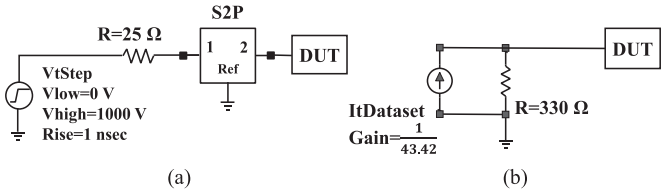

Fig. 14. Simulation approaches. (a) Use of *S*-parameters from a 3-D full-wave simulation to estimate response at, (b) use of a measured current source as the simulation input (330 Ω represents the ESD gun source impedance). The DUT is either a 50 Ω load or a model of the test board and its components (see Fig. 1).

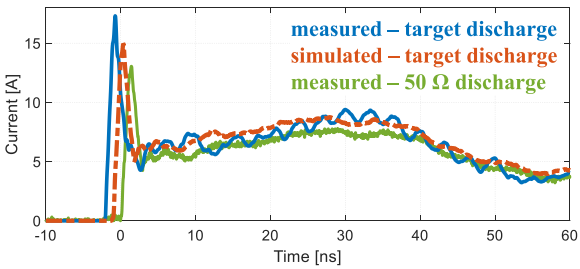

Fig. 15. Measured current during a 4 kV contact discharge to a 50 Ω load (Case 1) or the 2 Ω ESD target. The estimated current was simulated with the measured source (found using a 50 Ω load) when discharging to a 2 Ω load. The discharge time was slightly shifted for easier comparison.

The 330 Ω resistor shown in the figure represents the ESD gun's impedance. The current is extracted by dividing the measured voltage by the parallel resistive "loads," 330 Ω and 50 Ω load. A 50 Ω load was used to characterize the ESD gun discharge [22] since the USB cable impedance between the D+ pin and the cable shield is very close to 50 Ω. While the impedance looking into the ESD gun from the USB cable will not be exactly 330 Ω, and the load will not be much smaller than 50 Ω after the TVS and diode turn-ON, this current source representation is sufficient for most purposes. Changing this impedance will only impact voltage and current waveforms in the DUT after the time for energy to be reflected from the DUT to the ESD gun and back—or after about 12 ns for a 1.2 m long USB cable, which is after the most interesting portion of the discharge waveform has already occurred. Even if the TVS and diode impedance were seen instantaneously, with no cable delay, the impact would be small. Fig. 15 shows the measured current when discharging to a 2 Ω ESD target compared to an estimate of the current using the source model in Fig. 14(b) with a 2 Ω DUT load. The peak current was underestimated by about 10% but the remaining current waveform was captured well.

A. System-Level Simulation

An ESD discharge to a USB cable was simulated using current sources measured for each configuration shown in Fig. 12. The DUT was described by circuit models of the board, TVS, and on-chip diodes. Fig. 16 shows the measured and simulated TVS current waveforms for an 8 kV ESD gun discharge in Case 2 (cable shield grounded on both ends) and Case 4 (cable straight out). The simulation predicts the peak currents within 10% and captures the major features of the waveform, including the

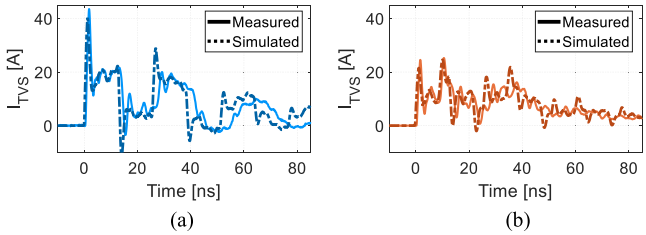

Fig. 16. Measured and simulated TVS currents in (a) Case 2—grounded both ends, and (b) Case 4—cable straight out under 8 kV contact discharge.

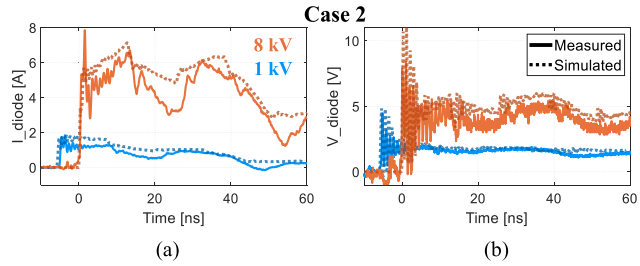

Fig. 17. Measured and simulated transient waveforms for the on-chip diode in the presence of a 1 kV and 8 kV contact discharge for the Case 2 cable configuration (both ends grounded): (a) on-chip diode current, (b) on-chip diode voltage. The start of the 1 kV event was shifted by 5 ns for easier comparison.

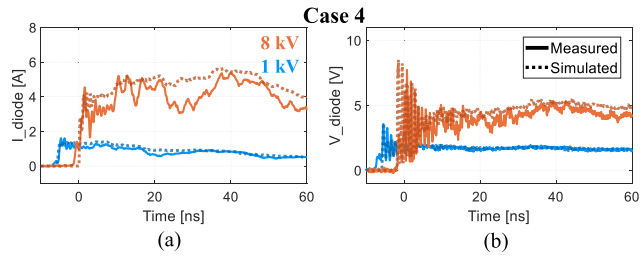

Fig. 18. Measured and simulated transient waveforms for the on-chip diode in the presence of a 1 kV and 8 kV contact discharge for the Case 4 cable configuration (cable straight out): (a) on-chip diode current, (b) on-chip diode voltage.

first prominent peak in Case 2 and the two smaller peaks in Case 4. Cases 1 and 3 are not shown for the sake of space since the model performs similarly well, and Cases 2 and 4 are the most interesting cable-discharge cases in terms of peak levels and waveshape. Considering that the current of the IEC waveform and actual human ESD has reduced substantially from its peak value when reaching 60 ns, the following results will focus on the first 60 ns to better visualize the initial events.

The currents and voltages seen by the on-chip diode are shown in Fig. 17 (Case 2, both ends grounded) and Fig. 18 (Case 4, cable straight out). The lowest ESD gun discharge level (1 kV) and the highest level (8 kV) are shown since they are the extreme conditions, which can best represent the model's performance. The simulation generally captures both the peak level and the waveshape well. The ringing observed in the diode voltage results when both the TVS and on-chip diode are turned "ON," essentially creating a transmission line shorted at both ends, which is also captured by the model.

The measurement and simulation results for Cases 2 and 4 are summarized in Fig. 19 as a function of the ESD event

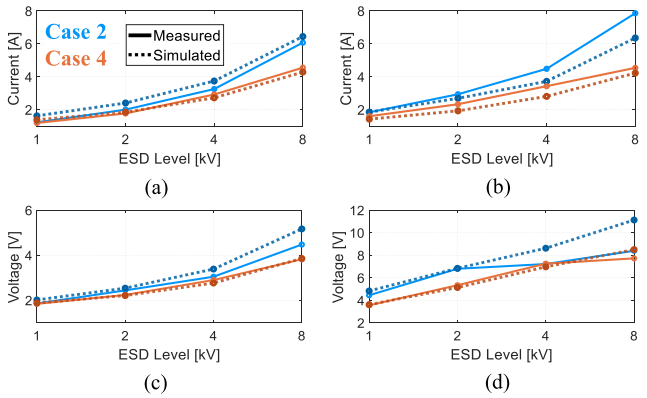

Fig. 19. Simulation performance for Case 2 (both ends grounded) and Case 4 (cable straight out) with a 1, 2, 4, and 8 kV contact discharge. (a) On-chip diode current at 10 ns. (b) On-chip diode peak current. (c) On-chip diode voltage at 10 ns. (d) On-chip diode peak voltage.

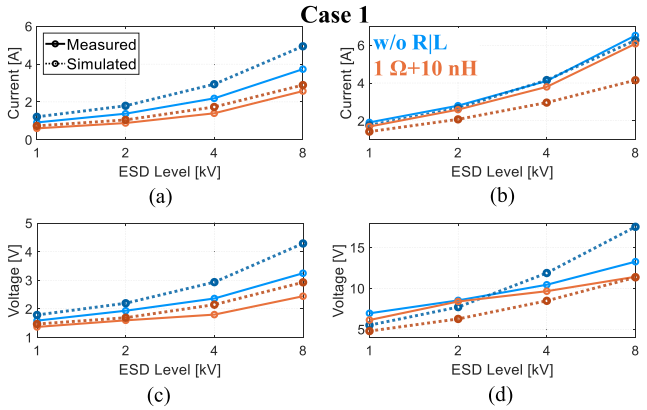

Fig. 20. Simulation performance for Case 1 (no cable) when 1) no passive components were added, and 2) with a 1 Ω resistor and a 10 nH inductor added between the TVS and on-chip diode. (a) Diode current at 10 ns. (b) Diode peak current. (c) Diode voltage at 10 ns. (d) Diode peak voltage.

level. Results are shown for both the quasistatic values at 10 ns (averaged from 9–11 ns), as well as the peak current and voltage. The steady-state current and voltage is predicted within 30% of those found through measurements, while peak currents and voltages are captured within 25%. There is less ESD stress at the on-chip diode in Case 4 than in Case 2, which is not surprising since the total injected current is much lower at the beginning of the Case 4 pulse waveform (see Fig. 13).

Tests were also performed when a 1 Ω resistance or 10 nH inductance was placed between the TVS and on-chip diode to simulate parasitics or other elements that might be present in an implemented circuit. Results are shown in Fig. 20 for Case 1 (no cable) and in Fig. 21 for Case 3 (cable grounded one end) for ESD gun discharges from 1 to 8 kV. The predicted peak and quasistatic voltages and currents match measurements within about 30%. The simulation of Case 1 performed worse than for Case 3, likely because of the rough approximation of the ESD gun using the simple current-source model. The additional impedance between the TVS and on-chip diode reduced the ESD stress seen by the on-chip diode as expected [17].

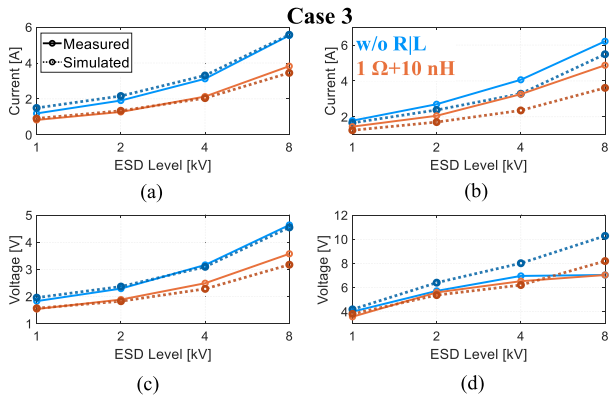

Fig. 21. Simulation performance for Case 3 (cable grounded one end) when 1) no passive components were added, and 2) with a 1 Ω resistor and a 10 nH inductor added between the TVS and on-chip diode. (a) Diode current at 10 ns. (b) Diode peak current. (c) Diode voltage at 10 ns. (d) Diode peak voltage.

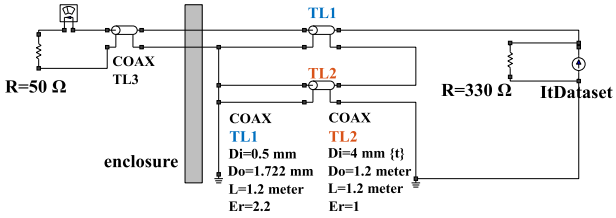

Fig. 22. Approximation of Case 4 when discharging to a 50 Ω load [16]: with inner path ("TL1," of 50 Ω characteristic impedance) and common mode path ("TL2," 377 Ω).

B. Impact of Cable Configuration

In the ESD immunity test with a contact mode discharge as defined in IEC 614000-4-2, the injected discharge waveform may deviate significantly from the waveform of the standard due to the impact of the cable configurations, leading to misleading immunity test conclusions. In particular, case 4 (cable straight out) leads to a substantial change to the discharge waveforms. With the help of full-wave simulations and some experiments (e.g., additional cable ferrites over the USB cable can eliminate the second peak at 10 ns in Case 4, Fig. 13), it was determined that the two peaks seen for Case 4 are due to the creation of an additional common mode current path along the outer shield of the USB cable [16]. The out shield of the cable, together with the ground plan 1.2 m below, roughly creates a transmission line with an impedance close to 377 Ω and wave velocity of 3E8 m/s, the wave impedance and propagation velocity in air. Correspondingly, a circuit model is shown in Fig. 22. TL1 represents the transmission line formed by the D+ pin and the USB cable shield. TL2 represents the transmission line formed by the cable shield and the ground plane. The discharge pulse at the inner conductor of the USB cable sees two parallel current paths: one along the inside of the 50 Ω USB cable and another along the 377 Ω common mode path along the outside of the shield. Since the initial pulse is split between these paths, the initial peak seen by the DUT is lower than when the cable shield is grounded. The second peak happens when the pulse following the cable shield is reflected at the enclosure and arrives back at the USB cable input. Simulations of the circuit in Fig. 22 demonstrate this basic explanation [16]. The simulation is not

perfect, as the cable shield 1.2 m above the ground plane cannot be perfectly represented by a TEM transmission line, but the result is close.

As can be seen, care should be taken when deciding the position and grounding of the USB cable in ESD tests. When the shield is un-grounded at the injection point [see Fig. 12(c) and (d)], the peak current will be lower than when the shield is grounded. The higher the cable above the ground plane, the lower the peak current. The duration between the first and second peaks is proportional to the cable length. These changes to the waveforms can impact if, or how strongly, the TVS turns ON, and thus, the peak current and total energy seen by the on-chip diode differ.

V. Discussion

Accurately predicting the combined response of a TVS and on-chip diode working together in a system-level simulation is challenging. It is essential to have a good understanding of the test board characteristics and to model these well. For example, results shown here demonstrate that the length and loss of the transmission line between the two devices must be captured to determine the amplitude, frequency, and duration of the resulting ringing that occurs when both devices turn-ON [see Fig. 17(b)]. It is also critical that behavioral models accurately capture the turn-ON behavior of the TVS and diode, including the turn-ON voltage as well as the shape of the rising and falling edges of their turn-ON response (just after the overshoot). A small error in the turn-ON behavior of the TVS will cause a large error in the predicted peak voltage seen by the on-chip diode. The importance increases with higher discharge levels [see Fig. 21(d)]. Without the improved model for conductivity modulation in the TVS, the error in the simulated peak currents and voltages can range from 30% to 210% when the discharge level is above 2 kV.

Properly capturing the ESD gun waveform seen on-board is similarly important. While the interaction between the ESD gun, enclosure, and the USB cable can be captured somewhat through full-wave simulation, the complexity is a concern, and fully predicting the waveform shape is difficult [15]. Here, we found that using a current source measured for each cable configuration was more accurate and easier to use than the full-wave simulation. The primary limitation to this approach is that the accuracy degrades after twice the cable delay, since the representative source cannot reconstruct the impact of reflections from the ESD gun impedance seen in the actual system. Measurements performed here, however, suggest the impact on the performance due to this limitation is minimal.

VI. Conclusion

The combined transient response of an off-chip TVS and on-chip ESD protection diode to an ESD gun contact discharge to a USB cable was studied with measurements and simulations. To accurately model the response, improvements were required for the TVS to properly capture the conductivity modulation that occurs after the snapback. The simple switch-based behavior of the previous model was replaced with a more physical nonlinear resistance that depends on the charge carried through the TVS. The modeling results were also improved by predicting the on-board waveform using a measured, rather than a simulated, source. This source could fully capture the interaction of the ESD gun, cable, and enclosure within the most critical first several nanoseconds of the waveform; and did a reasonable job even after. Overall, the SEED models presented here did a good job of accurately capturing the peak and quasistatic voltages and currents seen by the on-chip diode for various ESD gun injection levels and USB cable configurations, and when adding additional passive components to the circuit. Measured and simulated values matched within 30% or less. This level of accuracy is significantly better than observed in previous studies [15].

Results demonstrate the importance of the USB cable position and the method of grounding the shield. The board will see a two-peak event when the cable is far from the ground plane and the shield is unconnected at the discharge point. The size of the peaks and the time gap in between depend on the shield's size, the distance to the return plane, and the overall length of the cable, among other factors. The case where the cable was placed 1.2 m from the return plane, for example, produced an initial peak that was 50% smaller than when the cable was run along the enclosure with shield grounded at both ends. The cable position and grounding should be considered when determining ESD test strategies.

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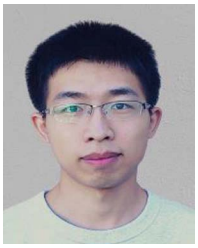

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