Analysis of Voltage Regulator Module (VRM) Noise Coupling to High-Speed Signals with VRM Via Designs

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***Abstract*— The physical noise coupling mechanism between voltage regulator module (VRM) noise coupling to high-speed signal traces is analyzed and different noise reduction methods are analyzed for the first time. The rapid switching of field effect transistors (FETs) creates an unintentional coupling region around the VRM. As high-speed traces are often routed in the inner signal layers of printed circuit boards (PCBs) as striplines for signal integrity, the VRM switching noise is mainly coupled from noisy power vias to the victim traces routed around the VRM region. To analyze different coupling reduction methods in practical high-speed channels, a simplified PCB design based on a high-speed server platform is proposed. Case studies under various conditions verifies the most effective VRM noise coupling reduction method. Different design parameters that influence the VRM noise coupling are analyzed to provide a design guide for high-speed channel designers.**

Keywords*— *voltage regulator module noise coupling, VRM power distribution network, via to trace coupling, PDN via design.

I. Introduction

In modern server systems, multiphase buck regulators are widely used for high efficiency. Multiphase buck regulators deliver stable DC output voltage from 12 V input voltage supply. However, fast-switching events associated with high and low-side power MOSFETs can cause a major electromagnetic interference (EMI) issue in dense integrated server platforms [1].

Different EMI issues caused by the VRMs are analyzed in [2-8]. VRM noise is coupled to high-speed traces and power planes, resulting in signal integrity (SI) and power integrity (PI) problems [5]. Many of the previous studies analyze the VRM noise coupling issues using a 3D and 2.5D full-wave simulation [6-8]. As majority of high-speed traces are routed in the inner signal layers, the previous studies mainly focused on the VRM via-to-signal via coupling as well as the coupling from noisy power planes to the signal via penetrating the power plane. To resolve the EMI issue caused by the VRM switching events, high-speed PCB designers often avoid placing decoupling capacitors under power via transitions because the decoupling capacitors can create a high switching current loop on the top layer as shown in Fig. 1. However, even with decoupling capacitors placed on the top, some conduction currents still couples to the return planes through the anti-pad the noisy of power via and can result in noise coupling to the high-speed traces within close proximity.

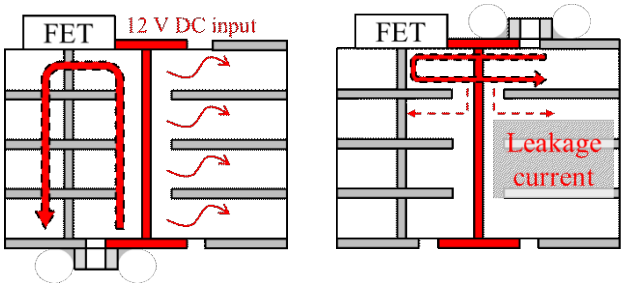

Fig. 1. EMI issue caused by switching VRM shown in the simplified PCB stack-up. (a) via transition due to the bottom de-cap. (b) reduced via transition with the top de-cap.

In this paper, the VRM noise coupling to the high-speed signal traces from the power distribution network (PDN) is introduced and analyzed using a simplified PCB design based on an actual server platform PCB. The high-frequency noise voltage is injected into the VRM power planes through the macro-model of VRM switching events [10], and the return currents on the ground planes are simulated using full-wave simulation. Based on the simulation results, the via to trace coupling design parameters that influence the noise coupling are analyzed. To validate the effect of coupling design parameters, transient simulation is performed with the extracted S-parameters from the simplified PCB design. Finally, optimization of power via design to minimize VRM to trace noise coupling is proposed based on the transient simulation results.

II. Analysis of VRM Noise Coupling

A. Simplified PCB Design for Analysis

To analyze the VRM noise coupling to high-speed traces, 3D and 2.5D full-wave simulations are used to extract the S-parameters or equivalent circuit models of PCB layouts. However, the simulation with the 3D and 2.5D models of large server board consumes relatively large computational resources. To reduce the full-wave simulation time for multiple designs, a simplified PCB design based on a practical server platform is proposed. The simplified PCB design includes the VRM noise coupling region in the signal layers. For the simplicity, the 5-layers stack-up is used in the simplified PCB design, composed of Top – GND – SIG – GND – Bottom layers. As victim of VRM noise coupling, a

stripline routed 100 mils away from the edge of anti-pad of VRM power vias is included in the simplified PCB design. A layout image from practical server design and corresponding simplified PCB design are shown in Fig. 2 for comparison.

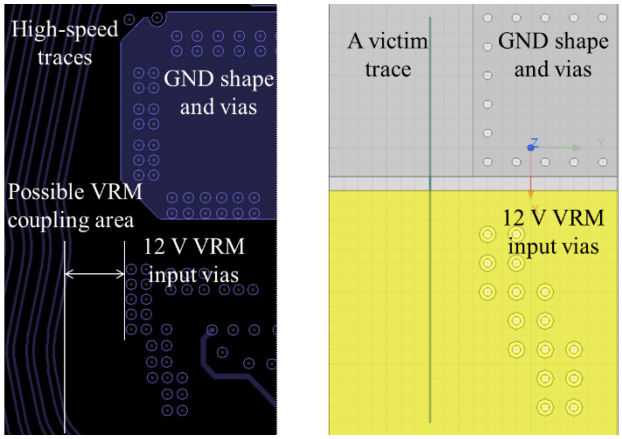

Fig. 2. (a) Target server platform. Distance between signal and VRM via is 100 mils (b) Proposed mock-up design. Trace and distance between signal and VRM via are 550, adn 100 mils, respectively. Total length and width are 15, 10 mm, respectively.

The simplified PCB design assumes no VRM power via transitions throughout the layers. To avoid via radiations as shown in Fig. 1(b), the high switching current loop is created on the bottom layer by applying the input voltage and VRM macro-model ports to the bottom layer. The estimated current path on the bottom layer is shown in Fig. 3. The major return current path is formed from the 12V VRM plane to the ground plane, as clearly indicated by the solid arrows to indicate return current However, a small amount of conduction current is leaked to the upper layer through the anti-pad of the power vias, as indicated by the dotted line in Fig. 3. This conduction current can be leaked to the upper ground planes for the high-speed stripline, which might cause inductive noise coupling.

B. *Design Parameters Affecting VRM Inducted Noise Coupling*

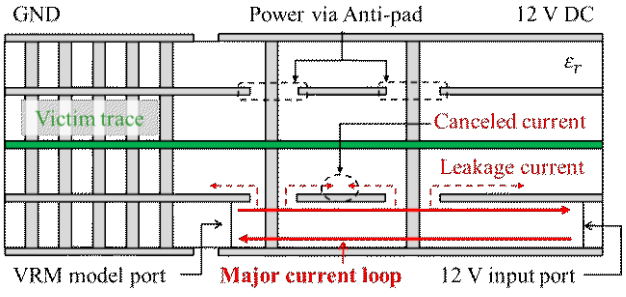

Fig. 3. Estimated current path of the simplified mock-up design in cross-sectional view. FR4 epoxy is used for dielectric layers. Thickness from the top to bottom dielectric layers are 2.7, 6, 3, 2.7 mils, respectively

The VRM noise coupling to high-speed traces can occur as shown in Fig. 3. In this section, the case studies are performed to evaluate different design parameters affecting VRM induced noise coupling. The design parameters that significantly affect the VRM to trace noise coupling are identified as follows:

1) Radius of VRM power via anti-pad: In the high-speed signal via design, single large shared anti-pad is often used to reduce the capacitance of differential via pairs [9]. However, the shared anti-pad for power vias can cause severe SI problems. As shown in top view of the simplified PCB design in Fig. 4, the leakage current dissipates out in all direactions from the anti-pad, and the current can be accumulated or reduced due to constructive and distructive interference according to the current direction. The current accumulating and reducing areas are highlighted in red and blue, respectively in Fig. 4(a). While most of the leakage current is cancelled out in VRM coupling region as shown in Fig. 4(a), the large shared anti-pad creates a stronger VRM noise coupling area as shown in Fig. 4(b). When the shared anti-pad is designed, most of the return current is leaked to close victim trace without cancelation. A large void on the ground plane pushes the conduction path even closer to the victim trace by accumulating the leakage current of each separated anti-pad, resulting in a larger and stronger coupling region. It is clear that the VRM coupling noise with a shared anti-pad design will be much larger in magnitued compred to that of the separated anti-pad design.

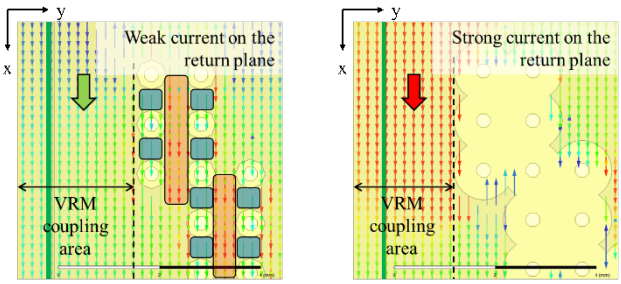

Fig. 4. Surface return current in the x-direction nearby the victim trace on the GND plane of the 4th layer of the PCB stack-up. (a) Power VRM vias with separated anti-pad. (b) Power VRM vias with shared anti-pads.

2) Distance between power vias and traces: To minimize the VRM noise coupling, PCB designers usually route the victim traces far from the noisy VRM power vias. Generally accepted seperation distance between VRM power vias and victim traces are minimum of 100 mils. In this case study, the distance between trace and the edge of the VRM power via anti-pad is analyzed. Since the return current path is significantly affected by the radius of the anti-pad, the seperation distance must be defined from the edge of the power via antipads, and not the center of the power vias. Therefore, the second design parameter that affects the VRM to trace noise coupling is the distance between the edge of the anti-pad to the victim trace.

3) Power via array design: As shown in Fig. 4(a), the leakage current can be canceled by the separated anti-pad for power vias. The VRM noise coupling can be determined not only by the anti-pad design but also the power via array design. In Fig. 4(b), a smaller and weaker coupling current region is formed right below the strong VRM coupling region. It is formed by the anti-pads of the second power via array. The strong return current in x-direction is canceled out due to the leakage current dispiating out from the second power via array. Based on this knowledge, the leakage current can be canceled with the appropriate power via patterns.

The time-varying current created by the VRM switching events is not considered since it is determined by the characteristics of the VRM circuit and power consumption of the server system, not the via and PDN designs. By considering the VRM noise coupling factors highlighted in this section, the transient analysis is performed for various power via designs.

III. Analysis of VRM Noise Coupling to the Traces

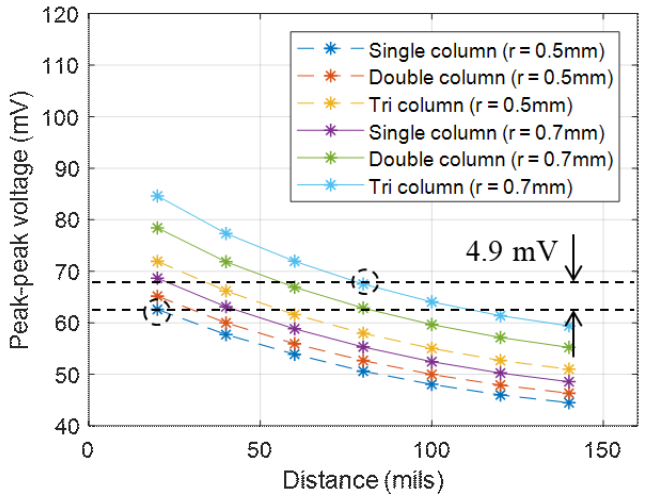

Fig. 5. VRM noise coupling depending on the investigated coupling factors: Number of straight power VRM via columns, antipad design, and distance between VRM power via and victim trace.

To evaluate the design parameters introduced in the previous section, the S-parameter models of simplified PCB designs are extracted using ANSYS HFSS. For the case studies, each design parameters are changed from the initial simplified PCB design. The 0.5 and 0.7 mm radius of VRM power via anti-pad are applied to realize the separated and shared anti-pad, respectively. The distance between the edge of the anti-pad and the victim trace is varied by parameter sweep from 20 to 140 mils in the 3D model. For the power via array design, the different number of power via column is used. The extracted S-parameter blocks from the modified simplified PCB designs are combined with the buck VRM behavior model [10]. With the combined simulation setups, the VRM noise coupling to trace is simulated. The peak-to-peak coupled voltage from VRM to victim trace is shown in Fig. 5.

In Fig. 5, the separated and shared VRM power via anti-pad designs are represented in dashed and solid lines, respectively. It is shown that the separated anti-pad usually induces less noise voltage on the victim trace. For the anti-pad to trace distance, it is clear that the trace routed far away from the power via has less noise voltage. The power via design with the number of via columns indicates that the severe VRM noise coupling occurs with the increased number of via arrays. The trace placed 20 mils away from the single via column with the separated anti-pad has a 4.9 mV lower noise voltage than the trace routed 80 mils away from the three power via columns with the large shared anti-pad design.

To minimize the VRM noise coupling to the victim trace, the pattern of VRM power vias is analyzed. Since the return current on the top surface of GND plane is dissipates away from the anti-pad of VRM vias, such return current can be canceled when the return current is formed in the opposite directions. The design comparison of modified VRM power via with the previous 3D model is shown on Fig. 6. The 3D model simulated in Fig. 5 is shown in Fig. 6(a). In this design, the return current is distributed evenly around the VRM vias resulting in the voltage coupling to the nearby victim traces. On the other hand, the specific patterns on Fig. 6(b) achieves the current cancelation in the highlighted area, and enough space between anti-pads and victim trace. The patterned VRM via design is combined with the buck VRM behavior model as a S-parameter function block and the transient noise coupling is simulated.

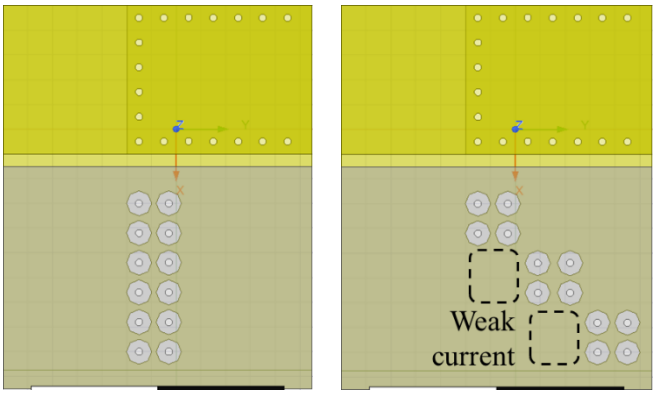

Fig. 6. Simplified PCB designs with (a) two straight power VRM via columns. (b) patterned power VRM vias. Identical stack-up with Fig. 3. Total width and length of PCB are 12.5 and 15 mm, respectively.

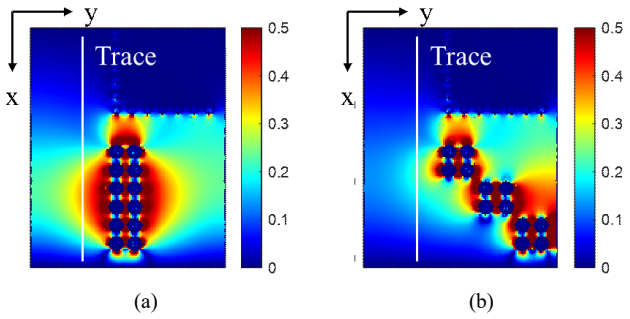

Fig. 7. Surface return current in the x-direction nearby the victim trace on the GND plane of the 4th layer of the PCB stack-up. (a) Two straignt power VRM via columns. (b) Patterned power VRM vias.

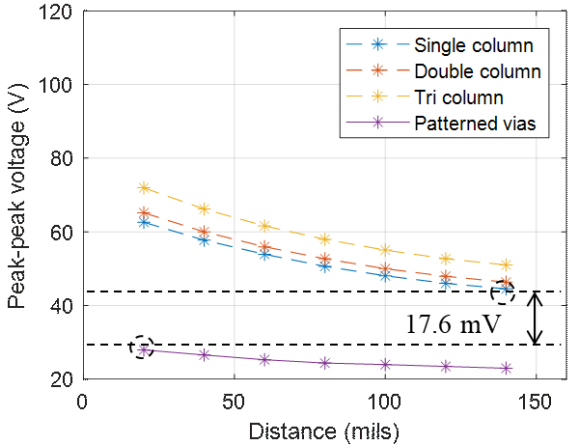

Fig. 8. VRM noise coupling depending on the power VRM via designs: Comparison between the straight power VRM via columns and patterned power VRM via design.

The simulation results are shown in Fig. 7 and 8. The separated anti-pad design is applied to the 3D models for improved noise coupling suppression. The return current on the GND plane of design Fig. 6(b) shows canceled surface current on the weak current area. For the new design, the coupled noise voltage of the patterned VRM via design shows 17.6 mV lower than the straight via column case. It is verified that the patterned VRM power via around the victim transmission line can achieve more effective noise suppression. The analysis results shown in Fig. 5 and 8 address that the power via design has a significant effect on the SI problems caused by the switching events of VRM circuits.

The simulation results show that the less number of VRM power vias has better SI performance. However, in DC analysis, larger number of VRM power vias has better performance in terms of IR drop. Since the stable VRM input voltage is required to achieve a proper operation of a step-down buck converter, the DC IR drop must be minimized. For DC stability, drilling the vias in the high voltage/current planes is recommended [11]. This is contrary to the AC simulation results performed in this paper. For the optimal power via design in the server platform, the balance between DC and AC analysis must be carried out in future research. This analysis results address that the power via design has a significant effect on the SI problems caused by the switching events of VRM circuits.

IV. Conclusion

In this paper, the VRM noise coupling to victim trace due to the power via design is investigated. Simplified PCB designs are proposed based on the possible VRM noise coupling region in the highly integrated server platform. In the simplified PCB design setup, via transition is restricted by forming the return current loop on the bottom layer of the 3D model. Three design parameters that significantly affect the level of VRM noise coupling are proposed. The proposed design parameter have a significant effect on the return current path and the transient simulations are performed with the extracted S-parameters. Based on the simulation results, the effect of each coupling factor is compared using the peak-peak coupled noise voltage. For future research, the optimal design of power via must be carried out to balance the AC/DC analysis and minimize the VRM noise coupling.

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