Analytical Comparison of 3-Level 2-Phase and Double-Step-Down Topologies for Integrated High-Ratio DC-DC Converters in BCD and GaN Process

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***Abstract*— This paper provides a comprehensive analysis and comparison between 3-level and double-step-down (DSD) integrated power converters, which are two of the most popular topologies for 48V-to-1V point-of-load conversion. Because DSD converters have two inductors, the 3-level topology in this study is also constructed with 2-phase interleaved operation (3L2P) to make the comparison fair. Same chip-area budget, loading conditions and ripples are also ensured, such that comparisons are made under similar bill-of-materials and power density to provide engineers a more practical view of the characteristics of both topologies. Theoretical analysis is provided with similarity in switching behaviors discovered. Transistor-level simulations are conducted in a 180-nm BCD and a commercially available enhancement-mode GaN processes, assuming all power FETs are integrated on-chip. The simulation results agree with our analysis. In conclusion, DSD converters can achieve an overall higher efficiency than 3-level converters at near-same conditions with same or smaller chip-area budget due to the much lower conduction loss. In addition, both topologies, especially the DSD, achieved significantly higher (up to 12%) efficiency in a 200-V GaN process compared to a 55-V BCD process despite being overrated (due to limited available options), because of the much lower switching loss. This makes GaN process worth considering for integrated high-ratio DC-DC converter designs even though the current fabrication cost will be higher.**

Keywords—48V-to-1V, High Ratio, Voltage Regulator, DC-DC Conversion, 3-Level Converter, Double-Step-Down Converter, Buck Converter, Direct Conversion, Gallium Nitride (GaN)

I. INTRODUCTION

Due to skyrocketing demands for internet- and cloud-related applications, data centers, as the backbone of these services, are the most fast-growing load on the grid. They consumed more than 200 TWh of energy in 2018, which is expected to increase by 15X by 2030 [1]. As such, the efficiency of power conversion in data centers are critical in relieving the energy and thermal stress and reducing carbon emissions. Data centers have started to migrate their intermediate DC voltage in the racks from 12V to 48V, which can reduce the current and thus losses in power transmission. However, it raises challenges in 48V-to-1V point-of-load (PoL) converters for low-voltage chips due to much higher step-down voltage conversion ratios (VCRs), for which conventional buck converters have considerably lower efficiency due to the 48-V high voltage swing at the switching node(s) with high current passing through high-voltage power transistors, with extra challenges in controller design with only ~2% duty cycle. Using multiple stages [2-4] is one of the most common ways to achieve a high voltage conversion ratio. For example, 48V-to-12V conversion in the first stage followed by 12V-to-1V conversion in the second stage. However, although each stage can be optimized separately to improve efficiency, the additional stages increase the number of components, which increase the form-factor and cost and reduce the power density that is also a critical specification for power converters. Similarly, transformer-based converters (e.g. resonant LLC or active-clamp forward topologies [5]) can provide high power capacity and efficiency in one stage, however, the power density is limited by the bulky transformer with increased form-factor. It is important to minimize the form-factor for 48V-to-1V converters along with increasing the power density because server racks have limited space available on the motherboard where such converters are located with the PoL chips, in addition to lower bill-of-material (BoM) with less components.

Researchers from industry and academia have proposed different hybrid topologies for high-conversion-ratio direct down-conversion, which take advantage of both switched capacitive and inductive topologies by combining them in different creative ways [6-21]. These topologies do not require transformers, but only capacitors and inductors, thus could be relatively easier to achieve a higher level of integration and power density. Among them, multi-level topologies, e.g. 3-level [8-16] converters, and double-step-down [17-21] converters have gained most popularity because of being viable for a wide range of applications. In the literature, there are several papers comparing the characteristics of integrated 3-level and DSD converters [22,23]. However, those papers compared traditional multi-level converters, which only have one inductor operating in single-phase, directly with DSD converters, which have two inductors interleaved with extra ripple cancellation. This places multi-level converters at a disadvantage as the condition is very different because inductors normally dominate the cost and volume of the overall power converter designs, and 3-level converters can also benefit from 2-phase interleaved operation for higher power capacity, better efficiency, and smaller ripples. In addition, previous comparisons were performed under different loading and chip-area conditions.

To provide a more practical view of the characteristics of the two topologies, in this paper, we will compare both 3-level and DSD topologies under near-same conditions by ensuring both topologies having: *1)* the same numbers of the same inductors; *2)* the same chip-area budget using the same process and voltage-rating power transistors; *3)* the same inductor current and output voltage ripples; and *4)* supplying the same amount of current. By doing so, a near-same BoM, power capacity and form-factor, thus power density, will be ensured during the analysis and comparisons. This will help engineers better understand the trade-offs between the two topologies and select the better one under practical constraints.

In addition, because GaN process become increasingly

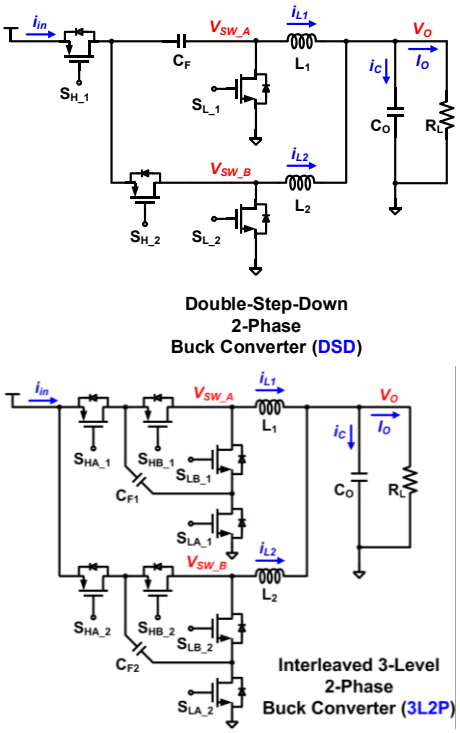

Fig. 1. Power stages of a DSD and a 3L2P buck converter to be analyzed and compared in this paper.

popular for monolithic power stage designs in recent years to achieve higher efficiency at higher frequency [24,25], comparisons between the two topologies in two processes, namely the conventional 180-nm BCD silicon process and the recently available enhancement-mode GaN process, will be performed. Considering the startup and transients of each topology, 55-V devices are used for the BCD process in this study. However, overrated 200-V transistors are used for the GaN process due to the limited available options (200-V or 650-V). The efficiency results are generated in Cadence using foundry-provided models in their process design kits (PDKs).

II. Switching Behaviour Analysis

A. Operation Principle

Fig. 1 shows the power stage configuration for both DSD and 3L2P topologies in comparison. Because the number of power transistors are not the same, the comparison will only be fair for integrated power converters with all the power transistors implemented on-chip, whereby transistor sizing for each topology can be optimized and adjusted to result in the same total chip-area budget despite the different transistor counts. In this comparison, even current balancing between the two phases of 3L2P is being ensured, which is often the case with multi-phase converters, to have a fair comparison with DSD that has inherent current balance between the two inductor currents. In terms of BoM, the only difference is the addition of an extra flying capacitor in 3L2P, which can be implemented with small-sized and low-cost SMD capacitors.

Both topologies have four states of operation [22]. However, DSD has only one switch in each current path, while 3L2P has two switches, in series, in each current path. For low VCR, i.e. smaller than 0.5, during state I, the high-side switch S_{H_1} is turned on along with the low-side switch S_{L_2} in DSD, whereas the switches S_{HA_1}, S_{LB_1}, S_{HA_2}, S_{LB_2} are turned on in 3L2P, charging the flying capacitors C_F and C_{F1}, C_{F2} in DSD and 3L2P, respectively. States II and IV connect the two switching nodes, V_{SW_A} and V_{SW_B}, to ground through the low-side switches. During state III, the switches S_{L_1} and S_{H_2} (S_{LA_1}, S_{HB_1}, S_{LA_2}, S_{HB_2}) are on for DSD (3L2P) discharging the flying capacitor(s) C_F (C_{F1}, C_{F2}) through the inductor(s) L_2 (L_1, L_2) in DSD (3L2P), respectively. It should be noted for 3L2P that during states I and III, the set of switches that are turned on comprise one high-side and one low-side switch as opposed to only one high-side switch for DSD. In other words, low-side switches of 3L2P conduct in three rather than two states but the effective conduction time of both topologies remain the same for the high-side and the low-side switches. It can also be observed from the steady-state analysis of DSD [20] that the low-side switch S_{L_1} carries current of the two inductors in state III as opposed to the other low-side switch S_{L_2} that carries only one inductor current when conducting. However, the two low-side switches can still have the same size for high conversion ratios due to the duration of state III being significantly smaller than the duration of states II and IV. In contrast, the low-side switches in 3L2P carry only one inductor current and usually have the same size. Although the switching scheme for the two phases of 3L2P described above considers the switching behavior in each state of both phases together, the two phases practically have the same states operating with a 90° phase shift.

A difference between the two topologies exists based on the steady-state average current of the two inductors. In each switching cycle of 3L2P, the flying capacitor of each phase interacts with a single inductor corresponding to that phase. As a result, voltage across this capacitor (V_{CF}) determines symmetry between the inductor current between the two charging phases of that inductor. DSD flying capacitor, on the other hand, interacts with both inductors, whereby it determines the symmetry between the currents of the two inductors every switching cycle as each inductor charges only once per switching cycle. Therefore, DSD inductor currents are balanced despite the mismatches such as series resistance of the inductors [20] due to inherent feedback loop [21] as opposed to 3L2P where the two inductor currents are independent of each other. It also means that V_{CF} in DSD is inherently balanced to half of the supply voltage (V_g) as V_{CF} is proportional to the difference of the two inductor currents [21] instead of the single inductor current in 3L2P.

In this study, flying-capacitor V_{CF} voltage is maintained to half of the supply voltage V_g (i.e. 0.5 of 48V or 24V) in steady state, which may not be the case during start-up or transients. Nevertheless, this is not an issue in this study as devices being used have a voltage rating higher than 48V. However, if low-voltage devices are employed to improve efficiency, additional techniques should be used to achieve V_{CF} balance and to avoid voltage across each device exceeding its breakdown limit. For instance, soft charging of the flying capacitors during start-up [15] can be used for 3L2P topology, and flying capacitor voltage-balance in steady-state can be maintained by adjusting the duty cycle [16,26].

B. Ripple Comparison

An important difference between the two topologies is that the duty cycle, D, in DSD is twice the VCR, whereas it is same as the VCR in 3L2P. In addition, frequency of switching nodes in 3L2P is twice the switching frequency, f_{sw}, as opposed to being same as f_{sw} in DSD. It has been observed that when operated at the same frequency, inductor current ripple, Δi_L, and output capacitor current ripple, Δi_C, are 2X

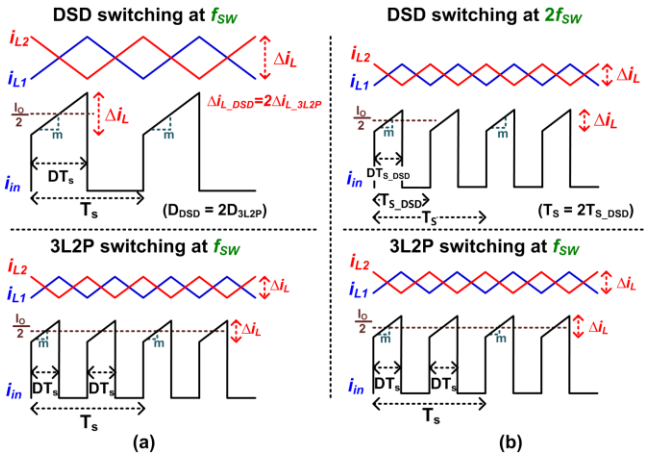

Fig. 2. Input current and inductor current ripples for (a) same frequency operation of DSD and 3L2P, and (b) DSD being operated at 2X the frequency of 3L2P.

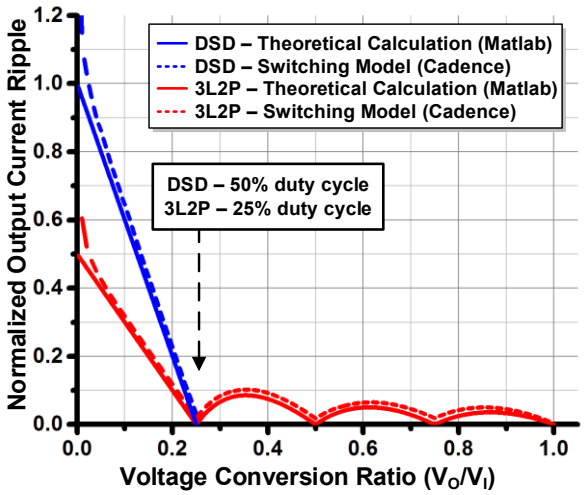

Fig. 3. Normalized output current ripple comparing theoretical and switching models for both DSD and 3L2P.

larger for DSD compared to 3L2P. This, in turn, means input currents are also different as elaborated in Fig. 2. As slopes of the inductor currents, m, are the same, longer charging period in DSD increases ripples. Δi_L for VCR<0.25 can be derived as:

$$\Delta i_{LDSD} = \frac{V_o}{L}.\frac{1}{f_{sw}}.\left(1 - 2\frac{V_o}{Vi}\right) \quad (1a)$$

$$\Delta i_{L3L2P} = \frac{V_o}{L}.\frac{1}{f_{sw}}.\left(0.5 - \frac{V_o}{Vi}\right) \quad (1b)$$

for DSD and 3L2P, respectively, where Δi_{LDSD} or Δi_{L3L2P} applies to both inductors. Due to the interleaving of the two inductor currents, Δi_C, which is the current charging and discharging C_O, $\Delta i_C = \Delta(i_{L1} + i_{L2})$, will be smaller than Δi_L due to cancellation effect, and can be written as:

$$\Delta i_{C3L2P} = \frac{V_o}{Lf_{sw}}\left(0.5 - 2\frac{V_o}{Vi}\right) \quad (2a)$$

$$\Delta i_{CDSD} = \frac{V_o}{Lf_{sw}}\left(1 - 4\frac{V_o}{Vi}\right) \quad (2b)$$

, for 3L2P and DSD, respectively. Fig. 3 plots the normalized (to $Lf_{sw}/(I_O R_L)$) output current versus VCR with theoretical models in MATLAB and switching models in Cadence for both topologies, in which D is limited to 0.5 for DSD due to its operation principle. To achieve the same output ripples, 3L2P can be operated at half the frequency of DSD with $f_{sDSD} = 2f_{s3L2P}$. On the other hand, the C_F voltage ripple, $\Delta V_{CF} = \frac{I_O}{2C_F}.t_{on}$, is the same for both converters since the current and t_{on}, which is the high-side on time as $t_{on} = (2D \times T_S)_{DSD} = (D \times 2T_S)_{3L2P}$, are the same for both topologies. Output voltage ripple, ΔV_O, for VCR<0.25 are given by:

$$\Delta V_{oDSD} = \frac{V_o}{16LC}.\frac{1}{f_{sw}^2}.\left(1 - 4\frac{V_o}{Vi}\right) + \Delta i_{CDSD}.ESR_C \quad (3a)$$

$$\Delta V_{o3L2P} = \frac{V_o}{16LC}.\frac{1}{f_{sw}^2}.\left(0.5 - 2\frac{V_o}{Vi}\right) + \Delta i_{C3L2P}.ESR_C \quad (3b)$$

, for DSD and 3L2P, respectively, where ESR_C is the equivalent series resistance of C_O.

III. Power Loss Analysis

A. DSD versus 3L2P Topology

Switching and conduction losses are the primary losses in a DC-DC converter. Here, switching loss, P_{SW}, include the transition loss, P_{OSS}, and gate switching loss, P_G. The transition loss occurs due to charging of the gate-source shorted output capacitance, namely C_{OSS}, when power transistors transition from ON state to OFF state, while gate switching loss is incurred due to charging of the drain-source shorted input capacitance, namely C_{ISS} of the transistor. The conduction loss, P_C, occur due to current flowing through resistive components in the current paths. For instance, inductor current, which can be written as:

$$i_L(t) = \begin{cases} \frac{\Delta i_L}{DT_s}t + \frac{I_o}{2} - \frac{\Delta i_L}{2}, & 0 < t < DT_s \\ \frac{-\Delta i_L}{(1-D)T_s}t + \frac{I_o}{2} + \frac{\Delta i_L(1+D)}{2(1-D)}, & DT_s < t < T_s \end{cases} \quad (4)$$

, causes conduction losses in the inductors due to the series resistance, DCR_L, that can be expressed by

$$P_{LDCR} = \left(\frac{I_O^2}{4} + \frac{\Delta i_L^2}{12}\right).DCR_L \quad (5)$$

Both topologies have identical inductor currents when $f_{sDSD} = 2 * f_{s3L2P}$ is followed with which in (4), T_S (the time period of the switching signals) will become $2T_S$ for 3L2P. The inductor current has two components: first segment from time *0* to DT_S denotes the charging of each inductor either by the input source or by the flying capacitor, and second segment from DT_S to T_S denotes discharging of each inductor while switching nodes are connected to the ground (states II/IV) with each inductor carrying half the output current on average. The other major sources of conduction losses are the on-resistances of the power switches. Given that $f_{sDSD} = 2f_{s3L2P}$ but with the same t_{on}, comparison can be made with two different assumptions.

a) Same Total Chip-Area Budget Assumption. In this case, the size of each transistor in 3L2P is half that of DSD due to 2X number of transistors. With 2X number of transistors in the current paths, the transistor conduction loss and switching loss of 3L2P will be 4X and 0.5X that of DSD, respectively. The power breakdown for this case is shown in Fig. 4. As expected, P_G and P_{OSS} for 3L2P is half that of DSD while P_{CON} is 4X that of DSD for each case of output voltage and frequency. For example, comparing the case of 550kHz f_{sw_DSD}, the red versus blue bars, verifies the expected loss breakdown. It can also be seen, by comparing the blue versus orange bars, for instance; that decreasing the frequency from 550kHz to 200kHz, decreases $P_{SW} = (P_G + P_{OSS})$ proportionally while

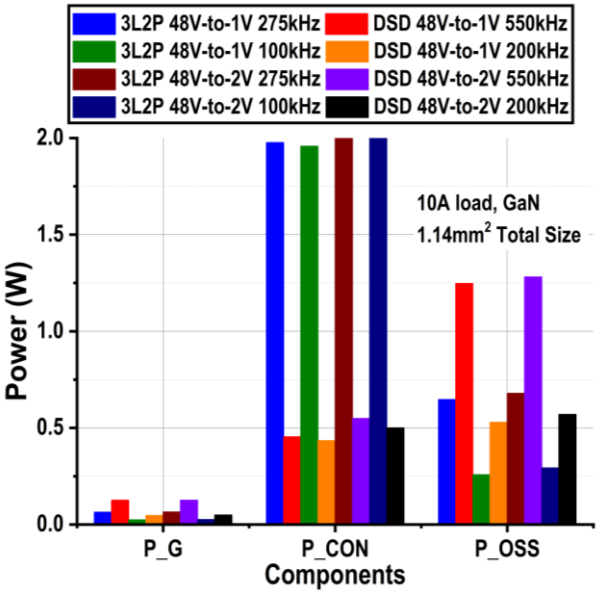

Fig. 4. Power breakdown comparison of GaN-based DSD vs 3L2P power stages under the same conditions and with the same total chip-area budget assumption (as labeled).

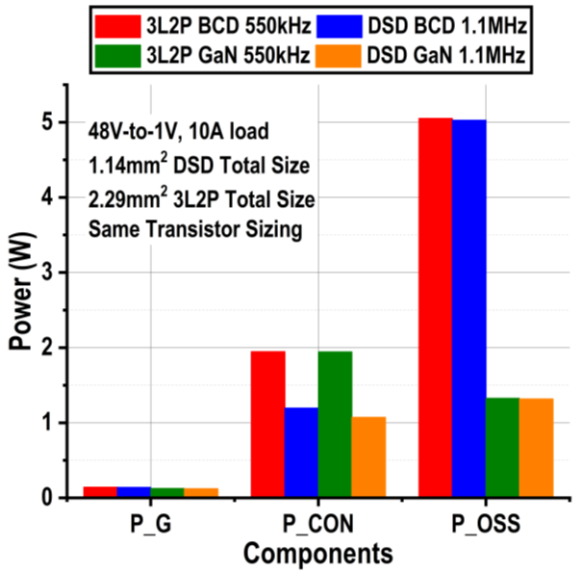

Fig. 5. Power breakdown comparison of BCD-based vs GaN-based DSD and 3L2P power stages under the same conditions with the same transistor sizing assumption (total area labeled).

P_{CON} remains the same as loading current is the same. The efficiency of 3L2P topology for this scenario can be approximated as follows given that simulation data of DSD topology, comprising power loss breakdown and efficiency, is available:

$$\eta_{DSD} = \frac{P_{OUT}}{P_{OUT}+P_G+P_{CON}+P_{OSS}}, \quad (6a)$$

$$\eta_{3L2P} = \frac{1}{\frac{1}{\eta_{DSD}}+\frac{6P_{CON}-P_G-P_{OSS}}{2P_{OUT}}}, \quad (6b)$$

As an example, consider the following DSD simulation data for a total size of 0.54mm^2: f_{SW_DSD} = 1.1MHz, f_{SW_3L2P} = 550kHz, V_O = 1V, I_O = 10A, P_{CON} = 2.38W, P_{OUT} = 10.03W, P_G = 64.1mW, P_{OSS} = 2.19W and η_{DSD} = 68.4%. From this data, 3L2P with the same total chip size gives 48% (52% from Cadence simulation) efficiency. Differences in the actual power breakdown between the 3L2P and the DSD that might occur due to imperfections in simulation measurements and conditions account for the difference in the estimated versus actual efficiency as the above expression assumes the same P_{OUT}, but $0.5P_G$, $0.5P_{OSS}$ and $4P_{CON}$ for 3L2P. The improvement in efficiency of DSD when scaling the output voltage alone is given by:

$$\eta_{DSD\_nV} = \eta_{DSD\_1V}.\left[1+\frac{\frac{n-1}{n.P_{OUT}}}{\frac{P_G+P_{CON}+P_{OSS}}{}+1}\right] \quad (7)$$

, where n is the factor by which output voltage is being scaled. For instance, increasing output voltage to 2V, with n = 2, given the same power components at 0.54mm^2 as mentioned before, BCD DSD efficiency is expected to increase from 68% to 81%. If the output voltage is increased further to 4V, with n = 4, 89% efficiency is expected. It can also be observed from (7) that at higher output power, efficiency gain, achieved from increasing output voltage, decreases. Likewise, the efficiency gain also reduces at lower frequencies because P_G and P_{OSS} components are reduced with respect to P_{OUT}.

Another comparison result that can be derived from Fig. 4 is at different VCRs. For instance, the red versus purple bars shows 1V versus 2V output comparison for DSD having P_{CON} approximately equal for both cases. This is due to the fact that increasing V_O increases conduction time of the charging-phase devices but proportionally reduces the conduction time of the discharging-phase devices, they do not cancel each other out though due to different sizing of the high-side and the low-side transistors. Similar result is observed for 200kHz, by comparing the orange versus black bars. Similarly, 3L2P also exhibits approximately equal P_{CON} for both conversion ratios. However, efficiency for higher VCR is higher as explained below due to differences in output power with roughly the same losses.

b) Same Transistor Sizing Assumption. If same size for each transistor is assumed for DSD and 3L2P i.e. 2X total size of 3L2P compared to DSD topology, then switching loss will be identical but 3L2P will have 2X the transistor conduction loss compared to DSD. For this case, following expression provides an estimate of the efficiency of 3L2P topology when DSD simulation data is available:

$$\eta_{3L2P} = \frac{1}{\frac{1}{\eta_{DSD}}+\frac{P_{CON}}{P_{OUT}}}, \quad (8)$$

As an example, consider the following DSD simulation data for a total size of 0.54mm^2: f_{SW_DSD} = 1.1MHz, f_{SW_3L2P} = 550kHz, V_O = 1V, I_O = 10A, P_{CON} = 2.38W, P_{OUT} = 10.03W, and η_{DSD} = 68.4%. From this data, the 2X size of 3L2P i.e. 1.08mm^2, gives 59% (60% from Cadence simulation) efficiency. As before, differences in the actual power breakdown between the 3L2P and DSD account for the difference in the estimated versus actual efficiency as the above expression assumes the same P_{OUT}, P_G, and P_{OSS}, but $2P_{CON}$ for 3L2P. The above expression also shows that for the same P_{CON} as noted above from Fig. 4 but different output power i.e. different VCR with the same loading current, higher output voltage should have higher efficiency results. This is because for the same amount of loss, output power increases and efficiency is the ratio of P_{OUT} to $(P_{OUT}+P_{LOSS})$.

The power breakdown for this case is shown in Fig. 5 for both BCD and GaN technologies under the same conditions for VCR resulting in 1V output voltage with l0A loading conditions. This comparison is revealed by horizontal comparison from Fig. 5, that is the red versus blue, and the

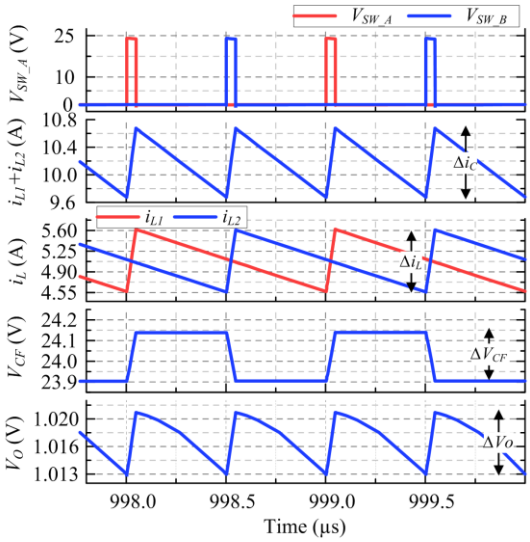

Fig. 6. Identical waveforms for DSD and 3L2P power stages, with 3L2P switching at half the frequency of DSD.

green versus orange bars. As expected, values of P_{SW} are close to each other while values of P_{CON} for DSD are half that of 3L2P for both BCD and GaN technologies.

B. BCD versus GaN Technology

GaN devices are well-known for being more efficient compared to silicon devices. However, only lower parasitic capacitances, especially drain-source capacitance, provide an advantage in this study as voltage-rating of the two devices are different and we have observed approximately equal on-resistance of the two devices when both are sized to achieve the same area. As a result, 200V-GaN devices exhibit ~4X lower transition loss but approximately the same conduction loss, compared to the same-sized 55V BCD devices in each topology. The Cadence simulation results of this observation are shown in Fig. 5, when comparing vertically, as the red versus green and the blue versus orange bars. Thus, the use of GaN devices as power transistors in each topology are anticipated to provide significant efficiency improvements when compared to the BCD devices with the same total size. The efficiency of GaN-based topology can be derived as follows:

$$\eta_{GaN} = \frac{1}{\frac{1}{\eta_{BCD}} - \frac{(k-1)P_{OSS}}{kP_{OUT}}}, \tag{9a}$$

$$k = \frac{P_{OSS\_BCD}}{P_{OSS\_GaN}} \approx 3.8 \tag{9b}$$

, where k is the BCD to GaN transition-loss ratio which is found to be 3.8 from simulations. The right-hand side of (9a) contains parameters determined using the simulation data of a topology using the BCD switches. Notice that P_G is assumed to be identical for the same sizing of BCD and GaN devices in (9a) as this ratio from BCD to GaN is found to be 1.13 (~1) from the simulations. For instance, consider the following BCD DSD simulation data for a total size of 1.14mm^2: f_{SW_DSD} = 1.1MHz, V_O = 1V, I_O = 10A, P_{OSS} = 1.32W, and η_{BCD} = 62.4%. Using the above expression, the same size of GaN DSD gives 81% (80% from Cadence simulation) efficiency.

IV. Verification and Comparison

Fig. 6 shows the simulation waveforms of transistor-level power stages in Cadence for both DSD and 3L2P. Both converters are supplying 10-A load current with 48V-to-1V conversion, 1μH inductors, 40μF output capacitor and 1μF flying capacitors. The DSD and 3L2P are switching at 1 MHz

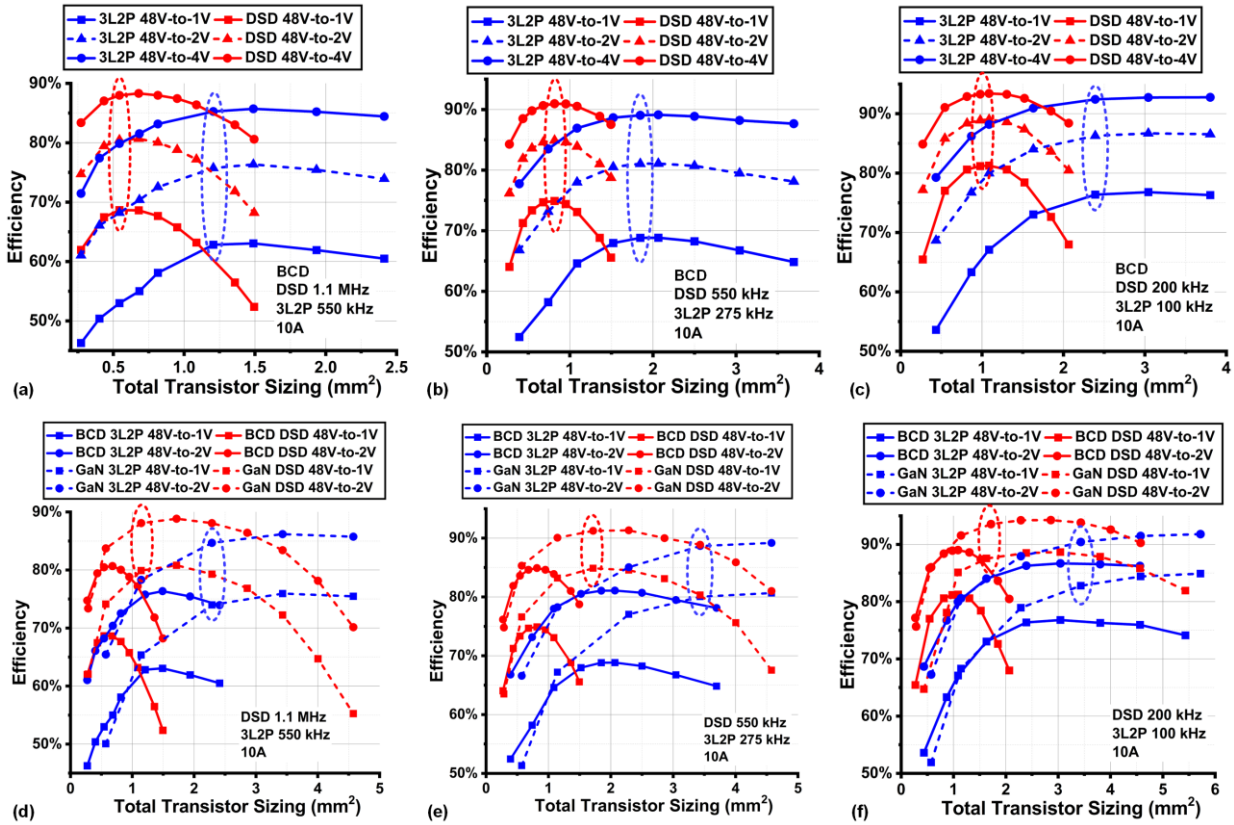

Fig. 7. Efficiency vs total chip area comparison of DSD vs 3L2P topologies under the same conditions for different switching frequencies and conversion ratios. (a-c): BCD, with DSD vs 3L2P at different VCR with different switching frequencies; (d-f): BCD vs GaN, with DSD and 3L2P at 48V-1V/2V and different switching frequencies.

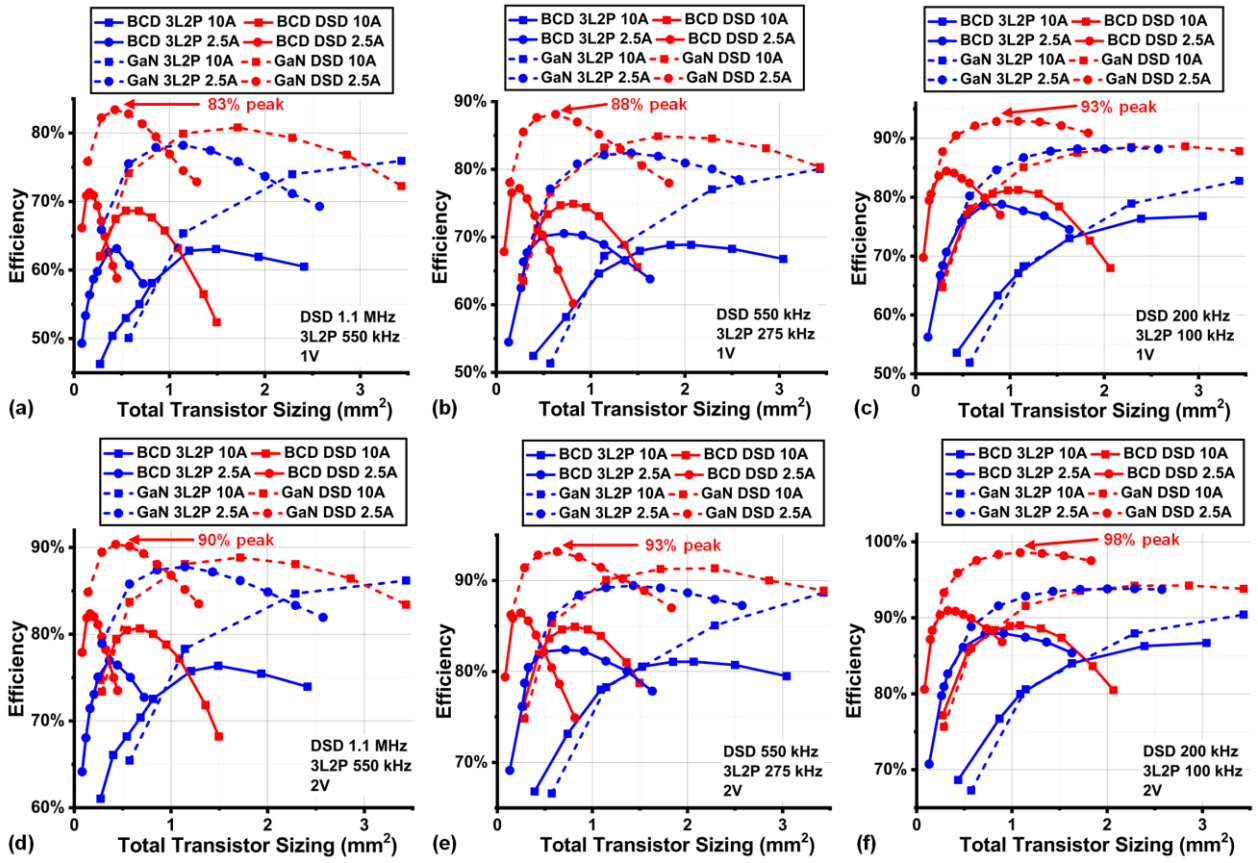

Fig. 8. Efficiency vs total chip area comparison of DSD vs 3L2P topologies under the same conditions for different loading conditions. (a-c): 48V-1V, DSD and 3L2P with BCD and GaN at 2.5A/10A loading conditions; (d-f): 48V-2V, DSD and 3L2P with BCD and GaN at 2.5A/10A loading conditions.

and 500 kHz, respectively, and have identical waveforms, which verifies our previous analysis. Fig. 7 (a-c) shows simulation results for efficiency versus total transistor sizing for both topologies using BCD at various operating conditions while maintaining the same loading current and inductors between the two topologies. The approximate peak efficiency points, considering area-efficiency trade-offs, are enclosed in the oval shapes which occur at around twice the area for 3L2P than DSD, as expected due to the 2X number of switches in the current path in 3L2P. In addition, the peak efficiency of DSD is higher for each VCR compared to 3L2P due to higher power losses in 3L2P as described above. Moreover, it can also be seen that efficiency of each topology increases with decreasing frequency due to reduced switching loss. Yet, efficiency of DSD stands higher than 3L2P due to difference in the conduction loss verifying the previous analysis. Furthermore, the efficiency increases when increasing output voltage from 1V to 2V and then to 4V as per the previous calculations from (7) in Section III.A but the efficiency gain reduces when comparing higher output voltages as expected from the previous analysis. Next, if we compare the efficiency versus switching frequency for 1V/10A conditions, then optimum efficiency of DSD improves from 68% to 75% to 81%, for 1.1MHz, 550kHz and 200kHz, respectively.

Fig. 7(d-f) provides comparison of BCD versus GaN technologies. The GaN results are shown alongside previous BCD results at two output voltages, 1V and 2V. The best area-efficiency combinations for GaN are also highlighted. As before, optimum size of 3L2P is almost doubled of that of DSD, efficiency improves for both topologies at lower frequencies with DSD always being better in terms of area-efficiency trade-off, but efficiency gain reduces at lower VCR.

TABLE I. INDUCTOR PARAMETERS USED FOR EFFICIENCY RESULTS

f_{SW_DSD}	$f_{SW\_DSD} = 2f_{SW\_3L2P}$ **Same Inductors for DSD and 3L2P DCR 8mΩ, $L_1 = L_2$**		
	Output Voltage, V_O		
	1V	***2V***	***4V***
1.1MHz	1µH	2µH	4µH
550kHz	2µH	4µH	8µH
200kHz	5.5µH	11µH	22µH

Moreover, the efficiency of GaN-based DSD surpasses the efficiency of BCD DSD, BCD 3L2P and GaN 3L2P. In fact, GaN DSD has a considerably higher efficiency compared to 3L2P. For instance, 1mm^2-sized GaN DSD has almost 15% higher efficiency compared to the same size of GaN 3L2P. Similar trend is observed at different VCRs as well as at lower frequencies. Upon comparing the efficiency versus switching frequency for 1V/10A conditions, it can be seen that optimum efficiency of GaN DSD increases from 80% to 85% to 88% as frequency decreases from 1.1MHz to 550kHz to 200kHz, respectively. These optimum efficiencies are materially higher than the BCD DSD for the same conditions. For instance, 1V/10A/1.1MHz GaN DSD has optimum efficiency almost 12% higher than the optimum efficiency of BCD DSD under the same conditions. These results are expected from our earlier analysis of power breakdown because a GaN-based design has been observed to have significantly lower P_{OSS} than a BCD design of the same topology. The total transistor sizing is computed using length, width, fingers and multipliers of the devices, without considering the additional area occupied by

the layout of each device due to isolation rings, substrate/well taps etc. as layout varies from designer to designer and from process to process, and such variations will make it difficult for a fair comparison.

Another important parameter that affects the efficiency is the loading current. The simulation results at various frequencies for both topologies and both technologies under different loading conditions, i.e. 2.5A and 10A, but the same inductors (between topologies and technologies, but different at different frequencies and voltages as summarized in Table I) and output voltages are shown in Fig. 8. Fig. 8 (a-c) depict the 1V results, whereas Fig. 8 (d-f) depict the 2V results. The optimum size shifts to a smaller value at lower current as P_{CON} reduces relative to P_{SW}. The peak values for 2.5A curves are also shown to illustrate the effect of changing the switching frequency or the output voltage. The previous analysis is validated by these results as well. As expected, GaN DSD has higher efficiency than BCD DSD which is higher than both GaN 3L2P and BCD 3L2P. As mentioned earlier, the peak efficiency improves with lower loading current due to smaller P_{CON} and it also improves with lower frequencies due to lower P_{SW}. Further, increasing VCR improves the efficiency too for all the cases as described earlier. Combining these results gives the best-case peak efficiency at 2V output, 200kHz frequency, 2.5A loading current for GaN DSD which is shown in Fig. 8(f). The peak efficiency in this case reaches 98%. Such a high value for GaN DSD is evident from the previous calculations too. The aforementioned power-breakdown values for 0.54mm^2 can be modified to get the expected efficiency from (6) for BCD operating at these conditions as follows: reducing P_{CON} by 16 times as current is reduced by 4 times, reducing P_G and P_{OSS} by 5.5 times as frequency is reduced by 5.5 times and reducing P_{OUT} by 2 times due to lower output current and higher output voltage. As a result, BCD DSD should have 90% efficiency at the given conditions, verified by the 0.54mm^2 point plotted in Fig. 8(f). This efficiency and the modified breakdown values can then be substituted in (9a) to get the expected GaN DSD efficiency at the same conditions which is found to be 95%, also verified by the 0.54mm^2 point from GaN DSD curve plotted in Fig. 8(f).

For 3L2P, even when switching at half the frequency of DSD, DSD almost always shows better efficiency compared to 3L2P, even with smaller chip-area budget. The efficiency difference, however, starts to decrease with lower switching frequencies. This provides better efficiency at a cost of larger inductors thus lower power density. In addition, GaN-based design provides further efficiency improvement for the same total sizing under almost all the operating conditions in both DSD and 3L2P topologies. However, there is a cost-benefit trade-off because GaN-based chip fabrication can be relatively more expensive than a Si-based chip fabrication.

Small-signal control-to-output transfer function of DSD is also almost the same as that of a conventional two-phase buck converter [20]. The three-level buck has the same control-to-output transfer function as that of a conventional buck [3]. Therefore, DSD is also expected to have almost the same control-to-output transfer function as that of a 3L2P converter.

V. Conclusion

In this paper, we have provided a comprehensive comparison between DSD and 3L2P topologies with carefully controlled conditions. Based on the analysis and verification results, the switching waveforms are identical when 3L2P is switched at half the frequency of DSD, while DSD can achieve better efficiency even with a smaller chip area. Further efficiency improvements can be achieved by using GaN devices for the power stage. Although GaN fabrication might cost more, it is worth considering given the efficiency benefits achieved for each device despite of having 4X higher voltage rating than BCD devices. For instance, 48V-to-1V 2.5A loading current GaN DSD having an area of 1mm^2 is 93% efficient when switched at 200kHz which increases to 98% for 48V-to-2V. Thus, GaN DSD is a better design choice considering area constraints to achieve an efficient direct down-conversion, especially for very high down-conversion ratios such as 48V-to-1V.

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