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Near Field Scanning-Based EMI Radiation Root Cause Analysis in an SSD

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***Abstract*—In modern portable electronic devices, solid-state drives (SSDs) are commonly used and have been identified as one of the dominant electromagnetic interference (EMI) noise sources that can cause RF desensitization issues. In this paper, the EM emission source from an SSD module is identified and analyzed using near field scanning and dipole moment source reconstruction. The identified noise current path including the power management integrated circuit and the decoupling capacitor is validated with the assistance of full-wave simulation. The measured noise voltage is used as an excitation in the simulation and the simulated near fields showed a good correlation with measured near fields in both pattern and magnitude. Based on the validated radiation mechanism, an optimized layout is proposed and validated in simulation reducing the far field radiation by 10 dB.**

Keywords—EMI, near field scan, radiation mechanism, SSD

I. Introduction

Due to the increasing speed and complexity of recent electronic technologies, the internal structures of mobile platforms including phones and laptops are becoming more and more compact. The distance between antennas and high-speed modules is getting closer, which causes the radiated electromagnetic noise can be picked up by the radio frequency (RF) antennas [1], resulting in RF desensitization on the receivers as discussed in [2]. Electromagnetic interference (EMI) problems are owing to different noise sources, such as dynamic random-access memories (DRAMs) [3], USB connectors [4], heatsinks [5], and flexible flat cables [6]-[7].

Because of its high memory/dimension ratio, solid-state drive (SSD) is widely installed in portable devices. However, such high-speed modules could be the critical radio frequency interference (RFI) noise source. As reported in [8], the SSD module could degrade RF sensitivity causing problems such as global positioning system (GPS) failure. When the SSD module is located 60 cm away from the GPS antenna, the positioning accuracy is still affected [9]. Therefore, detecting, analyzing, and resolving EMI issues in an early stage of the design process is beneficial.

The design of SSD is complex and many modules could be a potential noise source for EMI problems, such as NAND chips, DRAM chips, controller integrated circuits (ICs), DC-DC converters, and interface connectors, and the dominant noise source could vary in different SSD models. It is common practice to use near field scanning to identify and locate the noise sources [10]-[12]. One would map the locations of the hot spots in the measured electric and/or magnetic fields to the layout and infer suspicious points in the layout. Although it could be a good starting point for troubleshooting, there is no well-established systematic procedure to relate the near field patterns to the exact current path in the layout.

In this paper, near field scanning is used to systematically locate the current path of an SSD that is responsible for EMI. Locating the noise current path is done based on the dipole moment source reconstruction and by relating the reconstructed source to the layout. Full-wave simulations using the actual layout and the measured voltage waveform are carried out for validation. The reproduced H-fields showed well-matched patterns compared to the measured H-fields and the differences in the magnitude are less than 5 dB. Based on the understanding of the current path, an optimized layout is proposed and validated reducing the far field radiation by 10 dB.

II. Near Field Scanning

The device under test (DUT) of this paper is an SSD mounted on a laptop, as shown in Fig. 1. To avoid the idle state of the SSD, a script was executed during the measurement to maximize the communication between SSD and the motherboard.

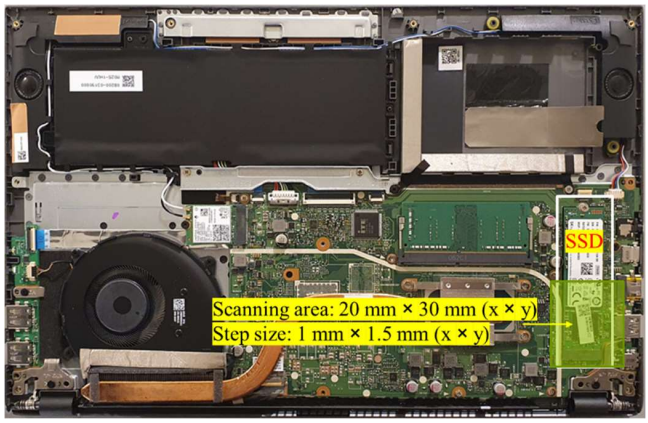

Fig. 1. The SSD and the laptop used in this paper.

Fig. 2 shows the diagram of the near field scanning measurement setup. A broadband H-field probe (2 mm × 1 mm aperture size) was mounted on the robot arm, which was digitally controlled in three dimensions. The robot arm can rotate the probe by 90 degrees to measure two perpendicular field components H_x and H_y. The output of the probe was connected to a spectrum analyzer and two cascaded low-noise amplifiers were used. The scanning height was 2.1 mm from the top surface of the SSD board. The probe calibration was

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performed before the scanning with a coplanar waveguide (CPWG) following the procedure reported in [13].

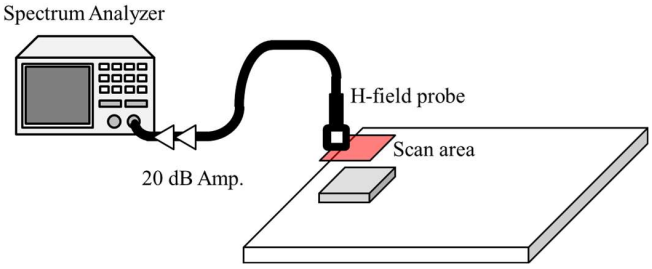

Fig. 2. Illustration of near field scanning setup.

Fig. 3 shows the H-field patterns of an ideal M_y dipole moment placed in the center, observed on a plane 2 mm above the source. A similar pattern could be found in the scanning results. The measured H fields are overlaid with the layout in Fig. 4. It was clear to see a four-leaf clover pattern in H_x component and a division sign pattern in H_y component, which are close to the H-field patterns of an ideal M_y (Fig. 3). 300 MHz case is shown here as an example, but similar patterns were observed from 200 MHz through 1100 MHz. From Fig. 4, we know that the dipole location, i.e. the noise source on the layout, is at the center of near field patterns. By mapping the near field scanning results onto the SSD, we found that there is a buck converter at the center of the patterns. Because the noise type is an M_y dipole, the current path creating the noise emission should be on the xz-plane with its normal vector pointing to the y-direction. The detailed noise current path and radiation mechanism are discussed in the next section.

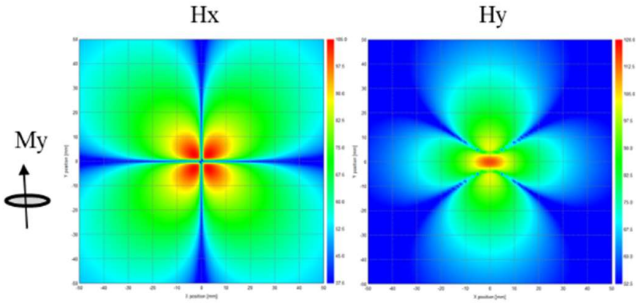

Fig. 3. Ideal H-fields above M_y dipole moment.

III. Radiation Mechanism Analysis

From the reconstructed source based on the near field scanning, there are two important pieces of information: 1) the potential current path is on the buck converter circuit and 2) the current loop should be on the xz-plane. As reported in [14], there are mainly three possible mechanisms can generate EMI issues in buck converters, including the switching frequency harmonics, the ringing on the phase voltage loop, and the reverse recovery noise. The study in [15] reports that the ringing of the phase voltage loop usually contributes to the EMI issue above 100 MHz. The ringing noise current path was a loop including the high-side (HS) field-effect transistor (FET), the low-side (LS) FET, and the input decoupling capacitors as shown in Fig. 5. By traveling along the same current path on the layout of DUT, we found the same current path could form a loop mostly normal to the y-axis.

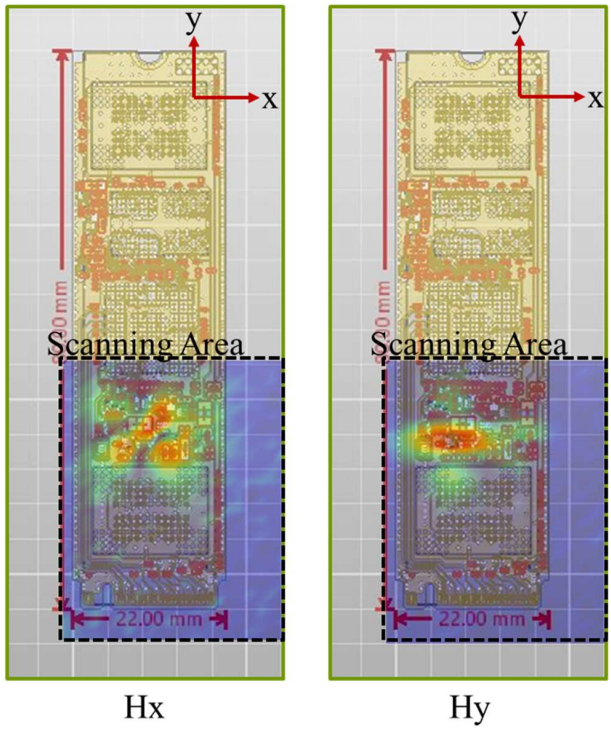

Fig. 4. Measured near field scanning results at 300 MHz.

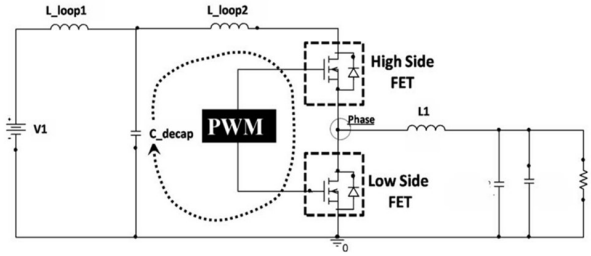

Fig. 5. Schematic of a buck converter and noise path.

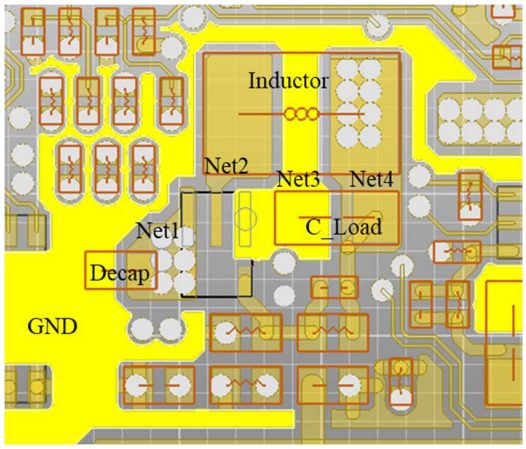

Fig. 6. The buck converter layout.

A. Noise Path Analysis

The buck converter layout of the DUT is shown in Fig. 6. The Net1~ Net4 are 3.3 V input, switching node, ground net, and 0.8 V output net, respectively. A 4.7 µF decoupling capacitor is mounted on the input node. The board is a six-layer printed circuit board (PCB), with the top and bottom layers as signal layers. The second and fifth layers are the ground layers and the third and fourth layers are the power layers. The HS FET, LS FET including the controller are integrated in the power management integrated circuit (PMIC). But based on the topology of the buck converter, the HS FET is between Net1 and Net2. And LS FET is between Net2 and Net3.

The phase voltage loop in the DUT is formed from the input net to the ground net on the right, then to the second ground layer through via 2, then to the left side of the decoupling capacitor through via1, and finally return to the input net across the decoupling capacitor. This HS FET → LS FET → decoupling capacitor current path is shown in Fig. 7. The solid arrow represents the current on the top layer and the dash arrow represents the current on the second ground layer. This vertical noise loop is normal to y-axis. The H-fields generated by the anticipated current loop will be validated in the next section.

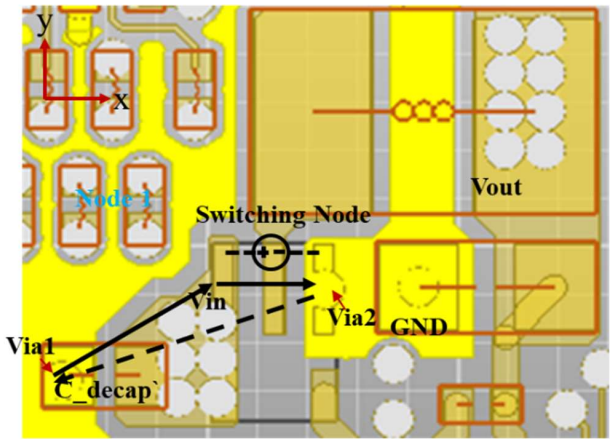

Fig. 7. Illustration of the noise current path.

B. Noise Voltage Measurement

For the full wave simulations, besides of the noise loop, the magnitude of the noise source also needs to be known. In this regard, the substitution theorem is used [16] - an element in a network can be replaced by a voltage source (or a current source) if the voltage and current in the rest of the circuit are kept the same. The voltage should be measured across the component and there is no need to consider source impedance. In the buck converter circuit, the elements between Net1 and Net3 can be substituted by a voltage source. Based on the substitution theorem, the anticipated current loop is reproduced in the full wave simulation with a voltage source as shown in Fig. 7.

The voltage between Net1 to Net3 was measured using an active differential probe. The probe bandwidth is 5 GHz, which is sufficient for the interested frequency range. Fig. 8. shows the measured waveform with the DC offset removed. The period of the noise is around 0.5 µs. The corresponding fundamental frequency is 2 MHz, which is the switching frequency of the buck converter.

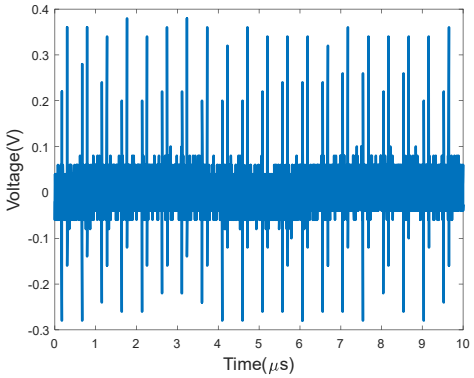

Fig. 8. Measured switching noise waveform between Net1 and Net3.

IV. Validation

To validate the anticipated current loop and the radiation mechanism, the simulated H-fields are compared to the measurement H-fields. Since we focus on the ringing on the phase voltage loop, only the components around the current path are necessary to be included in the simulation model. The simulated model is shown in Fig. 9. The vias and nets information were directly gotten from the printed circuit board (PCB) documents. The decoupling capacitor and PMIC were the only two components on the current path. Because the real structure inside of the capacitor and PMIC won't influence the noise current path, for the sake of simplification, a 4.7 µF edge umped element was used to replace the decoupling capacitor. The equivalent series inductance (ESL) and equivalent series resistance (ESR) were neglected. A voltage source was assigned between the input net of the PMIC and the ground net of the PMIC. And the excitation waveform was self-defined to the measured noise waveform.

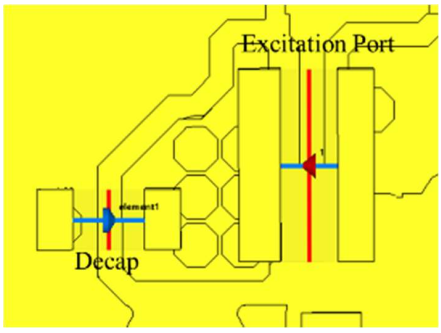

Fig. 9. Illustration of the simulation model and source excitation.

Fig. 10 shows the simulated H-fields at 2.1 mm above the top surface of the PCB, which is the same observation height in the near field measurement. The simulation results show a good match in terms of both pattern and magnitude. For better quantitative comparison, we reconstructed the equivalent dipole moment from both simulated and measured H-fields, respectively, based on the least square method (LSQ) [17]. The comparison of the reconstructed dipole moment is shown in Fig.

11. The max error from 200 MHz to 1100 MHz is 5 dB, and the average error is 1.91 dB.

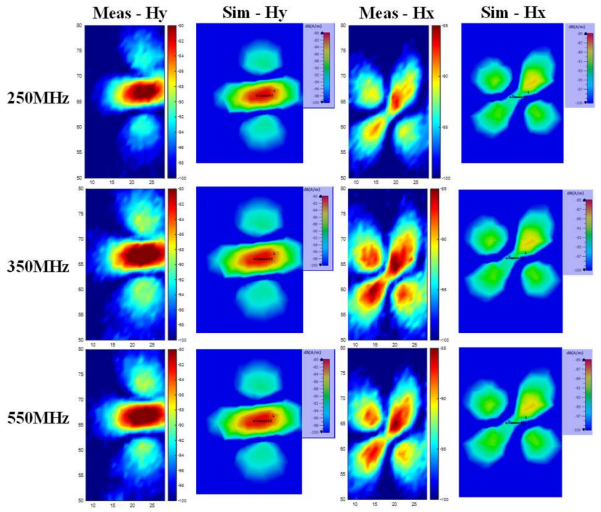

Fig. 10. Measured & simulated H-fields.

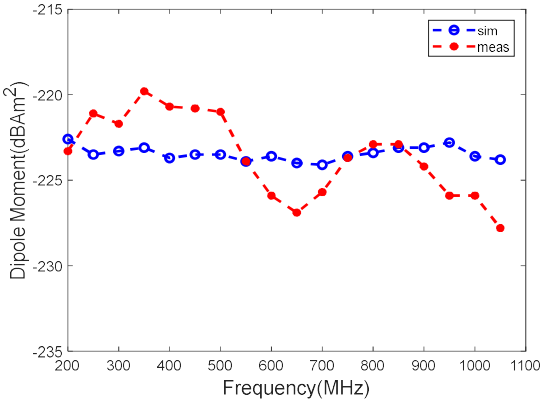

Fig. 11. Comparison of the equivalent dipole magnitude reconstructed from the measured and simulated H-fields.

V. Layout Optimization to Reduce EMI

Based on the understanding on the noise current loop, the electromagnetic emission can be reduced by minimizing the current loop size or changing the loop orientation - an M_z dipole on a ground plane does not radiate effectively. The proposed layout change is shown in Fig. 12. In the proposed layout, the PMIC and decoupling capacitor are in parallel. The new noise current path is as follows: input net → PMIC → ground net → decoupling capacitor → input net. The loop is now normal to the z-direction. The whole current loop is on the top layer of the board and the second layer is a perfect large ground plane. Thus, it behaves as an M_z dipole above a ground plane and does not radiate effectively.

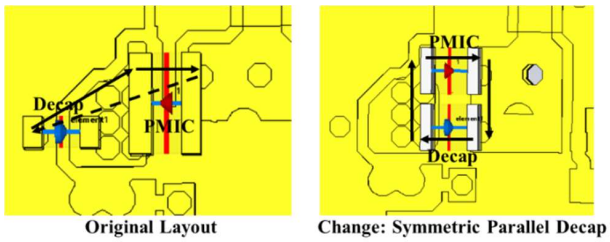

Fig. 12. Illustration of the original layout and optimized layout.

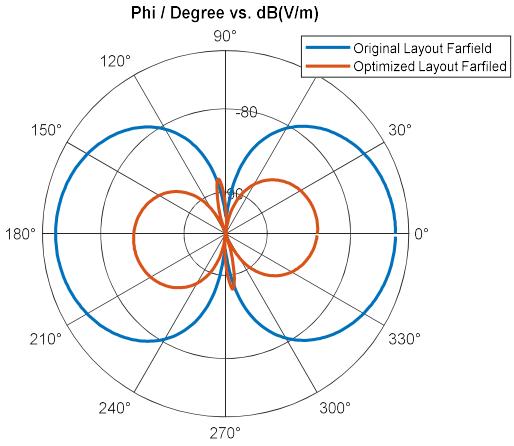

Fig. 13. Comparison of the simulated radiation patterns of the original and optimized layout.

Both original and revised models were excited with the same voltage source across the PMIC. The electric fields at 1 meter away along maximum radiation direction (theta angle = 90 degrees) is shown in Fig. 13. The proposed layout showed 10 dB lower radiation than the original case. The improvement is limited due to the interaction between the two components. In the cancellation concept, the current flowing through each component is independent of each other, but it was found that the two components are close enough and the displacement currents start to kick limiting the further improvement.

VI. Conclusion

This paper introduces a systematic way to map the near field patterns to the potential root cause in the DUT. An SSD, as an example, is investigated and the anticipated noise path in the buck converter is proposed and validated by full-wave simulations. The difference between the measured and simulated H-fields is less than 5 dB in the whole frequency range from 200 MHz to 1.1 GHz. Based on the understanding of the EMI root cause, an optimized buck converter layout is proposed, which reduces the far field radiation by 10 dB compared to the original layout.

References

[1] Q. Huang, Y. Liu, L. Li, Y. Wang, C. Wu and J. Fan, "Radio frequency interference estimation using transfer function based dipole moment model," *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, Singapore, 2018, pp. 115-120.

[2] D. -H. Han, H. -H. Hsu, J. Chen, M. Schaffer, C. M. Cheung and P. Davuluri, "PC client platform RFI risks and mitigation

methodologies," *2015 IEEE Symposium on Electromagnetic Compatibility and Signal Integrity*, 2015, pp. 85-90.

[3] M. Joodaki and A. Attar, "A radiated EMI measurement setup for un-buffered DRAM PCBs," *2014 International Symposium on Electromagnetic Compatibility*, 2014, pp. 756-759.

[4] Y. Sun, H. Lin, B. Tseng, D. Pommerenke, and C. Hwang, "Mechanism and Validation of USB 3.0 Connector Caused Radio Frequency Interference" *IEEE Trans. on Electromagnetic Compatibility*, vol. 62. no.4, pp.1169-1178, Aug. 2020.

[5] Huang, Qiaolei, et al. "Reciprocity theorem based RFI estimation for heatsink emission." *2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+ SIPI)*. IEEE, 2019.

[6] X. Yan et al., "EMI Investigation and Mitigation of Flexible Flat Cables and Connectors," *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, 2021, pp. 515-519.

[7] Y. Zhong *et al*., "Measurement-Based Quantification of Buzz Noise in Wireless Devices," *2019 Joint International Symposium on Electromagnetic Compatibility, Sapporo and Asia-Pacific International Symposium on Electromagnetic Compatibility (EMC Sapporo/APEMC)*, 2019, pp. 552-555.

[8] J. Joo *et al*., "Modeling of RF Interference Caused by Solid-State Drive Noise," *2022 Asia-Pacific International Symposium on Electromagnetic Compatibility (APEMC)*, 2022, pp. 685-687.

[9] H. -N. Lin, C. -C. Lu, H. -Y. Tsai and T. -W. Kung, "The analysis of EMI noise coupling mechanism for GPS reception performance degradation from SSD/USB module," *2014 International Symposium on Electromagnetic Compatibility, Tokyo*, 2014, pp. 350-353.

[10] Z. Sun, Y. Wang, W. Lee, K. Wu and D. Kim, "Radiated Noise Source Characterization Based on Magnitude-Only Near Field," *2021 IEEE International Joint EMC/SI/PI and EMC Europe Symposium*, 2021, pp. 376-380.

[11] C. Wu, Z. Sun, Q. Huang, Y. Wang, J. Fan and J. Zhou, "A Method to Extract Physical Dipoles for Radiating Source Characterization and Near Field Coupling Estimation," *2019 IEEE International Symposium on Electromagnetic Compatibility, Signal & Power Integrity (EMC+SIPI)*, 2019, pp. 580-583.

[12] Y. Liu, J. Li, C. Hwang and V. Khilkevich, "Near-Field Scan of Multiple Noncorrelated Sources Using Blind Source Separation," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 62, no. 4, pp. 1376-1385, Aug. 2020.

[13] J. Zhang, K. W. Kam, J. Min, V. V. Khilkevich, D. Pommerenke and J. Fan, "An Effective Method of Probe Calibration in Phase-Resolved Near-Field Scanning for EMI Application," in *IEEE Transactions on Instrumentation and Measurement*, vol. 62, no. 3, pp. 648-658, March 2013.

[14] A. Bhargava, D. Pommerenke, K. W. Kam, F. Centola and C. W. Lam, "DC-DC Buck Converter EMI Reduction Using PCB Layout Modification," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 53, no. 3, pp. 806-813, Aug. 2011.

[15] A. Bhargava *et al*., "EMI prediction in switched power supplies by full-wave and non-linear circuit co-simulation," *2009 IEEE International Symposium on Electromagnetic Compatibility*, 2009, pp. 41-46.

[16] J. Yao, S. Wang and Z. Luo, "Modeling, Analysis, and Reduction of Radiated EMI Due to the Voltage Across Input and Output Cables in an Automotive Non-Isolated Power Converter," in *IEEE Transactions on Power Electronics*, vol. 37, no. 5, pp. 5455-5465, May 2022.

[17] Z. Yu, J. A. Mix, S. Sajuyigbe, K. P. Slattery and J. Fan, "An Improved Dipole-Moment Model Based on Near-Field Scanning for Characterizing Near-Field Coupling and Far-Field Radiation From an IC," in *IEEE Transactions on Electromagnetic Compatibility*, vol. 55, no. 1, pp. 97-108, Feb. 2013.