

# Interfacial Layer Engineering in Sub-5-nm HZO: Enabling Low-Temperature Process, Low-Voltage Operation, and High Robustness

Eunseon Yu<sup>1</sup>, Xiao Lyu, Mengwei Si<sup>1</sup>, *Member, IEEE*, Peide D. Ye<sup>1</sup>, and Kaushik Roy<sup>1</sup>, *Fellow, IEEE*

**Abstract**—For low-voltage reliable operation of ferroelectric devices, the scaling of  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  (HZO) thickness ( $t_{\text{HZO}}$ ) is important. Despite the importance of scaling, ferroelectricity degradation and increased process thermal budget hinder progress. In this work, we propose the use of an interfacial layer (IL) to mitigate these scaling issues and validate its effectiveness in thin  $t_{\text{HZO}}$ . Our findings demonstrate that IL can activate ferroelectricity below the critical temperature of ferroelectric HZO. Moreover, we report  $2\times$  polarization improvement, reduced operation voltage from 1.5 to 1.2 V, and substantially improved endurance with  $>10$  years of reliability, all based on experimental results. We believe this systematic work offers a simple yet efficient route toward HZO scaling in ferroelectric devices.

**Index Terms**—Back-end-of-the-line (BEOL) compatible process, ferroelectricity improvement,  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  thickness ( $t_{\text{HZO}}$ ) scaling, HZO reliability, interfacial layer (IL) engineering, operation voltage scaling.

## I. INTRODUCTION

THE standard CMOS technology, with transistors as efficient switches, has been the workhorse of today's high-performance systems. However, with the evolving computing workloads and the demand for ubiquitous intelligence, high energy efficiency has come to the forefront. To meet this challenge, the need to rethink the entire computing stack has

become apparent. To achieve this goal, there is a need to incorporate more functionalities into a single device, beyond what a CMOS transistor can provide. In light of this, we consider ferroelectric devices, which offer energy-efficient building blocks for boosting performance on challenging workloads [1], [2], [3], [4], [5], [6].

Recent research on ferroelectric devices has focused on scaling the thickness ( $t_{\text{HZO}}$ ) of  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  (HZO) [7], [8], [9], [10], [11], [12]. Achieving lower operation voltage as well as more robustness is the largest gain of scaled  $t_{\text{HZO}}$ . However, scaling  $t_{\text{HZO}}$  is hindered by increased process temperature and degraded ferroelectricity because of the increased amorphous structure of HZO [9], [13]. It has been reported that an annealing temperature higher than 450 °C is required to secure sufficient ferroelectricity when  $t_{\text{HZO}}$  is reduced below 5.6 nm [9] and 4.8 nm [10]. However, that is not favorable for back-end-of-the-line (BEOL) process which has a thermal budget limit of 400 °C [14]. Two different approaches have been tried to improve ferroelectricity in scaled HZO structures. In [11], different top-electrode (TE) and bottom-electrode (BE) combinations were investigated to minimize the depolarization field. Depending on the electrode materials, the formation of nonferroelectric layers (i.e., dead layers) at the ferroelectric/metal interface changes. Although high remnant polarization ( $P_r$ ) was obtained at  $T_{\text{PMA}} = 400$  °C, the negative coercive field ( $E_c$ ) increasing to  $\sim -1.75$  MV/cm at  $t_{\text{HZO}}$  of 5 nm or less offsets the advantages of scaling  $t_{\text{HZO}}$ . Additionally, there is a lack of reliability studies in electrode material design. Another approach adopted is the HZO epitaxy high-quality HZO can be obtained. Results show a high  $P_r$  even at  $t_{\text{HZO}} = 4.5$  nm [12]. However, it requires a high temperature of 800 °C for the HZO epitaxy process. Considering ferroelectric devices are mostly to be fabricated in BEOL, such a high process temperature is not a feasible solution. This work proposes an approach to improving  $P_r$  and securing low operation voltage even at  $T_{\text{PMA}}$  below 400 °C.

Previous research has investigated using an interfacial layer (IL) to increase the ferroelectric properties of thicker HZO films (around 10 nm). Table I provides information on the IL materials and annealing processes used in these studies. The IL enhances ferroelectricity by increasing

Manuscript received 12 November 2022; revised 3 February 2023, 11 March 2023, and 12 April 2023; accepted 20 April 2023. Date of publication 10 May 2023; date of current version 25 May 2023. The work of Peide D. Ye was supported in part by the Semiconductor Research Corporation (SRC)/Defense Advanced Research Projects Agency (DARPA) the Joint University Microelectronics Program (JUMP) ASCENT Center and in part by the Air Force Office of Scientific Research (AFOSR). The work of Kaushik Roy was supported in part by the Center for Brain-Inspired Computing (C-BRIC), in part by the SRC/DARPA JUMP Center, in part by the National Science Foundation (NSF), and in part by the Intelligence Advanced Research Projects Activity (IARPA) Microelectronics for Artificial Intelligence (MicroE4AI) Program. The review of this article was arranged by Editor F. Schwierz. (Corresponding author: Eunseon Yu.)

Eunseon Yu, Xiao Lyu, Peide D. Ye, and Kaushik Roy are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA (e-mail: yu966@purdue.edu).

Mengwei Si is with the Department of Electronic Engineering, Shanghai Jiao Tong University, Shanghai 200240, China.

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TED.2023.3270397>.

Digital Object Identifier 10.1109/TED.2023.3270397

**TABLE I**  
SUMMARY OF MATERIALS AND PROCESS INFORMATION  
OF THE PREVIOUS IL RELATED WORK

| IL Material                    | Ref. | $t_{\text{HZO}}$ | $t_{\text{IL}}$ | Annealing Conditions |         |
|--------------------------------|------|------------------|-----------------|----------------------|---------|
|                                |      |                  |                 | Temperature          | Time    |
| HfON                           | [15] | 8~25 nm          | 2~200 nm        | 500°C                | 30 sec  |
|                                | [16] | 10 nm            | 1~20 nm         | 600°C                | 10 sec  |
| HfO <sub>2</sub>               | [17] | 10 nm            | 1 nm            | 300~400°C            | 60 sec  |
|                                | [18] | 10 nm            | 1 nm            | 350°C                | 60 sec  |
|                                | [19] | 15 nm            | 3 nm            | 450°C                | 30 sec  |
| TiO <sub>2</sub>               | [17] | 10 nm            | 1 nm            | 300~400°C            | 60 sec  |
|                                | [20] | 10 nm            | 2~3 nm          | 500°C                | 300 sec |
|                                | [21] | 10 nm            | 0~5 nm          | 400°C                | -       |
| SiN <sub>x</sub>               | [22] | 4.5 nm           | 1.5 nm (850°C)  | 500°C                | 30 sec  |
|                                | [17] | 10 nm            | 1 nm            | 300~400°C            | 60 sec  |
|                                | [23] | 10 nm            | 0.5~5.0 nm      | 600°C                | 60 sec  |
| ZrO <sub>2</sub>               | [24] | 10 nm            | 2 nm            | 400~700°C            | 60 sec  |
|                                | [25] | 9.5 nm           | 2 nm            | 900°C                | 60 sec  |
|                                | [26] | 10 and 25 nm     | 1~2 nm          | 550°C                | 60 sec  |
|                                | [27] | 12 nm            | 1.5 nm          | 550°C                | Unknown |
|                                | [28] | 10 nm            | 2 nm            | 500~800°C            | 30 sec  |
|                                | [29] | 10 nm            | 2 and 10 nm     | 300~600°C            | 60 sec  |
|                                | [33] | 9.5 nm           | 1.2 nm          | 800°C                | Unknown |
| AlON                           | [23] | 10 nm            | 2 nm            | 600°C                | 60 sec  |
|                                | [25] | 9.5 nm           | 2 nm            | 900°C                | 60 sec  |
|                                | [33] | 9.5 nm           | 1.2 nm          | 800°C                | Unknown |
| Al <sub>2</sub> O <sub>3</sub> | [34] | 10 nm            | 0.5~3 nm        | 600~900°C            | Unknown |
|                                | [35] | 10~40 nm         | 1 nm            | 500°C                | 30 sec  |
|                                | [36] | 7 nm             | ~1 nm           | 450~600°C            | 30 sec  |
| Ta <sub>2</sub> O <sub>5</sub> | [37] | 10 nm            | 1~5 nm          | 600°C                | Unknown |

the ferroelectric orthorhombic-phase (*o*-phase) content of the HZO film. One reason for this is claimed as using polycrystalline nature of as-deposited IL, such as ZrO<sub>2</sub> [17], [23], [24], [25], [26], [27], [28], [29], [30]. X-ray diffraction (XRD) data of the ZrO<sub>2</sub> layer before the annealing process was provided to support the claim. Here, the analyzed ZrO<sub>2</sub> layers were 14 nm [23] and 10 nm [29]. However, thicker ZrO<sub>2</sub> (>6 nm) is known to have polycrystallinity during atomic layer deposition (ALD) [31], [32], while the ILs used in the studies listed in Table I were mostly 1–2 nm, and thus too thin to be polycrystalline. Our position on this will be discussed in detail in the last few paragraphs of Section II. The other reason for enhanced ferroelectricity with IL is the large stress introduced onto the HZO layer, which increases *o*-phase fraction [13], [38]. These benefits of using IL naturally motivated us to invoke the idea of adopting it for  $t_{\text{HZO}}$  scaling.

We propose a simple but effective approach, harnessing an ultrathin IL to alleviate challenges associated with scaling  $t_{\text{HZO}}$ . Specifically, we investigate the effect of IL materials in sub-5-nm HZO films, covering various perspectives, such as crystallization temperature, ferroelectricity, low-voltage operation capability, and reliability characteristics. Our findings demonstrate that incorporating an IL can induce a higher *o*-phase content in the HZO layer, reduced operation voltage, improved ferroelectricity, and enhanced retention performance.

**TABLE II**  
DEVICE STRUCTURAL AND PROCESS TEMPERATURE CONDITIONS

| $t_{\text{HZO}}$ | 1-nm IL (BE side)              | $T_{\text{PMA}}$ (Time: 60 sec) |
|------------------|--------------------------------|---------------------------------|
| 4.5 nm           | Without IL                     | 300, 350, 400, and 500°C        |
|                  | HfO <sub>2</sub>               |                                 |
|                  | ZrO <sub>2</sub>               |                                 |
| 9.5 nm           | Without IL                     | 300, 350, 400, and 500°C        |
|                  | HfO <sub>2</sub>               |                                 |
|                  | ZrO <sub>2</sub>               |                                 |
|                  | Al <sub>2</sub> O <sub>3</sub> |                                 |

Importantly, we observe that the use of an IL can reduce the critical temperature of HZO crystallization. This finding supports the use of IL for scaling  $t_{\text{HZO}}$ .

## II. DEVICE FABRICATION AND ITS FERROELECTRICITY

In this work, ferroelectric capacitors were fabricated to understand the behaviors of the different ferroelectric stacks. A 10-nm-thick TiN BE, an IL, an HZO layer, and a 10-nm-thick TiN TE were deposited subsequently using thermal ALD at 200 °C on the  $p^+$ -type Si substrate. Table II contains information about the device structures and annealing conditions that were employed. Note, a 1-nm IL was intentionally deposited between the BE and HZO layer, followed by in situ deposition of 4.5- or 9.5-nm HZO layers, which improves ferroelectricity and endurance [43]. Previous studies have shown that the optimum IL thicknesses to improve  $P_r$  with HfO<sub>2</sub> [16], ZrO<sub>2</sub> [23], and Al<sub>2</sub>O<sub>3</sub> [34] ILs are 1, 2, and 0.5 nm, respectively. In this work, we aimed to investigate the effects of IL over the HZO layer while keeping the thickness as thin as possible but within a reliable and controllable range. Therefore, we chose a 1 nm of IL thickness to encompass the optimum thicknesses of each IL material. Rapid-thermal annealing (RTA) as a post-metal annealing (PMA) was performed after the TE deposition. Al deposition and lift-off were conducted for capacitor patterning (area: 3600  $\mu\text{m}^2$ ). Note, we additionally attempted PMA annealing at  $T_{\text{PMA}} = 275$  and 300 °C for 60 s and 2 h, but none of the devices showed ferroelectricity.

The electric field ( $E$ ) is a key metric used to compare the performance of different structures. It is calculated by dividing the applied voltage ( $V_{\text{apply}}$ ) by the total dielectric thickness (averaged  $E$ ). However, the actual electric field applied to the ferroelectric layer can vary due to factors such as the permittivity of the IL, the quality of the metal-dielectric interface, and the quality of the HZO layer. Even though we do not plot the measurement result with the actual electric field on HZO, we calculated the voltage drop across the HZO ( $V_{\text{HZO}}$ ) by extracting the dielectric constant, charge density, total capacitance, and interfacial capacitance. We then expressed  $V_{\text{HZO}}$  as a percentage of  $V_{\text{apply}}$  ( $=V_{\text{HZO}}/V_{\text{apply}} \times 100$ ). Overall, higher  $T_{\text{PMA}}$  and the use of an IL increase the percentage of  $V_{\text{HZO}}$ . However, the differences in the percentage of  $V_{\text{HZO}}$  between cases with IL and without IL become more significant at thinner  $t_{\text{HZO}}$ . Among the different ILs, ZrO<sub>2</sub> IL shows the highest percentage of  $V_{\text{HZO}}$ , due to its high permittivity and improved interface and HZO quality.

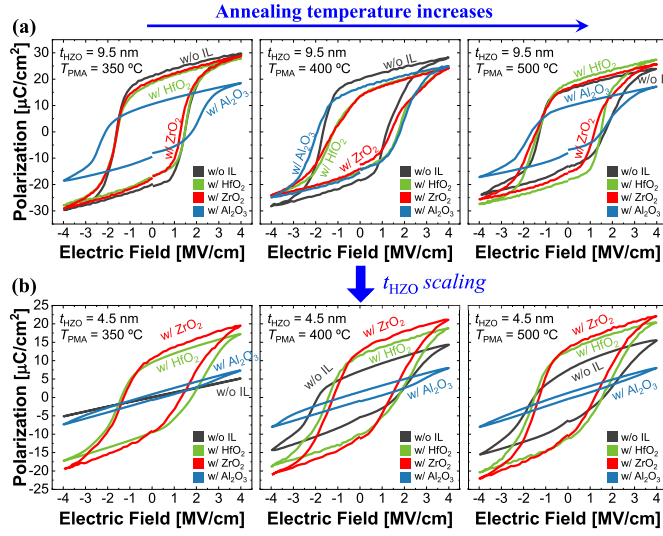


Fig. 1.  $P$ - $E$  loops of the devices having (a) 9.5- and (b) 4.5-nm  $t_{\text{HZO}}$ .

Importantly, at 4.5-nm  $t_{\text{HZO}}$  and low  $T_{\text{PMA}}$ ,  $\text{ZrO}_2$  IL indicates 70.5% and 81.4% of  $V_{\text{app}}$  dropped on HZO at 350 °C and 400 °C  $T_{\text{PMA}}$ , respectively (56.0% and 65.7% for  $\text{HfO}_2$  IL, and 50.3% and 69.8% for  $\text{Al}_2\text{O}_3$  IL, respectively).

Fig. 1(a) and (b) depict the measured polarization ( $P$ )-electric field ( $E$ ) loops for 9.5- and 4.5-nm  $t_{\text{HZO}}$  films annealed at  $T_{\text{PMA}}$  of 350 °C, 400 °C, and 500 °C, respectively. The period taken in  $P$ - $E$  measurement was fixed to 1 kHz. Wake-up pulses of 5000 cycles with  $\pm 4$  MV/cm amplitude were applied before all measurements. The  $2P_r$  ( $=P_r^+ - P_r^-$ ) and the  $E_c$  [ $=0.5 \cdot (E_c^+ - E_c^-)$ ] extracted from Fig. 1 are plotted in Fig. 2(a) and (b), respectively. For  $t_{\text{HZO}} = 9.5$  nm, using an IL did not improve  $2P_r$  for the 350 °C and 400 °C annealed cases. However, for scaled  $t_{\text{HZO}}$ , using an IL plays a significant role not only in boosting  $P_r$ , but also in reducing  $E_c$  (see Fig. 2). Importantly, the IL decreases the critical temperature for HZO crystallization at scaled  $t_{\text{HZO}}$ . With  $\text{HfO}_2$  and  $\text{ZrO}_2$  ILs, 350 °C for  $T_{\text{PMA}}$  is sufficient to activate ferroelectricity, whereas the device without an IL exhibits no ferroelectricity. At  $T_{\text{PMA}} = 400$  °C, 1.7 $\times$  and 1.9 $\times$  of  $P_r$  improvements are obtained with  $\text{HfO}_2$  and  $\text{ZrO}_2$  ILs, respectively, compared to devices without an IL. The usage of  $\text{HfO}_2$  and  $\text{ZrO}_2$  IL also improves  $2P_r$  compared to HZO without an IL at the same voltage condition. At scaled  $t_{\text{HZO}}$ , the  $\text{Al}_2\text{O}_3$  IL is not helpful at all in improving ferroelectricity. The devices with  $E_c$  values of 9.5-nm  $t_{\text{HZO}}$  without IL, with  $\text{HfO}_2$  IL, and with  $\text{ZrO}_2$  IL, exhibit similar behavior. However, the insertion of  $\text{Al}_2\text{O}_3$  IL results in a high  $E_c$  at 9.5-nm  $t_{\text{HZO}}$  due to its low dielectric constant and a small  $E_c$  at 4.5-nm  $t_{\text{HZO}}$  due to weak ferroelectricity.  $\text{ZrO}_2$  IL provides the most consistent  $E_c$  values across different  $t_{\text{HZO}}$  and  $T_{\text{PMA}}$  conditions. The relationship between  $E_c$  and low-voltage operation capability is discussed in Section III.

Transmission electron microscopy (TEM) images of the devices without IL and with  $\text{ZrO}_2$  IL ( $T_{\text{PMA}} = 350$  °C) are shown in Fig. 3(a) and (b), respectively. The HZO layer has an amorphous structure without IL. However, the HZO layer becomes crystallized with 1-nm  $\text{ZrO}_2$  IL at the same  $t_{\text{HZO}}$ . It is

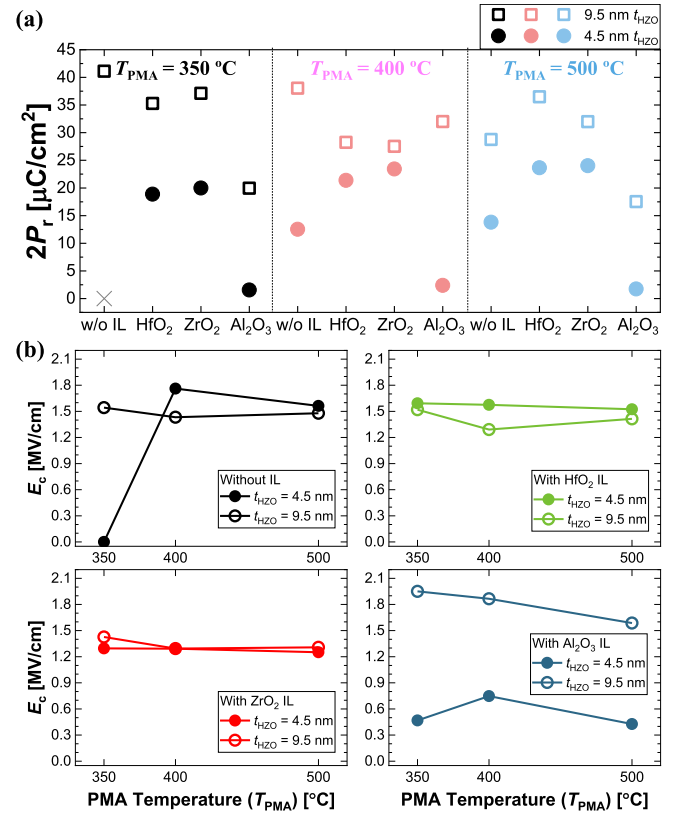


Fig. 2. Extracted figure-of-merits for 9.5- and 4.5-nm  $t_{\text{HZO}}$  devices. (a)  $2P_r$  and (b)  $E_c$  plots.

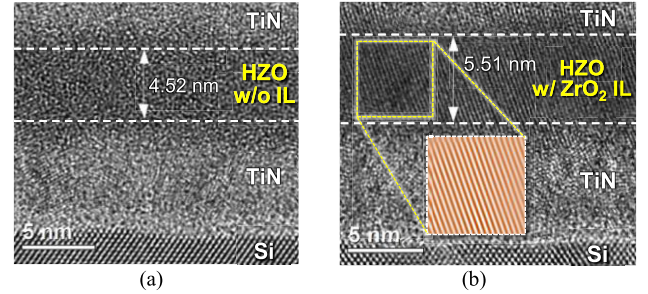


Fig. 3. TEM images for 4.5-nm  $t_{\text{HZO}}$  devices (a) without IL and (b) with 1-nm  $\text{ZrO}_2$  IL.  $T_{\text{PMA}}$  was 350 °C for both.

worth noting that the  $\text{ZrO}_2$  IL might not be intermixed into the HZO layer during or after the PMA process, but rather secured as a bilayer structure. Previous works have demonstrated the maintained bilayer of the 10-nm HZO/2-nm  $\text{ZrO}_2$  IL structure even after annealing at 400 °C–700 °C for 60 s [24], [26]. Since our  $T_{\text{PMA}}$  conditions are between 300 °C and 500 °C, the deposited IL would be preserved after the PMA process. Therefore, our device dielectric stacks cannot be considered as having 5.5-nm  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  ( $x > 0.5$ ) without IL.

The use of an IL has resulted in improved crystallinity and higher  $o$ -phase content in the HZO layer, which in turn has led to an increase in  $P_r$ . To figure out the cause of this improvement, we conducted grazing incidence XRD (GI-XRD) analysis and capacitance measurement. The GI-XRD data for the 400 °C annealed devices is presented in Fig. 4(a). The X-ray intensity contains signals from multiple phases due to XRD

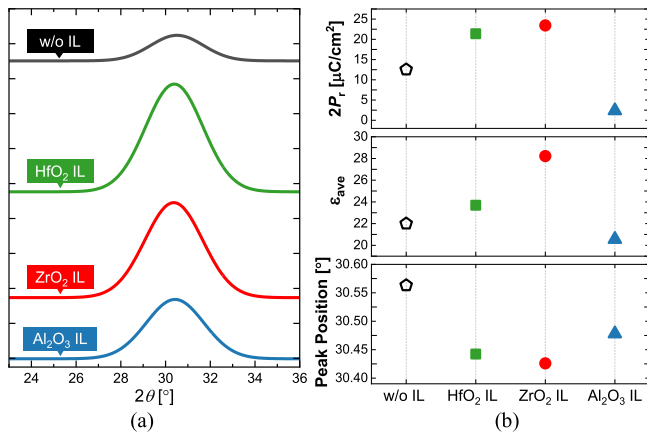


Fig. 4. Devices at  $T_{\text{PMA}} = 400^\circ\text{C}$  with 4.5-nm  $t_{\text{HZO}}$ . (a) GI-XRD data and (b)  $2P_r$ ,  $\epsilon_{\text{ave}}$ , and peak position of  $2\theta$  from GI-XRD results.

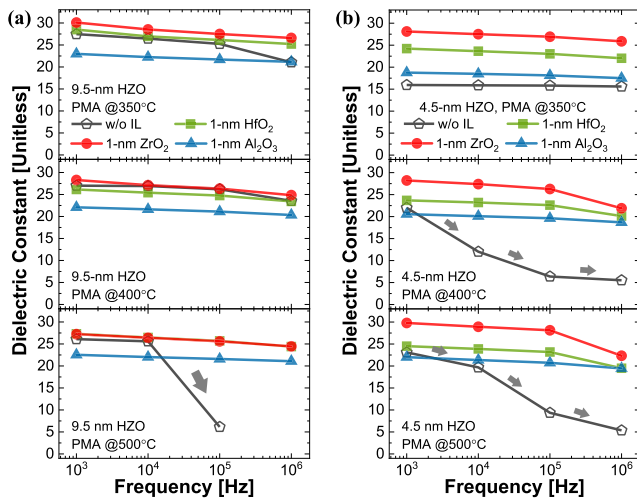


Fig. 5. Average dielectric constant ( $\epsilon_{\text{ave}}$ ) calculated from the  $C$ - $E$  measurement ( $\epsilon_{\text{ave}} = C/\text{Area} \times (t_{\text{HZO}} + t_{\text{IL}})$ ) of (a)  $t_{\text{HZO}} = 9.5$  nm and (b)  $t_{\text{HZO}} = 4.5$  nm devices.

peak broadening. We estimated the phase concentration based on the position of the intensity peak. The significant degrees of the HZO phases are  $28.5^\circ$  ( $m(-111)$ ),  $30.4^\circ$  ( $o(111)$ ),  $30.8^\circ$  ( $t(011)$ ), and  $31.6^\circ$  ( $m(111)$ ). Fig. 4(b) indicates  $2P_r$ , the average dielectric constant ( $\epsilon_{\text{ave}}$ ), and XRD peak position for the  $400^\circ\text{C}$  annealed devices with 4.5-nm  $t_{\text{HZO}}$ . The HZO without IL exhibits the smallest X-ray signal and the peak is located far from  $30.4^\circ$  ( $o(111)$ ), indicating low phase concentration. In contrast, the devices with HfO<sub>2</sub> and ZrO<sub>2</sub> IL show strong intensities with peaks located close to  $30.4^\circ$ , representing a high ferroelectric  $o$ -phase concentration. Additionally,  $>10 \mu\text{C}/\text{cm}^2$  of  $2P_r$  is obtained with HfO<sub>2</sub> and ZrO<sub>2</sub> IL, indicating the introduction and stabilization of high  $o$ -phase concentration in thin HZO. The HZO with Al<sub>2</sub>O<sub>3</sub> IL also exhibits a comparable X-ray intensity with HfO<sub>2</sub> and ZrO<sub>2</sub> IL, but has almost zero  $2P_r$ , indicating large nonferroelectric phases on HZO.

Capacitance ( $C$ )- $E$  measurement was performed for all devices at different frequencies ( $f$ ) of 1 kHz, 10 kHz, 100 kHz, and 1 MHz. Fig. 5(a) and (b) show calculated  $\epsilon_{\text{ave}}$  from  $C$ - $E$  measurement, which were extracted at the cross point of the butterfly curves in forward- and reverse-direction

sweeps. Here,  $RC$  delay was observed, which suggests that the evaluated  $\epsilon_{\text{ave}}$  may be lower than the actual value. However, the observed trends between devices and our conclusions would not be affected. The dielectric constants of the  $o$ - and tetragonal ( $t$ )-phase are known to be  $\sim 30$  and  $32$ – $40$ , respectively [40]. The  $\epsilon_{\text{ave}}$  of amorphous HZO is 16 (the value is from the 4.5-nm  $t_{\text{HZO}}$  without IL at  $350^\circ\text{C}$   $T_{\text{PMA}}$ ). When both  $\epsilon_{\text{ave}}$  and  $2P_r$  are considered, it can be assumed that the devices with the  $\epsilon_{\text{ave}}$  of  $\sim 16$  and weak ferroelectricity contain a significant portion of amorphous or nonferroelectric phases in HZO. This finding is consistent with the cases of Al<sub>2</sub>O<sub>3</sub> IL. Thereby, the introduction of Al<sub>2</sub>O<sub>3</sub> is believed to create phases in HZO, as indicated by the intensity in GI-XRD data, but most cannot stabilize to  $o$ -phase.

In the following paragraphs, we will discuss the factors contributing to improved ferroelectricity and reduced crystallization temperature of ferroelectric HZO. Achieving a high  $o$ -phase concentration is significant for improving  $P_r$ . Additionally, surface energy plays a crucial role in stabilizing the crystalline phases in the thin HZO structure [41]. To transform nonferroelectric  $t$ -phase to ferroelectric  $o$ -phase, sufficient stress is required after amorphous HZO is converted to crystalline HZO in the  $t$ -phase [42]. The different coefficients of thermal expansion (CTEs) between HZO and abutting layers, as well as the lattice mismatch-induced strain, are the primary factors affecting the transformation of the dominant HZO crystalline phase from  $t$ - to  $o$ -phase.

During the annealing process, HfO<sub>2</sub>, ZrO<sub>2</sub>, and Al<sub>2</sub>O<sub>3</sub> can trigger the formation of  $t$ -phase in HZO due to their inherent material properties. HfO<sub>2</sub> and ZrO<sub>2</sub> have low surface energies owing to their thin thickness and small grain sizes [7], [43]. The thermodynamic model with Gibbs free energy can explain these properties [41]. A previous study reported that deposited Al<sub>2</sub>O<sub>3</sub> underneath HZO can effectively reduce grain size and hinder grain growth of HZO [35]. Therefore, all HfO<sub>2</sub>, ZrO<sub>2</sub>, and Al<sub>2</sub>O<sub>3</sub> IL can induce  $t$ -phase during the PMA process, as verified by our GI-XRD data in Fig. 4. The  $t$ -phase can later transform to  $o$ -phase via in-plane tensile stress that originates from the different CTEs of stacked materials [13], [38], and lattice mismatch strain induced by crystallized phases [20].

It is important to note that there are properties distinguishing HfO<sub>2</sub> and ZrO<sub>2</sub> IL from Al<sub>2</sub>O<sub>3</sub> IL. Both HfO<sub>2</sub> and ZrO<sub>2</sub> have similar crystallization temperatures [32], [44], crystal structures, and phase formation energies with HZO [45]. This suggests that HfO<sub>2</sub> and ZrO<sub>2</sub> IL can mutually affect HZO during the crystallization process, leading to their crystallization during annealing. This can be observed in the TEM image in Fig. 3(b), which shows a vertically grown HZO layer with no interface with the crystallized ZrO<sub>2</sub> IL. The resulting decrease in surface-to-volume-ratio (due to the increased volume of the crystallized layer) can lower the kinetic barrier for the transition from amorphous to crystalline and  $t$ - to  $o$ -phase transition [44], [46]. As a result, high  $o$ -phase concentrations are observed for both HfO<sub>2</sub> and ZrO<sub>2</sub> IL cases in our measurement data. However, Al<sub>2</sub>O<sub>3</sub> IL has a higher crystallization temperature ( $900^\circ\text{C}$ ) than HfO<sub>2</sub> and ZrO<sub>2</sub> IL, making it less effective in inducing  $o$ -phase in HZO under the given  $T_{\text{PMA}}$  conditions [47].

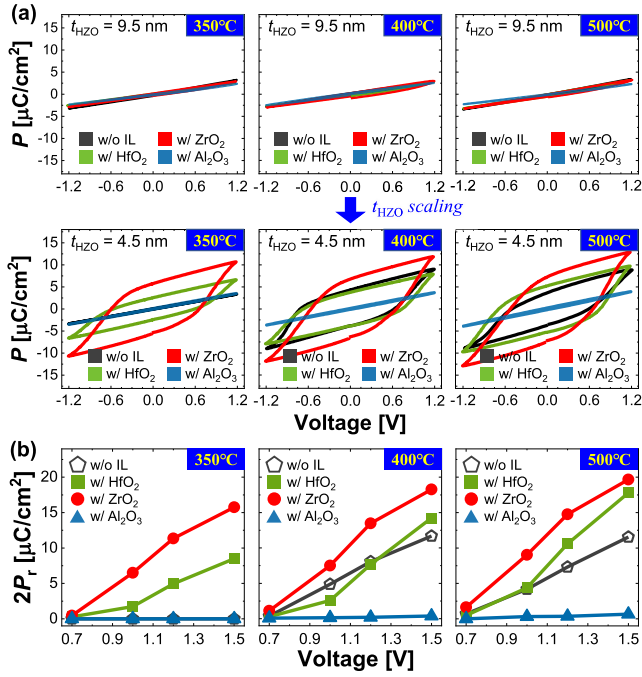


Fig. 6. Low-voltage operation characteristics. (a)  $P$ - $V$  loops when the voltage sweep range is fixed to  $\pm 1.2$  V at  $t_{\text{HZO}} = 9.5$  nm (upper) and  $4.5$  nm (lower). (b)  $2P_r$  versus operation voltage of  $4.5$ -nm HZO devices.

To lower the crystallization temperature of ferroelectric HZO, it is important to choose IL which has a low crystallization temperature and structural similarity to HZO. Furthermore, an IL with a low CTE can also help lower the crystallization temperature of HZO [48], [49], [50]. As previously reported, using a low CTE electrode generates stress in HZO during the crystallization [48], [49], [50]. The CTE values of TiN, HZO,  $\text{HfO}_2$ ,  $\text{ZrO}_2$ , and  $\text{Al}_2\text{O}_3$  are  $7$ – $9.4 \times 10^{-6} \text{ K}^{-1}$  [20], [51],  $5 \times 10^{-5} \text{ K}^{-1}$  [52],  $3.8 \times 10^{-6}$ ,  $7$ – $10.3 \times 10^{-6}$ , and  $8.1$ – $8.4 \times 10^{-6} \text{ K}^{-1}$  [20], [53], respectively. Compared to  $\text{ZrO}_2$  and  $\text{Al}_2\text{O}_3$ ,  $\text{HfO}_2$  has a large difference in CTE with HZO, which can induce greater stress in HZO. This enables  $\text{HfO}_2$  IL to have superior ferroelectric performance, despite its slightly higher crystallization temperature compared to  $\text{ZrO}_2$  or HZO [44].

### III. LOW-VOLTAGE OPERATION CAPABILITY

Along with dimension scaling, reducing operation voltage is important to decrease power consumption. Fig. 6(a) shows the  $P$ - $V$  loops of devices with  $9.5$ - and  $4.5$ -nm  $t_{\text{HZO}}$  at  $\pm 1.2$  V voltage sweep, and Fig. 6(b) shows the  $2P_r$  observed for the  $4.5$ -nm  $t_{\text{HZO}}$  devices at different operating voltages. At  $\pm 1.2$  V, the  $9.5$ -nm HZO samples do not exhibit  $2P_r$  above  $10 \mu\text{C}/\text{cm}^2$ . However, the  $4.5$ -nm HZO devices achieve high  $2P_r$  due to the relatively unchanged  $E_c$  ( $=$  coercive voltage ( $V_c$ ) divided by the  $t_{\text{HZO}}$ ) between  $9.5$  and  $4.5$  nm of  $t_{\text{HZO}}$  [see Fig. 2(b)]. With the usage of  $\text{ZrO}_2$  IL, HZO shows superior low-voltage operation performance, inducing a small  $E_c$  and the largest  $2P_r$  at scaled  $t_{\text{HZO}}$ . The required operation voltage for the  $\text{ZrO}_2$  IL case to obtain  $2P_r > 10 \mu\text{C}/\text{cm}^2$  is  $1.2$  V, which is  $0.3$  V lower than without IL. At  $1.2$ -V operation,  $P_r$  increases  $1.67$  times with  $\text{ZrO}_2$  IL ( $T_{\text{PMA}} = 400^\circ\text{C}$ )

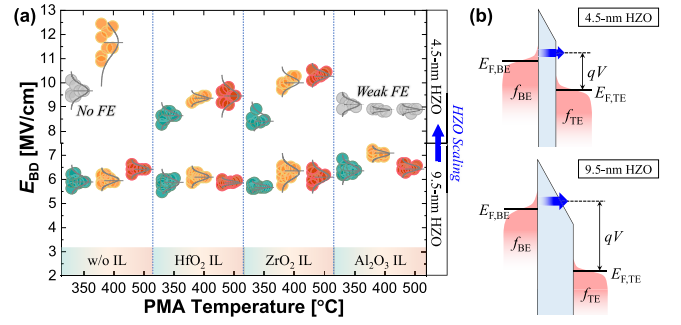


Fig. 7. Dielectric breakdown characteristics. (a)  $E_{\text{BD}}$  distribution plots. (b) Energy-band diagram when  $t_{\text{HZO}}$  is thin (upper) and thick (lower).

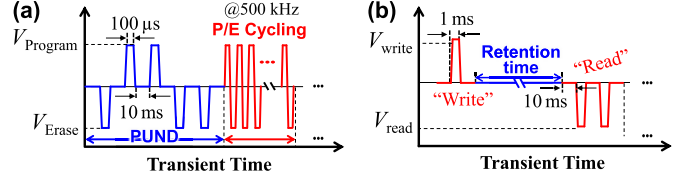


Fig. 8. Pulsing schemes for reliability test of (a) endurance and (b) retention.

compared to one without IL. For  $500^\circ\text{C}$  annealed devices,  $1.5$  and  $2.0$  times of  $2P_r$  improvement are observed by using  $\text{HfO}_2$  and  $\text{ZrO}_2$  IL, respectively. The improved low-voltage operation capability is confirmed based on our claim that the IL ( $\text{HfO}_2$  and  $\text{ZrO}_2$ ) promotes the large  $o$ -phase content onto the scaled HZO and enhances the quality of HZO and interfaces.

### IV. RELIABILITY CHARACTERISTICS

In previous sections, we have confirmed that the use of IL leads to increased  $P_r$ , lower operational voltage, and reduced process temperature. In this section, we will examine the impact of  $T_{\text{PMA}}$  and IL on various reliability performances of the device, including hard breakdown electric field ( $E_{\text{BD}}$ ), endurance, and retention. To investigate dielectric strength, a time-zero dielectric breakdown test was conducted. Fig. 7(a) displays the distribution of the  $E_{\text{BD}}$  and Fig. 7(b) shows the energy band diagram across TE-HZO-BE. In endurance and retention measurement, the positive-up-negative-down (PUND) method was used. The pulsing schemes used in endurance and retention measurement are shown in Fig. 8(a) and (b). For the endurance measurement, the program/erase (P/E) bipolar cycling was employed at high-stress condition of  $\pm 4 \text{ MV}/\text{cm}$ .

Fig. 9(a) and (b) show the polarization switching amounts ( $P^*$ ) for the  $9.5$ - and  $4.5$ -nm of  $t_{\text{HZO}}$  samples, respectively. The endurance performance of the device is closely related to its  $E_{\text{BD}}$ , which is proportional to the observed endurance performance (see Fig. 9). The  $E_{\text{BD}}$  and endurance performance are improved by reducing  $t_{\text{HZO}}$ . Note that RC delay and the high endurance cycling frequency can cause the electric field across HZO to be less than the applied field. This is due to device capacitances and measurement equipment limitations. While the absolute number of breakdown cycles may differ, the performance trend across the devices remains consistent.

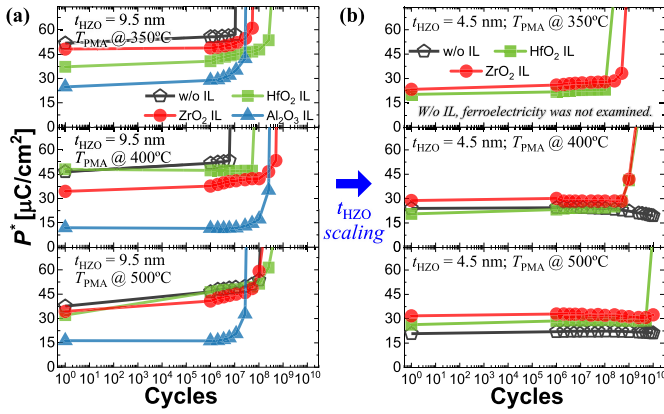


Fig. 9. Endurance performances with 4 MV/cm of bipolar cycling for the devices with (a) 9.5- and (b) 4.5-nm  $t_{\text{HZO}}$ .

Several reasons for improved dielectric robustness have been reported, including reduced electron injection energy (see Fig. 7(b)) [9], suppressed bulk charge trapping [54], and the formation of a relatively thick  $t$ -phase IL at the metal/HZO interface with decreased  $t_{\text{HZO}}$  [55].

The study yielded three significant findings with regard to endurance improvement: 1) scaling  $t_{\text{HZO}}$  and increasing  $T_{\text{PMA}}$  can improve endurance; 2) scaled  $t_{\text{HZO}}$  without IL shows similar or better endurance compared to devices with IL; and 3)  $\text{ZrO}_2$  IL provides better endurance over  $\text{HfO}_2$  IL. Generally, the endurance performance of HZO degrades as  $T_{\text{PMA}}$  increases due to increased defects and monoclinic-phase concentration [7], [40], [56]. However, the degradation of endurance is only observed from 600 °C of  $T_{\text{PMA}}$  [40], [57], [58]. In this work, no degradation in endurance was observed since  $T_{\text{PMA}}$  was intentionally limited to 500 °C to ensure BEOL process applicability.

In thin  $t_{\text{HZO}}$  devices, endurance can be improved by increasing  $T_{\text{PMA}}$  from 350 °C to 500 °C. However, decreasing  $T_{\text{PMA}}$  is a preferred method in the BEOL process. The only downside of using  $\text{HfO}_2$  and  $\text{ZrO}_2$  IL is relatively inferior endurance compared to devices without IL. To improve endurance, reducing input electric field and decreasing operation voltage are considered a reasonable direction for low-power-operation-aimed technology nodes. Importantly, the devices have sufficient  $2P_r$ , enabling further electric field reduction. Fig. 10 shows endurance measurement results measured at  $\pm 3$  MV/cm of P/E cycles on devices with 4.5-nm  $t_{\text{HZO}}$  and with  $\text{HfO}_2$  and  $\text{ZrO}_2$  IL ( $T_{\text{PMA}} = 350$  °C), which had the poorest endurance in Fig. 9(b). The devices show over 20 times improvement in endurance compared to the input with 4 MV/cm. The devices also do not experience breakdown until  $10^{10}$  cycles. This implies that degraded device endurance, the only obstacle of using IL, can be overcome by scaling the operation electric field or voltage.

To compare the effect of IL on retention, we performed retention measurements on 4.5-nm  $t_{\text{HZO}}$  devices annealed at 400 °C that are available to compare cases without and with IL, and within the reasonable range for the BEOL process [14]. The write/read pulses had an amplitude of  $\pm 3.5$  MV/cm (see Fig. 11(a)) and 1.2 V (see Fig. 11(b)). Each cycle included a

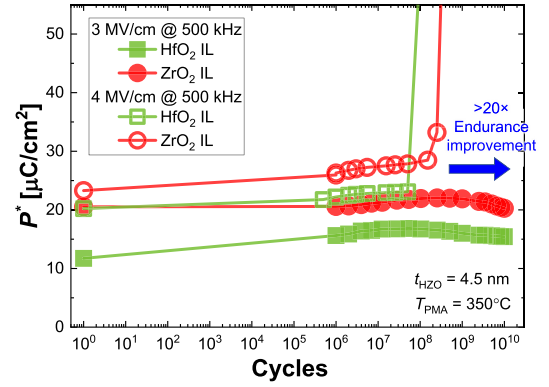


Fig. 10. Endurance improvement when the electric field of P/E bipolar cycle is reduced from  $\pm 4$  to  $\pm 3$  MV/cm. Measured devices have 4.5-nm  $t_{\text{HZO}}$  with  $\text{HfO}_2$  and  $\text{ZrO}_2$  IL.

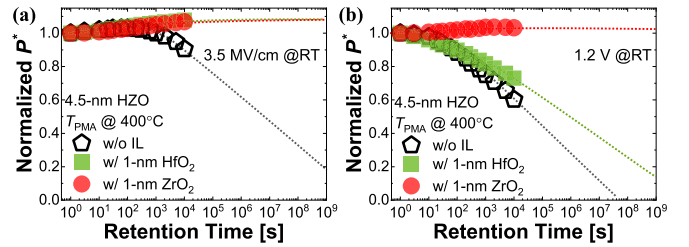


Fig. 11. Retention characteristics with 4.5-nm  $t_{\text{HZO}}$  without IL, with a  $\text{ZrO}_2$  IL, and with a  $\text{HfO}_2$  IL. (a) Fixed write/read pulses to 3.5 MV/cm and (b) 1.2 V.

positive-up (write) and two negative-down pulses (read and preset the ferroelectric layer for the next write operation) (see Fig. 8(b)).

Note, the usage of  $\text{HfO}_2$  and  $\text{ZrO}_2$  IL remarkably improves the retention behavior by suppressing depolarization field. Moreover, with  $\text{ZrO}_2$  IL, the programmed state can be retained for a projected 10 years at 1.2-V operation (see Fig. 11(b)).

The retention performance of the device without IL is the worst due to a high depolarization field. To understand this, interface capacitance ( $C_i$ ) was calculated using the formula  $1/C_{\text{total}} = 1/C_{\text{HZO}} + 1/C_i$ .  $C_{\text{total}}$  is from the capacitance measurement,  $C_{\text{HZO}}$  is the ferroelectric capacitance of the HZO layer, and  $C_i$  is the lumped capacitor including dead layer capacitance and IL capacitance. To avoid confusion, it should be clarified that the “dead layer” refers to the nonferroelectric IL generated by electrode metal oxidation, while the intentionally deposited layer of 1-nm thickness is referred to as the “IL.” The assumption is that only  $C_{\text{HZO}}$  depends on  $t_{\text{HZO}}$ . The  $C_i$  extraction process is shown in Fig. 12(a), and the calculated  $C_i$  for different  $T_{\text{PMA}}$  is indicated in Fig. 12(b). Small  $C_i$ , which is considered a major device reliability decelerating factor, induces a high field inside the IL and/or dead layer. This can be attributed to charges accumulating at the IL/dead layer boundaries, which can shield the ferroelectric polarization [59]. In particular, HZO without IL has the smallest  $C_i$  in all  $T_{\text{PMA}}$  cases, resulting in poorer retention characteristics compared to HZO with an IL. This is also consistent with the small percentage of  $V_{\text{apply}}$  on HZO without IL that we calculated in Section II. To improve device

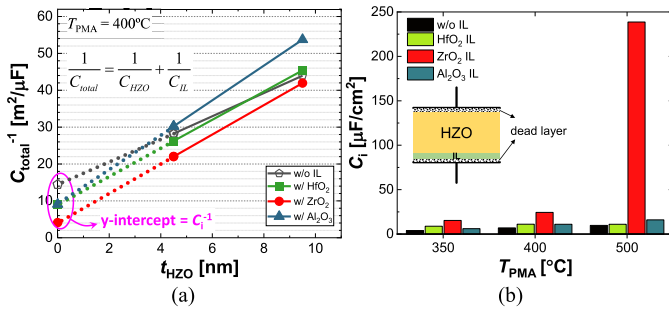


Fig. 12. Interfacial capacitance ( $C_i$ ) evaluation. (a)  $C_{\text{total}}^{-1}$  versus  $t_{\text{HZO}}$  for 400 °C annealed devices. (b) Extracted  $C_i$  of all devices.

retention performance, it is suggested to use sub-5-nm  $t_{\text{HZO}}$ , reduce the operation voltage, and adopt a 1-nm-thin IL to increase  $C_i$ .

## V. CONCLUSION

Our study proposes the use of a 1-nm IL can effectively alleviate the challenges associated with scaling  $t_{\text{HZO}}$  for use in ferroelectric devices. This is a simple but effective method that can be feasible in the BEOL process. By increasing the concentration of *o*-phase, the IL has enabled low-voltage operation with high  $2P_r$ , and improved retention by increasing  $C_i$ . At 4.5-nm  $t_{\text{HZO}}$ , ZrO<sub>2</sub> IL offers superior characteristics compared to devices without IL, including  $2\times$  larger  $P_r$ , 0.3-V lower operation voltage (reduced from 1.5 to 1.2 V), and  $>10$  years of long retention. Importantly, the use of an IL can effectively address the increased critical temperature for ferroelectric HZO crystallization associated with  $t_{\text{HZO}}$  scaling. While devices with IL show degraded endurance at high electric field operation, their performance has improved substantially under moderate operation condition of 3 MV/cm. Overall, these findings provide a promising approach for improving the performance of ferroelectric devices in advanced technology nodes.

## REFERENCES

- [1] K. Roy, A. Jaiswal, and P. Panda, "Towards spike-based machine intelligence with neuromorphic computing," *Nature*, vol. 575, no. 7784, pp. 607–617, Nov. 2019, doi: [10.1038/s41586-019-1677-2](#).
- [2] A. Chanthbouala et al., "A ferroelectric memristor," *Nature Mater.*, vol. 11, pp. 860–864, Sep. 2012, doi: [10.1038/nmat3415](#).
- [3] A. I. Khan, A. Keshavarzi, and S. Datta, "The future of ferroelectric field-effect transistor technology," *Nature Electron.*, vol. 3, no. 10, pp. 588–597, Oct. 2020, doi: [10.1038/s41928-020-00492-7](#).
- [4] D. Saito et al., "Analog in-memory computing in FeFET-based 1T1R array for edge AI applications," in *Proc. Symp. VLSI Circuits*, Jun. 2021, pp. 1–2, doi: [10.23919/VLSICircuits52068.2021.9492479](#).
- [5] C. Wang, A. Agrawal, E. Yu, and K. Roy, "Multi-level neuromorphic devices built on emerging ferroic materials: A review," *Frontiers Neurosci.*, vol. 15, Apr. 2021, Art. no. 661667, doi: [10.3389/fnins.2021.661667](#).
- [6] E. Yu et al., "Ferroelectric FET based coupled-oscillatory network for edge detection," *IEEE Electron Device Lett.*, vol. 42, no. 11, pp. 1670–1673, Nov. 2021, doi: [10.1109/LED.2021.3117229](#).
- [7] M. H. Park, H. J. Kim, Y. J. Kim, W. Lee, T. Moon, and C. S. Hwang, "Evolution of phases and ferroelectric properties of thin Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> films according to the thickness and annealing temperature," *Appl. Phys. Lett.*, vol. 102, no. 24, Jun. 2013, Art. no. 242905, doi: [10.1063/1.4811483](#).
- [8] X. Lyu, M. Si, X. Sun, M. A. Capano, H. Wang, and P. D. Ye, "Ferroelectric and anti-ferroelectric hafnium zirconium oxide: Scaling limit, switching speed and record high polarization density," in *Proc. Symp. VLSI Technol.*, Jun. 2019, pp. 44–45, doi: [10.23919/VLSIT.2019.8776548](#).
- [9] K. Toprasertpong et al., "Low operating voltage, improved breakdown tolerance, and high endurance in Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> ferroelectric capacitors achieved by thickness scaling down to 4 nm for embedded ferroelectric memory," *ACS Appl. Mater. Interfaces*, vol. 14, no. 45, pp. 51137–51148, Nov. 2022, doi: [10.1021/acsami.2c15369](#).
- [10] C.-I. Wang et al., "Evolution of pronounced ferroelectricity in Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> thin films scaled down to 3 nm," *J. Mater. Chem. C*, vol. 9, no. 37, pp. 12759–12767, Sep. 2021, doi: [10.1039/d1tc01778k](#).
- [11] S. Oh, H. Kim, A. Kashir, and H. Hwang, "Effect of dead layers on the ferroelectric property of ultrathin HfZrO<sub>x</sub> film," *Appl. Phys. Lett.*, vol. 117, no. 25, pp. 1–4, Dec. 2020, doi: [10.1063/5.0030856](#).
- [12] J. Lyu, T. Song, I. Fina, and F. Sánchez, "High polarization, endurance and retention in sub-5 nm Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> films," *Nanoscale*, vol. 12, no. 20, pp. 11280–11287, May 2020, doi: [10.1039/d0nr02204g](#).
- [13] M. H. Park, H. J. Kim, Y. J. Kim, T. Moon, and C. S. Hwang, "The effects of crystallographic orientation and strain of thin Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> film on its ferroelectricity," *Appl. Phys. Lett.*, vol. 104, no. 7, pp. 1–5, Feb. 2014, doi: [10.1063/1.4866008](#).
- [14] R. Khosla and S. K. Sharma, "Integration of ferroelectric materials: An ultimate solution for next-generation computing and storage devices," *ACS Appl. Electron. Mater.*, vol. 3, no. 7, pp. 2862–2897, Jul. 2021, doi: [10.1021/acsaelm.0c00851](#).
- [15] B. Y. Kim et al., "Enhanced ferroelectric properties in Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> films using a HfO<sub>0.61</sub>N<sub>0.72</sub> interfacial layer," *Adv. Electron. Mater.*, vol. 8, no. 6, 2021, Art. no. 2100042, doi: [10.1002/aelm.202100042](#).
- [16] V. Gaddam, D. Das, and S. Jeon, "Insertion of HfO<sub>2</sub> seed/dielectric layer to the ferroelectric HZO films for heightened remanent polarization in MFM capacitors," *IEEE Trans. Electron Devices*, vol. 67, no. 2, pp. 745–750, Feb. 2020, doi: [10.1109/TED.2019.2961208](#).
- [17] V. Gaddam, D. Das, T. Jung, and S. Jeon, "Ferroelectricity enhancement in Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> based tri-layer capacitors at low-temperature (350 °C) annealing process," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 812–815, Jun. 2021, doi: [10.1109/LED.2021.3075082](#).
- [18] C. Liu et al., "Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub>-based ferroelectric field-effect transistors with HfO<sub>2</sub> seed layers for radiation-hard nonvolatile memory applications," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4368–4372, Sep. 2021, doi: [10.1109/TED.2021.3095036](#).
- [19] C. Liu et al., "Orientation independent growth of uniform ferroelectric Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub> thin films on silicon for high-density 3D memory applications," *Adv. Funct. Mater.*, vol. 32, no. 49, 2022, Art. no. 2209604, doi: [10.1002/adfm.202209604](#).
- [20] Y. Qi, X. Xu, I. Krylov, and M. Eizenberg, "Ferroelectricity of as-deposited HZO fabricated by plasma-enhanced atomic layer deposition at 300 °C by inserting TiO<sub>2</sub> interlayers," *Appl. Phys. Lett.*, vol. 118, Jan. 2021, Art. no. 032906, doi: [10.1063/5.0037887](#).
- [21] A. A. Koroleva et al., "Retention improvement of HZO-based ferroelectric capacitors with TiO<sub>2</sub> insets," *ACS Omega*, vol. 7, no. 50, pp. 47084–47095, Dec. 2022, doi: [10.1021/acsomega.2c06237](#).
- [22] A. J. Tan et al., "Ferroelectric HfO<sub>2</sub> memory transistors with high-*k* interfacial layer and write endurance exceeding 10<sup>10</sup> cycles," *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 994–997, Jul. 2021, doi: [10.1109/LED.2021.3083219](#).
- [23] T. Onaya et al., "Improvement in ferroelectricity of Hf<sub>x</sub>Zr<sub>1-x</sub>O<sub>2</sub> thin films using ZrO<sub>2</sub> seed layer," *Appl. Phys. Exp.*, vol. 10, Jul. 2017, Art. no. 081501, doi: [10.7567/APEX.10.081501](#).
- [24] T. Onaya et al., "Improvement in ferroelectricity of Hf<sub>x</sub>Zr<sub>1-x</sub>O<sub>2</sub> thin films using top- and bottom-ZrO<sub>2</sub> nucleation layers," *APL Mater.*, vol. 7, Jun. 2019, Art. no. 061107, doi: [10.1063/1.5096626](#).
- [25] S. J. Lee et al., "Effect of ZrO<sub>2</sub> interfacial layer on forming ferroelectric Hf<sub>x</sub>Zr<sub>y</sub>O<sub>z</sub> on Si substrate," *AIP Adv.*, vol. 9, Dec. 2019, Art. no. 125020, doi: [10.1063/1.5124402](#).
- [26] M. Popovici et al., "Ferroelectric La-doped ZrO<sub>2</sub>/Hf<sub>x</sub>Zr<sub>1-x</sub>O<sub>2</sub> bilayer stacks with enhanced endurance," *Phys. Status Solidi RRL*, vol. 15, May 2021, Art. no. 2100033, doi: [10.1002/pssr.202100033](#).
- [27] W. Xiao et al., "Performance improvement of Hf<sub>0.5</sub>Zr<sub>0.5</sub>O<sub>2</sub>-based ferroelectric-field-effect transistors with ZrO<sub>2</sub> seed layers," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 714–717, May 2019, doi: [10.1109/LED.2019.2903641](#).

- [28] S.-Y. Lee et al., "Investigation of the impact of internal metal gate—From MFM capacitors to two-layer-stacked GAA poly-Si NW FE-FETs," in *Proc. Int. Symp. VLSI Technol., Syst. Appl. (VLSI-TSA)*, Aug. 2020, pp. 124–125, doi: [10.1109/VLSI-TSA48913.2020.9203642](https://doi.org/10.1109/VLSI-TSA48913.2020.9203642).
- [29] T. Onaya, T. Nabatame, M. Inoue, T. Sawada, H. Ota, and Y. Morita, "Wake-up-free properties and high fatigue resistance of  $\text{Hf}_x\text{Zr}_{1-x}\text{O}_2$ -based metal-ferroelectric-semiconductor using top  $\text{ZrO}_2$  nucleation layer at low thermal budget (300 °C)," *APL Mater.*, vol. 10, May 2022, Art. no. 051110, doi: [10.1063/5.0091661](https://doi.org/10.1063/5.0091661).
- [30] C. Huang, Y. Zhang, S. Zheng, Q. Yang, and M. Liao, "Interface effects induced by a  $\text{ZrO}_2$  seed layer on the phase stability and orientation of  $\text{HfO}_2$  ferroelectric thin films: A first-principles study," *Phys. Rev. Appl.*, vol. 16, no. 4, pp. 1–9, Oct. 2021, doi: [10.1103/PhysRevApplied.16.044048](https://doi.org/10.1103/PhysRevApplied.16.044048).
- [31] H.-S. Jung et al., "The effects of postdeposition annealing on the crystallization and electrical characteristics of  $\text{HfO}_2$  and  $\text{ZrO}_2$  gate dielectrics," *Electrochem. Solid-State Lett.*, vol. 14, no. 5, p. G17, 2011, doi: [10.1149/1.3551460](https://doi.org/10.1149/1.3551460).
- [32] W. Weinreich, L. Wilde, J. Muller, and J. Sundqvist, "Structural properties of as deposited and annealed  $\text{ZrO}_2$  influenced by atomic layer deposition, substrate, and doping," *J. Vacuum Sci. Technol. A, Vac., Surf. Films*, vol. 31, Nov. 2012, Art. no. 01A119, doi: [10.1116/1.4765047](https://doi.org/10.1116/1.4765047).
- [33] C.-Y. Chan, K.-Y. Chen, H.-K. Peng, and Y.-H. Wu, "FeFET memory featuring large memory window and robust endurance of long-pulse cycling by interface engineering using high- $k$  AlON," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: [10.1109/VLSITechnology18217.2020.9265103](https://doi.org/10.1109/VLSITechnology18217.2020.9265103).
- [34] D. Das, V. Gaddam, and S. Jeon, "Ferroelectricity in  $\text{Al}_2\text{O}_3/\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  bilayer stack: Role of dielectric layer thickness and annealing temperature," *J. Semicond. Technol. Sci.*, vol. 21, no. 1, pp. 62–67, Feb. 2021, doi: [10.5573/jsts.2021.21.1.062](https://doi.org/10.5573/jsts.2021.21.1.062).
- [35] H. J. Kim et al., "Grain size engineering for ferroelectric  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  films by an insertion of  $\text{Al}_2\text{O}_3$  interlayer," *Appl. Phys. Lett.*, vol. 105, Nov. 2014, Art. no. 192903, doi: [10.1063/1.4902072](https://doi.org/10.1063/1.4902072).
- [36] C.-J. Su et al., "Nano-scaled Ge FinFETs with low temperature ferroelectric  $\text{HfZrO}_x$  on specific interfacial layers exhibiting 65% S.S. reduction and improved  $\text{I}_{\text{ON}}$ ," in *Proc. Symp. VLSI Technol.*, Jun. 2017, pp. 152–153, doi: [10.23919/VLSIT.2017.7998159](https://doi.org/10.23919/VLSIT.2017.7998159).
- [37] V. Gaddam, D. Das, and S. Jeon, "Ferroelectricity enhancement in  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  capacitors by incorporating  $\text{Ta}_2\text{O}_5$  dielectric seed layers," in *Proc. 4th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Apr. 2020, pp. 1–3, doi: [10.1109/EDTM47692.2020.9117881](https://doi.org/10.1109/EDTM47692.2020.9117881).
- [38] Y.-C. Kao et al., "Toward highly pure ferroelectric  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  thin films by tailoring the strain in an unstable thermodynamic system," *ACS Appl. Electron. Mater.*, vol. 4, no. 8, pp. 3897–3908, Aug. 2022, doi: [10.1021/acsaem.2c00558](https://doi.org/10.1021/acsaem.2c00558).
- [39] Y.-K. Liang et al., "Demonstration of highly robust 5 nm  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  ultra-thin ferroelectric capacitor by improving interface quality," *IEEE Electron Device Lett.*, vol. 42, no. 9, pp. 1299–1302, Sep. 2021, doi: [10.1109/LED.2021.3102604](https://doi.org/10.1109/LED.2021.3102604).
- [40] M. Hoffmann et al., "Stabilizing the ferroelectric phase in doped hafnium oxide," *J. Appl. Phys.*, vol. 118, Aug. 2015, Art. no. 072006, doi: [10.1063/1.4927805](https://doi.org/10.1063/1.4927805).
- [41] T. S. Boscke, P. Y. Hung, P. D. Kirsch, M. A. Quevedo-Lopez, and R. Ramirez-Bon, "Increasing permittivity in  $\text{HfZrO}$  thin films by surface manipulation," *Appl. Phys. Lett.*, vol. 95, Aug. 2009, Art. no. 052904, doi: [10.1063/1.3195623](https://doi.org/10.1063/1.3195623).
- [42] U. Schroeder et al., "Temperature-dependent phase transitions in  $\text{Hf}_x\text{Zr}_{1-x}\text{O}_2$  mixed oxides: Indications of a proper ferroelectric material," *Adv. Electron. Mater.*, vol. 8, Sep. 2022, Art. no. 2200265, doi: [10.1002/aeml.202200265](https://doi.org/10.1002/aeml.202200265).
- [43] T. Nishimura, L. Xu, S. Shibayama, T. Yajima, S. Migita, and A. Toriumi, "Ferroelectricity of nonpolarized thin  $\text{HfO}_2$  films in  $\text{TiN}/\text{HfO}_2/\text{TiN}$  stacks," *Jpn. J. Appl. Phys.*, vol. 55, Jun. 2016, Art. no. 08PB01, doi: [10.7567/JJAP.55.08PB01](https://doi.org/10.7567/JJAP.55.08PB01).
- [44] H.-S. Jung et al., "Impacts of Zr composition in  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_y$  gate dielectrics on their crystallization behavior and bias-temperature-instability characteristics," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 2094–2103, Jul. 2011, doi: [10.1109/TED.2011.2136380](https://doi.org/10.1109/TED.2011.2136380).
- [45] S. Migita et al., "Phase transformation behavior of ultrathin  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  films investigated through wide range annealing experiments," *Jpn. J. Appl. Phys.*, vol. 58, Mar. 2019, Art. no. SBBA07, doi: [10.7567/1347-4065/ab00f6](https://doi.org/10.7567/1347-4065/ab00f6).
- [46] S. J. Kim et al., "Low-thermal-budget (300 °C) ferroelectric  $\text{TiN}/\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2/\text{TiN}$  capacitors realized using high-pressure annealing," *Appl. Phys. Lett.*, vol. 119, Dec. 2021, Art. no. 242901, doi: [10.1063/5.0075466](https://doi.org/10.1063/5.0075466).
- [47] S. Jakschik, U. Schroeder, T. Hecht, M. Gutsche, H. Seidl, and J. W. Barthab, "Crystallization behavior of thin ALD- $\text{Al}_2\text{O}_3$  films," *Thin Solid Films*, vol. 425, pp. 216–220, Feb. 2003, doi: [10.1016/S0040-6090\(02\)01262-2](https://doi.org/10.1016/S0040-6090(02)01262-2).
- [48] H. Kim, A. Kashir, S. Oh, and H. Hwang, "A new approach to achieving strong ferroelectric properties in  $\text{TiN}/\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2/\text{TiN}$  devices," *Nanotechnology*, vol. 32, Nov. 2020, Art. no. 055703, doi: [10.1088/1361-6528/abc115](https://doi.org/10.1088/1361-6528/abc115).
- [49] A. Kashir, H. Kim, S. Oh, and H. Hwang, "Large remnant polarization in a wake-up free  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  ferroelectric film through bulk and interface engineering," *ACS Appl. Electron. Mater.*, vol. 3, no. 2, pp. 629–638, Jan. 2021, doi: [10.1021/acsaem.0c00671](https://doi.org/10.1021/acsaem.0c00671).
- [50] T. Shiraishi et al., "Impact of mechanical stress on ferroelectricity in  $(\text{Hf}_{0.5}\text{Zr}_{0.5})\text{O}_2$  thin films," *Appl. Phys. Lett.*, vol. 108, Jun. 2016, Art. no. 262904, doi: [10.1063/1.4954942](https://doi.org/10.1063/1.4954942).
- [51] S.-H. Tsai et al., "Stress-memorized HZO for high-performance ferroelectric field-effect memtransistor," *ACS Appl. Electron. Mater.*, vol. 4, no. 4, pp. 1642–1650, Apr. 2022, doi: [10.1021/acsaem.1c01321](https://doi.org/10.1021/acsaem.1c01321).
- [52] U. Schroeder et al., "Temperature-dependent phase transitions in  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  mixed oxides: Indications of a proper ferroelectric material," *Adv. Electron. Mater.*, vol. 8, May 2022, Art. no. 2200265, doi: [10.1002/aeml.202200265](https://doi.org/10.1002/aeml.202200265).
- [53] J. Franc et al., "Mirror thermal noise in laser interferometer gravitational wave detectors operating at room and cryogenic temperature," 2009, *arXiv:0912.0107*.
- [54] A. J. Tan et al., "Hot electrons as the dominant source of degradation for sub-5 nm HZO FeFETs," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2, doi: [10.1109/VLSITechnology18217.2020.9265067](https://doi.org/10.1109/VLSITechnology18217.2020.9265067).
- [55] X. Li et al., "Experimental investigations on ferroelectric dielectric breakdown in sub-10 nm  $\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2$  film through comprehensive TDDb characterizations," *Jpn. J. Appl. Phys.*, vol. 61, Oct. 2022, Art. no. 101002, doi: [10.35848/1347-4065/ac8aea](https://doi.org/10.35848/1347-4065/ac8aea).
- [56] Y. Goh, S. H. Cho, S.-H.-K. Park, and S. Jeon, "Oxygen vacancy control as a strategy to achieve highly reliable Hafnia ferroelectrics using oxide electrode," *Nanoscale*, vol. 12, no. 16, pp. 9024–9031, Apr. 2020, doi: [10.1039/D0NR00933D](https://doi.org/10.1039/D0NR00933D).
- [57] E. Yurchuk et al., "Impact of layer thickness on the ferroelectric behaviour of silicon doped hafnium oxide thin films," *Thin Solid Films*, vol. 533, pp. 88–92, Apr. 2013, doi: [10.1016/j.tsf.2012.11.125](https://doi.org/10.1016/j.tsf.2012.11.125).
- [58] R. R. Khakimov, A. G. Chernikova, Y. Lebedinskii, A. A. Koroleva, and A. M. Markeev, "Influence of the annealing temperature and applied electric field on the reliability of  $\text{TiN}/\text{Hf}_{0.5}\text{Zr}_{0.5}\text{O}_2/\text{TiN}$  capacitors," *ACS Appl. Electron. Mater.*, vol. 3, no. 10, pp. 4317–4327, Sep. 2021, doi: [10.1021/acsaem.1c00511](https://doi.org/10.1021/acsaem.1c00511).
- [59] M. Grossmann, O. Lohse, D. Bolten, U. Boettger, and T. Schneller, "The interface screening model as origin of imprint in  $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$  thin films. I. Dopant, illumination, and bias dependence," *J. Appl. Phys.*, vol. 92, no. 5, pp. 2680–2687, Sep. 2022, doi: [10.1063/1.498966](https://doi.org/10.1063/1.498966).