

Roughness Suppression in Electrochemical Nanoimprinting of Si for Applications in Silicon Photonics

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Metal-assisted electrochemical nanoimprinting (Mac-Imprint) scales the fabrication of micro- and nanoscale 3D freeform geometries in silicon and holds the promise to enable novel chip-scale optics operating at the near-infrared spectrum. However, Mac-Imprint of silicon concomitantly generates mesoscale roughness (e.g., protrusion size ≈45 nm) creating prohibitive levels of light scattering. This arises from the requirement to coat stamps with nanoporous gold catalyst that, while sustaining etchant diffusion, imprints its pores (e.g., average diameter ≈42 nm) onto silicon. In this work, roughness is reduced to sub-10 nm levels, which is in par with plasma etching, by decreasing pore size of the catalyst via dealloying in far-from equilibrium conditions. At this level, single-digit nanometric details such as grain-boundary grooves of the catalyst are imprinted and attributed to the resolution limit of Mac-Imprint, which is argued to be twice the Debye length (i.e., 1.7 nm)—a finding that broadly applies to metal-assisted chemical etching. Last, Mac-Imprint is employed to produce single-mode rib-waveguides on pre-patterned silicon-on-insulator wafers with root-mean-square line-edge roughness less than 10 nm while providing depth uniformity (i.e., 42.9 ± 5.5 nm), and limited levels of silicon defect formation (e.g., Raman peak shift < 0.1 cm⁻¹) and sidewall scattering.

1. Introduction

Silicon photonics utilizes a variety of micro- and nanostructured waveguide and metamaterial-based components to enable

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applications such as optical interconnects within a chip, from chip-to-fiber and chip-to-chip.[1] However, the efficiency, performance, minimum feature size, and scalable manufacturing of chipscale silicon photonic devices is presently constrained to 2D designs compatible with modern deep ultraviolet or immersion lithography combined with reactive ion etching (RIE).[2,3] Introduction of 3D designs with grayscale or multilevel etch depths has been proposed to increase the performance and/or compactness of grating couplers, [4-6] edge couplers, [7] multimode waveguide bends,[8] waveguide crossings,^[9] polarization convertors,^[10] small-mode area waveguides,[11,12] and more. It also allows for the fabrication of advanced 3D photonic devices such as spoof surface plasmon structures, [13] chromatic-aberration corrected lenses,[14] and quasicrystal interferometers with physical unclonable functions.[15] However, such 3D structures are sensitive to depth and

shape inaccuracy of plasma etching and have so far remained challenging to realize while maintaining the scalability requirements of the semiconductor industry.

Recent demonstrations of 3D or multilevel silicon photonic components have utilized multiple lithography and RIE steps to achieve multilevel etch depths, [4-6] or grayscale electron-beam lithography (EBL) to achieve analog profiles. [8,9] The former multistep photolithography-based process inherently prohibits the independent and arbitrary control of lateral feature size and depth, while the latter EBL-based process is a direct writing technique and is not a scalable manufacturing solution. Both processes also require precise control over RIE selectivity, etching rate, and time to achieve the precisely desired silicon micro- or nanostructure dimensions. This challenging task is further complicated by loading effects and aspectratio-dependent etch rates.[16,17] Alternatively, the independent control of feature size and depth can be attained using direct parallel nanofabrication methods such as nanoimprint lithography of inorganic materials, which can either 1) mechanically pattern molten or porosified substrates,[18,19] or 2) electrochemically carve it via metal-assisted electrochemical nanoimprinting (Mac-Imprint).[20-22] The former two approaches are unable to pattern SOI wafers and retain its solid and single-crystalline SOI characteristics. Mac-Imprint by-passes this issue by

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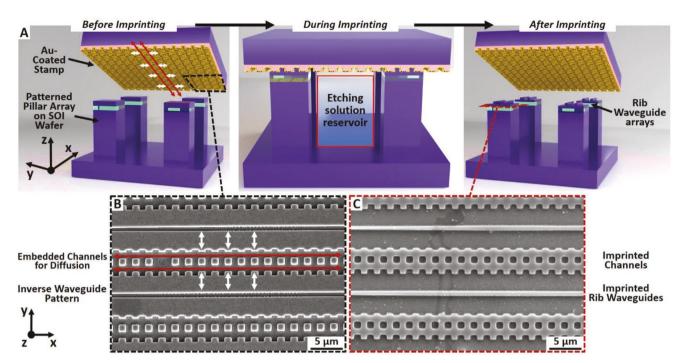


Figure 1. A) Schematics of the catalytic stamp and patterned SOI wafer interaction during Mac-Imprint. B,C) Top-down SEM images of catalytic stamp and Si rib waveguide patterns, respectively. The coordinate systems indicate the parallel (x), perpendicular (γ) and vertical (z) directions relative to the principal axis of the waveguide. The arrows highlight the solution diffusion pathways: red: through the embedded channels toward the center of the SOI pillar, and white: through the catalyst in-between embedded channels and waveguide patterns.

catalyzing the corrosion of silicon at the contact points between itself and a noble-metal coated stamp in the presence of hydrofluoric acid and an oxidizer (Figure 1A)^[22,23] whose detailed mechanism has been explained in existing literature on metalassisted chemical etching (MACE) that is focused on thin-film catalysts directly deposited onto silicon.^[24–26] Unlike MACE, in which the noble metal catalyst is not reusable and it's motion governed by the crystallography orientation of Si and etching conditions,^[27,28] Mac-Imprint by-passes these issues as the noble-metal catalyst is mechanically attached to the stamp and is retrieved upon each imprint cycle. At the same time, it introduces demolding issues such as delamination particularly prominent in high-aspect ratio structures (>1).

High pattern-transfer fidelity during Mac-Imprint of monocrystalline Si (Figure 1B,C) requires mass-transport of reactants through a nanoporous gold (np-Au) catalyst, $^{[23,29]}$ because solid catalysts cannot provide sufficient diffusion on length scales larger than 0.5 μm if Si is to be etched without concomitant porosification. At the same time, the catalyst pore size (e.g., average diameter \approx 42 nm in Sharstniou et al.) accurately transferred onto the bottom and sidewalls of the imprinted surface which increases bottom and line edge roughness (LER) of imprinted structures (i.e., \approx 49 nm) and induces prohibitive levels of scattering losses in waveguides. Conventional RIE machined waveguides have an as-machined roughness of 10 nm that can be smoothened in post-processing down to 2 nm. $^{[32]}$

With the goal of prototyping functional silicon rib waveguides using Mac-Imprint of SOI wafers, this paper elucidates the mechanism by which roughness is generated and suppresses it by reducing the pore size of the catalyst to sub-10 nm levels. The latter is attained via the synthesis of np-Au in far-fromequilibrium conditions using established process-structure relationships for dealloying.^[33] Bottom roughness surrounding the waveguide and its LER are reduced to less than 10 nm which represents a 75% improvement relative to prior work.^[23] At the lowest roughness levels, the grain boundary grooves of the np-Au are discernible on the surface of the imprinted Si and is a major contributor to it. This observation is discussed in the context of the resolution limit of Mac-Imprint and MACE which was first hypothesized by Sugita et al. to be proportional to the Debye length present at the metal-solution interface.^[34] Albeit never experimentally confirmed, a new analysis of previous work on MACE with ultra-fine gold nanoparticles reported by Liu et al.^[35] along with experimental data presented in this work strongly support Sugita's hypothesis to be true. This finding directly applies to both Mac-Imprint and MACE as they share the same fundamental mechanisms. Additionally, the influence of the solution diffusion supported by the porous catalyst on Mac-Imprint's patterning fidelity is presented in comparison to its solid counterpart. The reduced pore sizes of the catalyst increase the cathodic reaction rate, [23] which is compensated by increasing the Chartier-Bastide parameter (known as " ρ " in literature)^[25] to 99.5% yielding Si waveguides with limited levels of defect formation as characterized by Raman spectroscopy. Finally, the optical characterization of nanoimprinted rib waveguides 1) confirms the single mode light propagation which matches electromagnetic simulations, and 2) IR imaging reveals no significant levels of light scattering from its walls.

2. Results and Discussion

Mac-Imprint of Si waveguides onto the SOI pillars requires diffusion of reactants and byproducts over a large (e.g., >75 µm) and a heterogeneous pathway. This path extends from the edge of the pillar where reactants are stored in the solution reservoir confined around the pillar and toward its center (Figure 1A,B) and consists of embedded channels in the stamp parallel (i.e., x-direction) to the waveguide's principal axis (red arrows on Figure 1A,B) that are formed in the gaps between stamp and substrate upon their contact. Additionally, the solution must diffuse in the perpendicular direction (i.e., y-direction) between the waveguide and the embedded channels through the catalytic film (white arrows on Figure 1A,B) for a total distance of 3 µm. Note that the scenario in which diffusion takes place through a porosified silicon layer is detrimental to the waveguide's performance as it can create refractive index spatial variations.^[23] When both pathways support enough etching solution diffusion, the pattern from the stamp is accurately transferred onto Si without porous defects (Figure 1C).

2.1. Limiting Diffusional Pathways

In order to evidence the role of the catalyst film's porosity on supporting diffusion of the etching solution, pre-patterned SOI chips were Mac-Imprinted with stamps coated with thinfilms of solid Au (Figure 2A,B) and porous Au (Figure 2C,D). Pillars imprinted with solid Au stamps yielded waveguide patterns near its edges with distinguishable profile and depth (Figure 2B). However, the pattern becomes shallower and loses contrast in the scanning electron microscopy (SEM) images as it approaches the center of the pillar. The average distance from the edge of the pillar to the end of the distinguishable waveguide pattern is indicated by solid yellow arrows in Figure 2B.D and termed as the effective etching penetration distance (EEPD). At the end of the EEPD, not only patterns become indistinguishable, but SEM images reveal the formation of porous silicon defects (dark areas in Figure 2B). Note, that periodic grating with the period of 273 ± 8 nm and heights of 82 ± 10 nm could be observed on high magnification SEM image (Figure 2B) along the edge of the waveguide. The geometry of this grating mimics the one of original Si master mold highlighting the resolution capability of Mac-Imprint.

In contrast, pillars imprinted with porous Au stamps (Figure 2D) yielded an EEPD value that is maximum, and, thus, the entire half-width of the SOI pillar was successfully imprinted with the waveguide's pattern without any observable defect (e.g., porous silicon) formation. In a separate experiment, the largest EEPD that the porous catalyst and embedded channels can support was found to be $\approx\!\!700~\mu m$ by imprinting a Si substrate with wider pillars and a blank Si wafer (see Figures S1 and S2, Supporting Information), suggesting the porous catalyst cannot support diffusion beyond that length scale. Note, the periodic grating with the period of 255 \pm 2 nm and heights of 64 \pm 7 nm is also observed in the case of Mac-Imprint with np-Au (Figure 2D).

In contrast to the imprint results with the solid catalyst (Figure 2A,B), the addition of the thin porous catalyst represents a small increase in the cross-sectional area available for

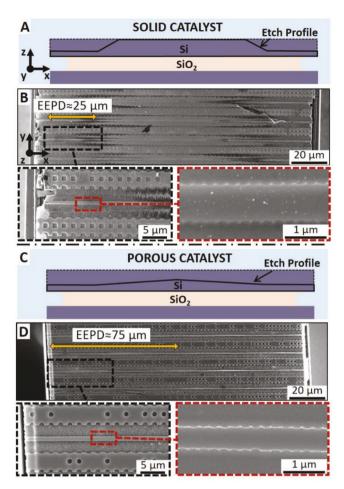


Figure 2. A,B) Schematic cross-sectional and top-down SEM images, respectively, of waveguide arrays imprinting with solid Au catalyst. Inset in (B) highlights the beginning of porous silicon formation region. C,D) Schematic cross-sectional and top-down SEM images, respectively, of the waveguide arrays imprinting with porous Au catalyst. The solid yellow arrows indicate the length of the region with distinguishable waveguide pattern (EEPD).

free-solution diffusion in the parallel direction (x-direction) and, thus, the effective diffusion constant is expected to be marginally altered. However, the effective diffusion constant along the perpendicular direction (y-direction) has been increased by orders of magnitude in comparison to the case of the solid catalyst. That is because the diffusion in the solid catalyst is supported through the grain boundaries which support a diffusional regime known as molecular sieving with an effective diffusion constant that is orders of magnitude lower than the diffusion in free solution.^[23] Meanwhile, the porous catalyst has pore sizes ranging from 10 to 42 nm which are much larger than the electric double layer thickness which is ≈8.6 Å (for detailed calculations, see Supporting Information), and can support free solution diffusion,[36] with simple corrections for tortuosity.[37,38] Note that the thickness of the precursor film was selected to be much larger (e.g., nine times) than the catalyst's pore size (i.e., 42 nm) to sustain diffusion through a well-developed 3D pore network without any optimization in its selection. A "digital twin" model that captures both reaction rate and

diffusional transport for Mac-Imprint with thinner catalysts is likely needed in the future to address such design questions. Instead, in this work, the catalyst's high-surface area and its increased cathodic reaction rate is compensated by increasing the Chartier–Bastide parameter (known as " ρ " in literature)^[25] to 99.5% until porous silicon formation is suppressed as characterized by Raman spectroscopy. Alternatively, the use of a counter electrode in solution biased against the gold catalyst as in prior works of Torralba et al.^[21] and Kim et al.^[39] is recommended as it does not require hydrogen peroxide and the reaction rate can be externally controlled via biasing.

In addition to the role of diffusion mechanisms, the results for the solid catalyst case such as the short EEPD, the non-uniform etch depth, and the porous silicon formation (Figure 2A,B) cannot be fully understood unless one considers the kinetics of the etching reaction during MACE. At first, oxidant is reduced on the surface of a noble metal (cathodic reaction), which results in the generation of positive charge carriers (holes) in Si.[25] Then, the holes are injected into Si through noble metal/Si Schottky junction and subsequently consumed during Si dissolution (anodic reaction).[25] Thus, whenever the diffusion of reactants toward the catalyst/Si contact interface is not sufficient, instead of confined etching under the catalyst, the porosification of silicon takes place around the catalyst/Si/ etching solution triple junction in both conventional MACE as well as in Mac-Imprint.^[22,23,30] This is expected to take place in the case of Mac-Imprint with solid catalyst since the masstransport for the etching solution in the perpendicular direction (i.e., labeled as "2" in Figure 3A) is constricted. Thus, the holes injected into Si at its junction with the catalyst (i.e., step labeled as "1" in Figure 3A) can diffuse through the substrate to the interface between the etching solution and Si (i.e., step labeled as "3"). Once holes reach the etching solution/Si interface they induce its porosification (step labeled as "4"). Upon the growth

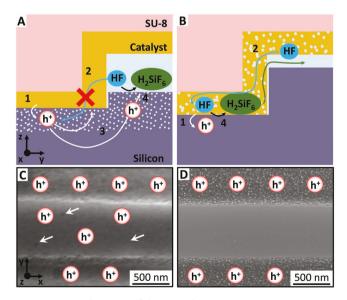


Figure 3. A,B) Schematics of charge- and mass-transport processes. C,D) High-magnification top-down SEM images of the individual waveguides. Holes are added to illustrate the charge carrier distribution around catalyst/Si interface. The white arrows point to the visible pores. (A)/(C) and (B)/(D) correspond to Mac-Imprint with solid and porous catalysts, respectively.

of a porous silicon layer underneath the catalyst, the anisotropic etching of silicon can take place since etching solution can now reach the catalyst/Si interface. This mechanism can explain the concomitant observation of anisotropically etched features (i.e., waveguide geometry) near the edges of the Si pillar (Figure 2B) and the porosification of the silicon surface observed in Figure 3C. Note that porous silicon is observed both in the regions surrounding the waveguide as well as in itself.

Ultimately, the uncontrollable porosification process is more pronounced on the edge of the pillar due to the abundant supply of reactants and is followed by its fast depletion in the embedded channel resulting in shallow etching depths in the center of the pillar which defines the EEPD distance. These findings highlight the fundamental limitation of solid catalyst since it cannot support the perpendicular diffusion for anisotropic imprinting of the designed 3 µm wide features, which is consistent with MACE literature on thin-film catalyst formats.[30,40,41] In recent literature of Si Mac-Imprint with solid catalysts, this issue was by-passed by designing stamps with an array of widely spaced patterns that simultaneously provided space for solution storage and were narrow enough (<520 nm) to sustain diffusion through the grain boundaries of catalyst or a porous layer underneath it.[42] Despite enabling diffusion, the nanoporous catalyst has higher specific surface area compared to its solid counterpart. This will inevitably increase the rate of H₂O₂ reduction and, as a result, lead to Si porosification. [23] Thus, this work implemented a reduction of the H₂O₂ concentration relative to the literature in MACE based on thin-films, [25] and increase in ρ value to 99.5% to minimize this effect and yield solid waveguides in Figure 3D. It should be noted that the cathodic reaction can be spatially separated from the anodic reaction, [43] with a counter electrode placed in solution polarized against the gold catalyst with or without a salt bridge,[21] which guarantees that diffusion and solution storage limitations associated with H₂O₂ and its reaction products can be eliminated.[43]

In order to qualify the imprint results, the waveguide's crosssectional depth profiles were extracted via atomic force microscopy (AFM) (Figure 4A) and analyzed. Its average depth was 42.9 ± 5.5 nm (Figure 4B) with a maximum of 60 nm at the edge and a minimum of 29.7 nm at ≈20 µm from the edge. The maximum depth is closer to the edge of the pillar (Figure 4B) which could be explained by: a) the non-flatness of the stamp resulting from molding issues, b) the proximity to the solution storage reservoir resulting in a faster etching, and c) the bending of the stamp due to contact forces. A gradual reduction of the depth profile as a function of the distance from its edge (i.e., horizontal axis in Figure 4B) is consistent with abovementioned scenarios "b" and "c." However, given the random nature of the depth profile (Figure 4B), the stamp's non-flatness (i.e., scenario "a") is the most consistent explanation. In fact, stamps were prepared by UV NIL of spin-coated SU-8 resist with soft PDMS-based molds (as described in the Experimental Section) which is known to introduce pattern distortions during demolding operation such as rimming,[44-46] which is a protrusion of the pattern's edges similar to the inverse of the silicon pattern observed in the inset of Figure 4B. Thus, the depth profile in Figure 4B is irregular since Mac-Imprint imprints the distorted geometry of the mold with high fidelity. This hypothesis

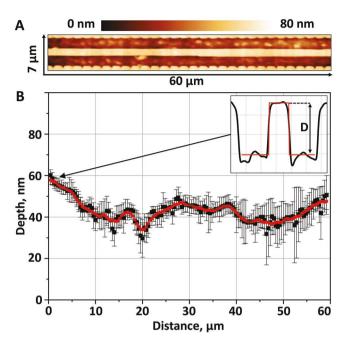


Figure 4. A,B) Depth analysis of imprinted waveguide with uniform depth showing large-area AFM scan of a single waveguide from the edge (left) to the center (right) of the SOI pillar (A), and the waveguide's depth profile (black squares) and three-point moving average (red squares) (B) with the inset highlighting one of the waveguide's cross-sectional and depth measurement (label D). The bottom sub-20 nm roughness of the waveguide surroundings induced by the catalyst cannot be detected due to the low resolution of the large-area AFM scan shown in (A). The data represent depth extracted through fitting of step-height function with error bar representing fitting error.

was further confirmed in the additional experiment where AFM scans of imprinted SOI pillar and Mac-Imprint stamp were acquired at complimentary locations and are indeed mirror images of each other (see Figure S3, Supporting Information). Note that the large and low-resolution AFM scan in Figure 4A does not provide enough resolution (see details in the Experimental Section) to capture the porous gold morphology imprinted onto silicon.

2.2. Roughness Reduction and Its Fundamental Limits

Mac-Imprint introduces bottom and sidewall roughness which originates from its resolution limit (i.e., minimum discernible positive feature) being smaller than the pore diameter of the catalyst and results in the accurate transfer of the catalyst's nanopores onto the imprinted surface. Thus, with the goal to address the roughness issue, it becomes necessary to find a theoretical basis to Mac-Imprint's resolution limit. In 2011, Sugita et al. In the silicon around the electrolyte—silicon—metal triple junction in the context of anodic electrochemical machining of silicon. Based on the work of Nakato et al., Sugita et al. proposed that the strong electric field developed in the electrical double layer at electrolyte—metal interface reduces the potential barrier in silicon near the electrolyte—silicon—metal junction (Figure 5A). This should lead to the migration of holes in silicon away from the triple junction

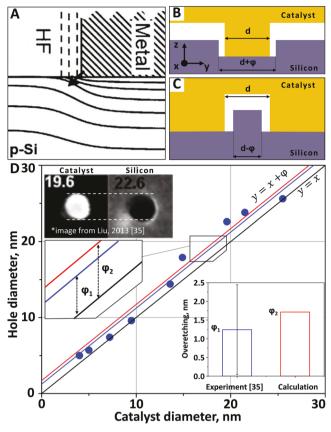


Figure 5. A) Theoretical model for band bending during anodic electrochemical machining of Si proposed by Sugita et al. Dashed lines at metal–solution interface represent isopotentials within the electrical double layer (Debye length) and solid lines represent isopotentials bending around the triple junction. Reprinted (adapted) with permission. [34] Copyright 2011, American Chemical Society. B,C) Schematics of the overetching for the negative and positive Si features, respectively (not to scale). D) Plot of silicon hole versus catalyst diameter using imported data from Liu et al. [35] Three lines with a unity slope are plotted with different offsets: zero (black – reference), best fit of experimental data (blue, ϕ_1), and two times the Debye length (red, ϕ_2). ϕ_1 on the bar plot is reported as average \pm standard deviation based on nine reported measurements. The upper inset contains top-down SEM images of the metal catalyst and the resulting hole in silicon. The inset images and data are adapted with permission. [35] Copyright 2013, American Chemical Society.

to a distance proportional to the Debye length. If this theoretical basis is correct, it would result in silicon features being overetched by a lateral distance, φ , that is proportional to the Debye length (Figure 5B) which has not been experimentally verified in literature. While Sugita et al. worked with feature sizes ranging from 10 to 100 μ m, recent experimental work on MACE by Liu et al. yielded sub-5 nm features. Using data from Liu et al., it is possible to calculate the average overetched distance (i.e., φ_1 in Figure 5D), which is the difference between catalyst diameter and silicon hole diameter and equals to 1.24 nm. This value closely matches two times the theoretical value of the Debye length (φ_2 in Figure 5D) which is 1.71 nm (see calculations in Supporting Information). Note that the large standard deviation (SD) of φ_1 (i.e., \pm 1.2 nm, details in the Table S2, Supporting Information) could be attributed to: 1) errors of the

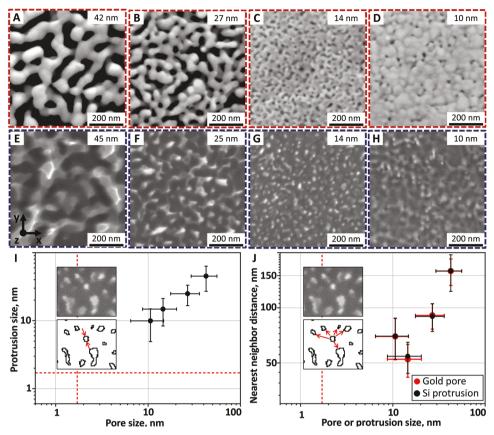


Figure 6. A—H) Top-down SEM images of the catalytic stamps with different average pore diameters (A—D) and imprinted waveguide surroundings (E—H). The boxes in the top right corner of the SEM images contain the average pore (A—D) and protrusion (E—H) diameters. I) Dependence of Si protrusion size on the catalyst pore size. Inset in (I): Illustration showing how the feature size (either pore or protrusion) was calculated. J) Dependence of nearest neighbor distance on the catalyst pore size and Si protrusion size (red and black, respectively). Inset in (J): Illustration showing how the nearest neighbor distance was calculated. Data are reported as average ± standard deviation. The red dashed lines in (I) and (J) indicate the resolution limit (i.e., double the Debye length).

measurement technique associated with limited resolution or 2) catalyst particle size distribution if catalyst and hole widths are not measured in complementary locations.^[48]

Next, this work attempts to eliminate roughness by designing catalyst films whose pore sizes approach the Debye length to within at least an order of magnitude (Figure 5C). This was accomplished by using previously established process-structure relationship in the electroless dealloying of Au₄₉Ag₅₁ thinfilms at far-from-equilibrium from literature which allows for ligament control between 25 and 64 nm.[33] By reproducing it and further reducing the dealloying time and temperature (for additional details, see Experimental Section), catalyst films with average pore diameters of 42, 27, 14, and 10 nm were fabricated (Figure 6A-D) and used to Mac-Imprint arrays of linear rib waveguide structures (Figure 6E-H). Additionally, albeit pores on Figure 6C,D appear isolated, a developed porous network structure is still formed throughout the thickness of the catalytic films which was confirmed by high-magnification crosssectional SEM images (Figure S4, Supporting Information). The impact of the pore size of the catalyst on the surface roughening during Mac-Imprint was established through the SEM analysis of imprinted linear rib waveguide structures. Overall, the catalyst size downscaling to 10 nm reduced the Si protrusion

size linearly (Figure 6I) from 45 nm (Figure 6E) to 10 nm (Figure 6H). In the latter case, it was observed that the grain boundary grooves of the catalyst are also transferred onto silicon which limits further reductions in its roughness.

In context to existing literature, Bastide et al. [29] and Sharstniou et al.[23] each attempted to reduce the catalyst pore size and roughness, but, at least in qualitative terms, their work did not reduce either the silicon protrusion size or roughness due to stamp defects (e.g., cracks and delaminated catalyst) transferred during imprinting and concomitant substrate porosification. In their works, the smallest distinguishable average Si protrusion size without indication of porosification was ≈27 and 31 nm.[23,29] Finally, according to the nearest neighbor analysis (for details, see Experimental Section) the average distance between nearest neighbor pores in the catalyst matches that of the Si protrusions (Figure 6J, red and black dots, respectively). Note that there is an increase of the nearest neighbor distance in the case of the smallest catalyst pore size (i.e., 10 nm) which is attributed to incomplete Ag removal during dealloying which is known to produce lower pore surface area coverage and, thus, increases the interpore distances.^[33]

Since the smallest pore size attained via electroless dealloying in this work is still five to six times larger than the

theoretical value for twice the Debye length, further reduction in the Si protrusion size is theoretically possible albeit the synthesis of catalysts with sub-10 nm average pore size becoming the limiting factor. In the literature of nanoporous gold synthesis through dealloying, the electroless and electrochemical dealloying methods have demonstrated the smallest pore size of ≈5 nm by either reducing its temperature (e.g., -20 °C)[49] or inhibiting gold adatom surface diffusion. [50,51] It was also shown that during dealloying ligament and pore size are inversely proportional to the melting temperature of host metal,^[52] suggesting that higher melting temperature metal or alloys catalysts suitable for MACE, such as platinum, could be potential candidates to further reduce pore size into the sub-5 nm domain.[41,53,54] It should also be noted that, to promote smoothening of the nanoimprinted surfaces, the Debye layer thickness can be increased to approach the catalyst's pore size by: 1) heating the etching solution and 2) decreasing its ionic strength. The first approach would increase Debye layer thickness by ≈1 Å given the low boiling point of the solution. The second approach can be achieved by reducing its concentration or by using solutes with a weaker dissociation constant both of which would reduce etch rates dramatically. These strategies should motivate future work to either eliminate the roughness or to improve the resolution limit of Mac-Imprint or MACE.

Although the bottom roughness of the waveguide surroundings may interfere with the guided electromagnetic wave, most of the propagation losses occur due to light scattering on the sidewall roughness of the waveguide. In Mac-Imprint, it is generated by the tangential movement of the np-Au surface parallel to the vertical direction of the Si sidewalls as the etching progresses, leaving "scratch" marks along it. Thus, in theory, the flatter and less rough the porous Au surface is, the smoother the sidewalls should become. To verify this hypothesis, the LER of the imprinted waveguides was measured at its top as a function of the pore size of the catalyst according to the procedure described in the Experimental Section. Figure 7E shows that, with the reduction of the pore size of the catalyst from 42 to 10 nm, the LER non-linearly decreases from 48 nm (Figure 7A) to 10 nm (Figure 7D), which is comparable with values reported for plasma-based micromachined silicon waveguides without post-processing strategies for smoothening.[32,55] The smallest LER in silicon features achievable by Mac-Imprint would be inherently limited by the LER of the stamp's pattern coated with solid gold which was measured to be ≈7.5 nm (Figure 7E, yellow dashed line) and is attributed to the roughness of gold thin-film and imperfections from soft-lithography steps used to fabricate the stamp. Thus, the improvements in sidewall roughness tend to saturate for pore sizes approaching 7.5-10 nm (Figure 7E) limiting further improvements. It is worth noting that, at the magnification and the pixel size of the analyzed SEM images which are 30 000× and 6.7 nm, respectively, it might also limit measurement of further improvements at sub-10 nm pore sizes and require the use of alternate metrology techniques.

The minimization of LER to sub-10 nm is expected to have a positive impact on the minimum line-width resolution (MLWR) of Mac-Imprint. Albeit never experimentally determined, a reasonable criterion to estimate the MLWR of a process is to use a 6-sigma approach based on sidewall LER (see Figure S5,

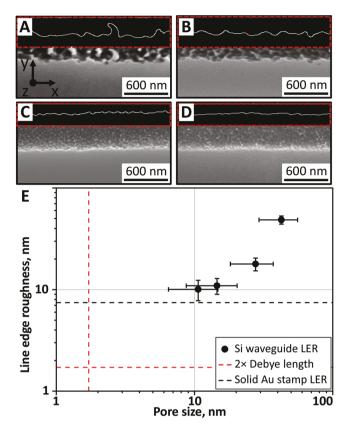


Figure 7. A–D) Top-down SEM images and edge profiles (framed with red dashed lines) of the waveguides, imprinted with porous catalysts with average pore sizes 42–10 nm, respectively. E) Waveguide line edge roughness as a function of catalyst pores size. Data are reported as average \pm standard deviation. The dashed lines indicate twice the Debye length (red) and solid Au stamp sidewall LER (black).

Supporting Information). According to this assumption, the reduction of the LER achieved with np-Au's pore size of 10 nm would translate to MLWR values of \approx 60 nm which is a significant improvement comparing to the state-of-the-art whose largest pore size of np-Au used was 42 nm.^[23]

2.3. Nanoscopic Defect Analysis

It is important to mention that the reduction of the catalyst pore size through the far-from-equilibrium dealloying leads to the incomplete removal of silver that can negatively affect Mac-Imprint process. In particular, in contrast to gold, silver: 1) induces changes to the energy band bending in silicon near catalyst/Si interface due its lower work function, which affects hole injection and transport in Si and induces its porosification, [53,56] and 2) is prone to dissolution and subsequent re-deposition. Despite catalysts with the smallest pore size being made with the shortest dealloying time, the large residual silver content of up to 42 at% did not appear to induce porosification as evidenced by the SEM or optical microscopy. However, the porosification of Si could be happening in nanoscale form that would be challenging to detect using these techniques.

The analysis of the such defects during Mac-Imprint was accomplished by Raman spectroscopy, which has been extensively used in theliterature to characterize defects in silicon such as lattice strains, [59] microporosity (i.e., sub-2 nm) and mesoporosity (i.e., 2-50 nm), [60] and amorphous regions. [61] The imprinted waveguide, presented in Figure 8A,B, exhibited average peak position and full width at half-maximum (FWHM) of \approx 521.38 \pm 0.07 and \approx 4.20 \pm 0.06 cm⁻¹, respectively (Figure 8C,D), throughout the center section of the waveguide excluding 6 µm away from each edge. At each of the edges, a 0.09 and 0.44 cm⁻¹ shift to lower frequencies, and a 0.16 and 0.08 cm⁻¹ broadening of the Raman signal was observed (see locations i and xi in Figure 8E,F). These edge effects are attributed to the release of the residual stresses and strains in the Si device layer by the undercut (Figure 2A) of the buried oxide layer during Mac-Imprint, as seen on Figure 8A,B near

the edges of the SOI pillar. In fact, SOI processing is well known to introduce strains in the Si device layer which causes Raman peak to shift by ± 0.4 cm⁻¹ from its mean position. [62] In our case, the blank SOI wafer had a peak position and FWHM of 521.47 \pm 0.02 and 4.15 \pm 0.04 cm⁻¹, respectively. With regards to it, the average peak position at the center of the waveguide shifts and broadens by ≈0.2 and 0.1 cm⁻¹, respectively, which is smaller than the expected values for microporous silicon (i.e., both ≈1 cm⁻¹ for crystallite sizes of <5 nm). [60] Note that, in locations viii and xi in Figure 8 on the waveguide's narrowest section, there are geometrical defects originated from molding defects in the stamp that cannot be well understood. Overall, the center section has a constant peak position and width relative to the Raman signal from the original SOI wafer which adds further confirmation of the crystallinity quality of the imprinted waveguides. In future applications, these edge effects

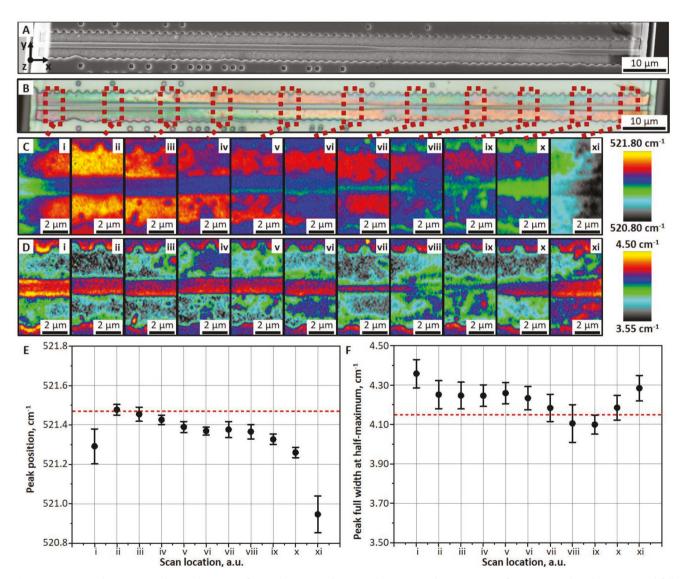


Figure 8. A,B) Top-down SEM and optical images of a single imprinted waveguide, respectively. C,D) Maps of Raman signal peak position and full width at half-maximum, respectively, taken at locations marked on (B). E,F) Average values for Raman peak position and full width at half-maximum, respectively, of the waveguide at location marked on (B). Data are reported as average \pm standard deviation. The red dashed lines in (E) and (F) high-light the Raman peak position and full width at half maximum of the blank SOI wafer.

can be by-passed if necessary to avoid unnecessary scattering by patterning away from the edge or protecting the buried oxide layer during Mac-Imprint.

Lastly, optical waveguiding is demonstrated in a Mac-Imprinted silicon rib waveguide (Figure 9A). The top-view IR imaging (Figure 9B) did not reveal a detectable scattering of the signal from the waveguide's walls, which suggests low scattering loss. The waveguide unfortunately was too short (L = 0.015 cm) to precisely measure its loss. The waveguide mode simulation of the rib waveguide with nominal width, w = 750 nm, and imprint depth, h = 43 nm, (Figure 9D) is presented on Figure 9C and demonstrates the single mode and quasi-transverse-electric polarized nature of the waveguide. The convolution of the simulation with the point-spread-function (PSF) of the 0.42 numerical apperture imaging objective is presented in Figure 9E and closely matches the output side-view image of the waveguide facet (Figure 9F). For more details on the convolution between simulated waveguide mode and PSF of the objective refer to the Figure S6, Supporting Information. It has previously been shown that that single mode rib waveguides with similar dimensions can exhibit favorable loss characteristics when compared to fully etched strip waveguides, owing to limited interaction between the waveguide mode and the waveguide surface. [63] Hence, optical propagation losses are expected to be a function of both the waveguide design and the

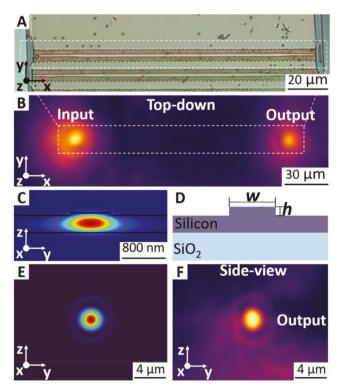


Figure 9. A) Top-down optical image of the individual SOI pillar prior to waveguide testing. B) Top-down infrared image of the individual SOI pillar during waveguide testing. The dashed lines in (A) and (B) highlight the tested waveguide. C) Side-view of waveguide mode simulation. D) Cross-sectional schematics of the waveguide, used for the simulation. E) Side-view of simulated waveguide mode, corrected by PSF of 0.42 numerical apperture objective. F) Side-view infrared image of the output waveguide facet.

surface roughness. The optical characterization demonstrated here importantly confirms that the Mac-Imprint process can be utilized to fabricate functional silicon photonic waveguides.

3. Conclusion

We have reported the first extension of Mac-Imprint to SOI substrates and to geometries specific to requirements of silicon rib waveguides. It was established that the mass-transport of the reactants in the perpendicular direction of the waveguide's longitudinal axis is the limiting factor for attaining imprinting of uniform patterns without porosity. This mass transport could not be supported by solid catalysts. In contrast, a nanoporous catalyst provided necessary diffusional pathways which allowed for fabrication of Si waveguides with an average depth of 42.9 ± 5.5 nm. This depth variation was attributed to the stamp distortions during demolding of the stamp during its fabrication which can be improved using commercial nanoimprinting tooling. The bottom and sidewall roughness induced by Mac-Imprint was controlled by reducing the pore sizes to within an order of magnitude of the Debye Length (i.e., the resolution limit of the Mac-Imprint). In particular, 10 nm-pore-size catalyst resulted in a 10 nm bottom and sidewall roughness of the Si rib waveguide which is comparable to similar structures which are made by conventional plasma etching methods. The limited levels of Si defect formation during Mac-Imprint were achieved by the use of the etching solution with high ρ parameter of 99.5% and were confirmed by Raman analysis of the imprinted waveguide, which revealed a uniform peak position and FWHM thought the middle portion of the waveguide excluding edges. Fabricated waveguides support single-mode light propagation which was measured by the side-view IR imaging and closely matches electromagnetic simulations. Additionally, top-down IR imaging does not reveal detectable light scattering from the waveguide walls. Overall, this paper represents a significant step toward commercial implementation of the Mac-Imprint for the fabrication of functional 3D freeform optoelectronic devices, such as advanced waveguides, [8-12] surface plasmon structures, [13] and chromatic-aberration corrected lenses. [14] Moreover, Mac-Imprint's unique ability to tailor its nanoscale roughness could be advantageous in fabrication of quasicrystal interferometers with physical unclonable functions which are essential for hardware and information security.[15] In the future, improvements to the stamp design aimed at embedding the etching solution storage reservoir in it instead of in the substrate are necessary for scaling the technique to blank SOI wafers. The work on determining the maximum EEPD supported by the thin-film catalyst in this work should inform the reasonable pitch that should exist between the embedded reservoirs in such proposed stamp designs. This approach will also allow for free optimization of Mac-Imprint parameters as the undercut of the BOX layer of the SOI pillar will be eliminated entirely. The authors also see potential scaling of Mac-Imprint in its integration with commercial mask aligners and nanoimprinting technologies presently used for polymer patterning by 1) adding liquid handling capabilities, 2) using less hazardous chemicals to simplify equipment design, and 3) investigating demolding strategies particularly for high-aspect ratio patterns.





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4. Experimental Section

Substrate Preparation: Mac-Imprint was performed on SOI wafers with 340 nm thick, p-type boron-doped device layer which had resistivity of 14–22 Ω cm and (100) crystal orientation. Prior to Mac-Imprint, arrays of 270 μm tall and 150 μm wide pillars spaced by 900 μm were fabricated on the SOI wafers by photolithography and deep-RIE in order to provide etching solution storage volume. The articulation on the necessity of SOI wafer pre-patterning and guidelines for the design of pillar size can be found in Supporting Information. Pre-patterned SOI wafers were thoroughly rinsed with acetone, isopropyl alcohol, and deionized (DI) water followed by RCA-1 cleaning and another DI water rinsing before Mac-Imprint.

Stamp Preparation: The fabrication of Mac-Imprint stamps consisted of four steps which are described below and detailed protocol of those can be found elsewhere. [64]

PDMS Replica Molding: At first, waveguide pattern was created on a Si master mold using e-beam lithography followed by RIE. Next, the pattern of the Si master mold was replicated onto PDMS according to the standard replica molding procedure. [65]

Soft Nanoimprint Lithography: After that, PDMS replica mold was used to pattern photoresist by means of nanoimprint lithography. To do so, $2.5\times2.5~{\rm cm^2}$ Si chips were first cleaned by RCA-1 solution followed by DI water rinsing. Next, clean Si chips were spin coated with 20 μm thick HF-resistant SU-8 2015 photoresist layer. Immediately after spin coating, the PDMS replica mold was placed on top of the photoresist layer with pattern facing down and pressed with the UV transparent glass slab, yielding 15 g cm $^{-2}$ of pressure. The UV curing was performed under 6 W UV bulb placed at 10 cm distance from the SU-8 surface for 2 h.

Catalytic Metal Sputtering: Upon UV curing, Si chips with patterned SU-8 layer were placed inside NSC-3000 magnetron sputter chamber at 20 cm distance from the sputtering targets. For the Mac-Imprint with solid catalyst, two layers of metal were deposited onto the stamp in the following order: 20 nm Cr (adhesion) and 80 nm Au (catalyst). For the Mac-Imprint with porous catalyst, three layers of metal were deposited onto the stamp in the following order: 20 nm Cr (adhesion), 50 nm Au (intermediate), and 375 nm Ag/Au alloy (precursor for porous catalyst).

Porosification of Catalyst: In order to create nanoporous catalysts, stamps with 375 nm Ag/Au alloy (51 at% of Ag) were subjected to selective dissolution of Ag by means of dealloying in far from equilibrium conditions. The dealloying was performed in aqueous solution of nitric acid (H₂O:HNO₃ = 1:1 by vol.) at a constant stirring rate of 100 rotations per minute following the protocol established in the work of Niauzorau et al. [33] The pore size of the catalyst was controlled by varying dealloying time and solution temperature. In particular, the np-Au with average pore sizes of 10 and 14 nm was produced at room temperature solution within 10 and 30 min, respectively, while the 27 nm average pore sizes were obtained at 65 °C temperature solution within 10 min. After the dealloying, a subset of porous catalytic stamps with average pore sizes of 27 nm was annealed in Ar environment at 250 °C for 1 h in order to increase average pore size to 42 nm through thermal coarsening.

Mac-Imprint Setup and Conditions: The Mac-Imprint set-up was composed of an electrochemical cell, a Teflon rod acting as a stamp holder, a load cell, and a vertical stage (see Figure S7, Supporting Information). The leveling between stamp and substrate was achieved during the assembly of the stamp to its holder. The stamp was placed on top of the substrate with its gold-coated side facing down and its back was attached to the stamp holder using a photocurable resin placed between them. The stamp and its holder were UV-cured using omnidirectional illumination (see Figure S7B, Supporting Information) ensuring that the stamp and substrate were parallel and aligned after assembly. After curing, the stamp could be retracted by the automated stage without loss of alignment. The SOI substrate was placed inside the electrochemical cell, which was then filled with the etching solution. The vertical stage brought a stamp holder with mounted stamp in plateto-plate contact with SOI substrate. The contact force of 22.24 N was developed within 0.1 s and maintained within $\pm 5\%$ of the set-point for

 10 ± 0.1 s. This allowed Mac-Imprint of the waveguide patterns to be reproducible provided the stamp-to-substrate alignment remained unaltered. After the imprinting, the stamp was retracted into home position and etching solution was aspirated from electrochemical cell. Further, SOI substrate was immediately flushed with excess amount of isopropyl alcohol to terminate the undercut of buried oxide layer. The total time of SOI substrate exposure to the etching solution was 70 s. Detailed description of Mac-Imprint setup and protocol can be found elsewhere. [64] It should be noted that ± 5 s variation in the Mac-Imprint total processing time (i.e., $\approx \! 70$ s) did not significantly affect the buried layer undercut depth (see Figure S8, Supporting Information).

The etching solution with ρ equal to 99.5% was prepared by mixing HF (48% by vol.) and H₂O₂ (30 % by vol.) in the 68:1 ratio (HF:H₂O₂; by vol.). Moreover, pure ethanol was added to the etching solution (4% of the etching solution volume) in order to improve solution's wettability. A fresh etching solution was mixed prior every Mac-Imprint operation. All chemicals were ACS grade, purchased from Sigma Aldrich.

Morphological, Structural, and Functional Characterization: Morphological properties of the Mac-Imprint stamps and imprinted waveguides were characterized by SEM using Philips XL-30 FEG SEM. All SEM images were acquired at 10 kV accelerating voltage and 130 pA beam current.

Imprint depth profiles were characterized by AFM using the Witec Alpha 300 RA+ system. AFM scans were acquired in tapping mode using NHCV-A Bruker probes with tip radius of 8 nm, spring constant of 40 N m $^{-1}$, and resonant frequency of 320 kHz. For AFM image acquired in Figure 4, the lateral resolution was determined by sampling distance which was set to be 234 and 39 nm in the x- and y-directions, respectively. The resolution of its height was set by the AFM instrumentation which, as per the vendor, was 0.5 nm.

The nanoscale defects of the imprinted waveguides and surroundings were characterized by confocal Raman microscopy using the same Witec system. The Raman signal was excited by 532 nm laser with the 0.1 mW output power. The Raman signal was acquired using 1800 g mm $^{-1}$ grating yielding 1 cm $^{-1}$ spectral resolution with the accumulation time of 0.2 s. Individual Raman mapping was performed over 4 \times 9 μm^2 area with total amount of 40 \times 90 data points.

The performance of the waveguide was characterized using near-IR (O-band) light from a tunable laser (Santec TSL-550), which was coupled onto the chip using through a polarization controller and tapered lensed fiber (OZ optics) and aligned using XYZ piezo controlled alignment stage (Thorlabs NanoMax). Fiber-to-chip alignment and successful waveguiding was verified by IR imaging both the top surface and output side-view of the chip with infrared cameras (Hamamatsu C2741). Waveguide mode simulation of the nanoimprinted silicon waveguide cross-section was performed at the wavelength 1310 nm using the finite difference eigenmode method (Ansys Lumerical MODE). The waveguide cross-sectional facet view IR imaging was modeled by convoluting the waveguide mode profile with the PSF of the NA = 0.42 imaging objective.

SEM Image Analysis: The quantification of: i) np-Au average pore size, ii) bottom roughness and iii) LER of the imprinted Si rib waveguides was performed through the analysis of the top-down SEM images using AQUAMI, [66] and Image] software (i.e., (i) and (ii), more details in Supporting Information and Figures S9 and S10, Supporting Information) as well as specifically written Python algorithm (i.e., (iii), more details in the Figure S11, Supporting Information). Note that in this work, bottom roughness of the imprinted waveguides was quantified using average sizes of Si protrusions. The distance between closest particles (either pores or protrusions in np-Au and imprinted Si, respectively) was called "nearest neighbor distance" and its analysis was performed using Image] software according to the algorithm published elsewhere (more details in the Figure S12, Supporting Information). [67]

Statistical Analysis: Analysis of AFM data was performed using Gwyddion software. Prior extracting imprint depth, the AFM data was leveled with respect to the non-imprinted top surface using "Mean Plane Subtraction" function. The individual imprint depth (Figure 4B, inset) was found from "Step-height" fitting function of "Critical dimension" module with error bar representing fitting error. The average imprint





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depth and its standard deviation (SD) were calculated based on 148 measurements along the AFM scan.

In the analysis of work by Liu et al., the average overetched distance and its SD was calculated based on nine reported measurements.

The analysis of the average size of np-Au pores, Si protrusions, and nearest neighbor distance was performed using AQUAMI and ImageJ software without any pre-processing of SEM images. The magnification was kept constant throughout the SEM images to maintain the same pixel size. Sample size for each measurement in this case was different and dependent on the amount of pores/protrusions present on the SEM image. Note that for a given sample the nearest neighbor distance for individual particle was found as an average distance to five nearest neighbors. The nearest neighbor distance of the sample was then calculated as average of all individual nearest neighbor distances. Data was presented as average \pm SD.

The analysis of the LER was performed by calculating the rootmean-square (RMS) of the waveguide's line edge profile obtained from high-magnification SEM images. The magnification was kept constant throughout the SEM images to maintain the same pixel size. Prior importing SEM images to the Python code, the bottom surface on the SEM images was thresholded and images were converted into .txt format using Image]. Waveguide line edge profiles were obtained on 2- μ m long waveguide segments using Canny edge detection algorithm with Gaussian filter size sigma equal to 2.6. The LER of individual line edge profile was calculated as an RMS of the pixel values multiplied by pixel size. The LER of the sample was then calculated as average of four independent measurements of different waveguide segments. Data were presented as average \pm SD.

The analysis of the Raman data was performed using Project FIVE software. Prior to extracting Raman signal position and FWHM, the signal was fitted using Lorentz function. The average peak position, FWHM, and its SD was calculated using data from the waveguide region only (i.e., excluding waveguide surroundings).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

B.A. is the co-founder and co-owner of a start-up called Nanobionics, LLC that works in the area of dental coatings. He has also recently served as consultant for NEWRY and New Mexico EPSCOR program.

Author Contributions

N.K., J.D.R., M.P., and B.A. conceived research. A.S., M.P., N.K., and B.A. designed research. A.S., S.N., and B.A. performed research. A.L.H and J.D.R. tested optical waveguiding. A.S. and B.A. wrote the manuscript. All the authors discussed the results and commented on the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

electrochemical nanoimprinting, metal-assisted chemical etching, optical metasurfaces, rib waveguides, silicon photonics, 3D nanophotonics

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