A 1.6pJ/b 65Gb/s Si-Dielectric-Waveguide based Multi-Mode Multi-Drop sub-THz Interconnect in 65nm CMOS

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Ever-increasing data generation and transmission demands have been driving great advancements in wireline communications from both electrical interconnect (EI) [1] and optical interconnect (OI) [2] for short- and long-distance scenarios, respectively. In the meter range, both EI and OI face great challenges: the lossy and bandwidth-limited channel is the bottleneck of EI; For OI, the features, such as the complex fabrication and high environment sensitivity, increase the power and cost budgets significantly, making it less economical for short-distance communications. To mitigate these issues, low-loss dielectric channel-based interconnects have been investigated and demonstrated [3-5]. However, they are all for point-to-point configurations, not suitable for multi-drop distributed architectures as shown in Fig.1. Thus, the unscalable feature limits their deployments. To address this important challenge, this paper adopts spatial multiplexers [6] and presents a Si dielectric waveguide (DWG) based multi-mode multi-drop sub-THz interconnect with great scalability for numerous ports and multi-dimensions. This approach is also more power and cost effective compared to OI due to the elimination of exotic materials and devices, such as lasers and OE/EO, and sophisticated fabrications. It only needs a low-cost and standard fabrication process with coarse alignment requirement.

Several key features contribute the high energy efficiency in the proposed architecture, as shown in Fig.1. First, the efficient and wide-band mode coupler and microstrip to waveguide transition (MWT), as well as the low-loss channel, relax the link budget, thus eliminating the power hungry high frequency power amplifiers. Second, the high isolation among different modes introduces minimum interference, thus allowing non-coherent detection at the receiver by removing power hungry clock generation and synthesizing. Third, the ultra-wide bandwidth of DWG enables ultra-high speed data transmission, which not only boosts bandwidth density but also allows using a simple and power efficient modulation scheme, such as OOK. Digital data is shaped by inverter driver in the TX and upconverted to 165 GHz by a passive switch-based OOK modulator. At the receiver, the RF signal is boosted by an integrated low noise amplifier (LNA) before feeding an envelope detector (ED) to recover the data.

The paper presents the first mode division multiplexing (MDM) based multi-drop sub-THz interconnect prototype with three modes, i.e. E_{11}^{y}, E_{21}^{y} and E_{31}^{y}, through a single Si DWG as shown in Fig. 2. The multi-drop DWG builds three individual channelization and is packaged on a high-Q quartz board together with CMOS TX/RX chipsets. Both DWG and quartz board are fabricated in-house with a standard micro-manufacturing process and assembled with a flip-chip bonder. The MWT, fabricated on a quartz board, converts the quasi-TEM signal in microstrip line (MSL) to the E_{11}^{y} mode signal in Si DWG. After that, the fundamental E_{11}^{y} signal can be further converted to higher-order modes, such as E_{21}^{y} or E_{31}^{y}, by mode couplers. Signals in the three modes are isolated from each other in principle, therefore can propagate together along the common DWG. On the receiver side, each mode RF signal is extracted by the corresponding coupler. Fig. 2 (d) presents the simulated E field around the couplers to show the successful mode conversion. Mode coupler is designed based on the phase matching theory such that mode coupling occurs when their propagation constant β in different DWGs are equal at a given frequency. The tapered MWT on the quartz board matches the β of quasi-TEM in MSL and E_{11}^{y} mode in DWG over 120~200GHz, with a typical loss of 1.8dB, so it is also identified as a mode coupler.

The other two mode couplers are waveguide mode couplers, which are realized by the EM field overlap and phase matching. The effective refractive index for different modes, as shown in Fig. 3 (a), changes with the DWG width W, so as β. Therefore, the prototype optimizes W to adjust β for mode coupling. Maximizing the coupling efficiency η not only reduces the loss, but also decreases the crosstalk. η is determined by the propagation constant difference $\Delta\beta$ and coupling coefficient κ, and it can be optimized by the coupler length, as shown in Fig. 3 (b). Tapered structures are also employed to improve the performance, e.g., the tapered coupler is optimized to enhance the coupling efficiency; the tip-end opens a radiation path for the residual EM energy, thus reduces reflection and crosstalk.

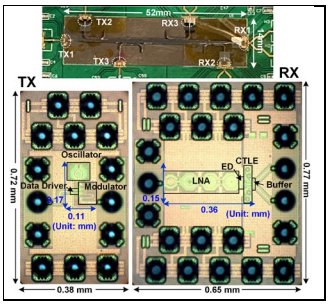

Fig. 4 shows the proposed high energy efficiency active subsystem, i.e., the OOK TX and direct detection RX. The TX consists of an inverter-based data driver, a cross-coupled oscillator as the 165GHz carrier generator and a multi-stage passive switch-based OOK modulator. TL_1 and TL_2 are utilized to adjust the signal phase and the transformer is to match the optimum loading. The TX output power is -3.2dBm with the DC power consumption of 11.5mW. The RX consists of a LNA, ED, continuous time linear equalizer (CTLE) and a buffer. Frequency-insensitive direct detection requires wide bandwidth and suffers from poor noise performance. To deal with this issue, a 3-stage LNA is employed to suppress the noise and enhance the sensitivity. A three-coil neutralization transformer is proposed for the first common-gate stage that aims at low noise figure (NF) and broad bandwidth at sub-THz. The following two common-source stages are neutralized by capacitors. It provides 24dB voltage gain with 7dB NF over 142~183 GHz. The input-referred noise equivalent power is improved from $15pW/\sqrt{Hz}$ to $100fW/\sqrt{Hz}$. The LNA consumes 15mW with a supply voltage of 1V. The CTLE compensates the voltage gain drop at high frequencies and increases the bandwidth from 14.9GHz to 33.6GHz.

The TX and RX chips are fabricated in a 65nm CMOS technology with the size of 0.38x0.72mm^2 and 0.65x.0.77mm^2, including the pads. The DWG is fabricated from a 4-inch high-resistivity Si wafer, thus has a limit of the length of 5.2cm. The measured back-to-back transition loss of the DWG including two MWTs is about 5dB within a 3dB bandwidth of 60, 35 and 25GHz for E_{11}^{y}, E_{21}^{y} and E_{31}^{y} modes, respectively. The measured TX output power of -3.1dBm and RX input matching are also shown in Fig.5. A PRBS pattern of 2^{21} was generated to test the three modes of the multi-drop interconnect system simultaneously with an arbitrary waveform generator (AWG) and oscilloscope. In Fig 6 (a), the measured data rates are 24, 22 and 19Gb/s for E_{11}^{y}, E_{21}^{y} and E_{31}^{y} modes respectively with the BER better than 10^{-12}. The demonstrated aggregate data rate of the three channels is 65Gb/s with the energy efficiency of 1.6pJ/b. Fig. 6 (c) compares with state-of-the-art (SOA) DWG based interconnects. Our approach achieves the best energy efficiency with the capability to support multi-drop and large scalability. Furthermore, the architecture and design approach can be readily extended to the meter range due to the ultra-low loss channel material.

The paper presents a novel multi-mode multi-drop DWG based interconnect. To the author's knowledge, this is the first demonstration of more than three channel simultaneous transmission. It can readily scale to more modes to support more logic channels per physical link and extend to multi-dimension interconnect systems. Besides, with more advanced semiconductor technologies for active circuits, the data rate per channel can be further increased. Therefore, we believe that the demonstrated multi-mode multi-drop sub-THz interconnect architecture opens a new path with high potentials to address the challenging meter range wireline communication scenarios.

References:

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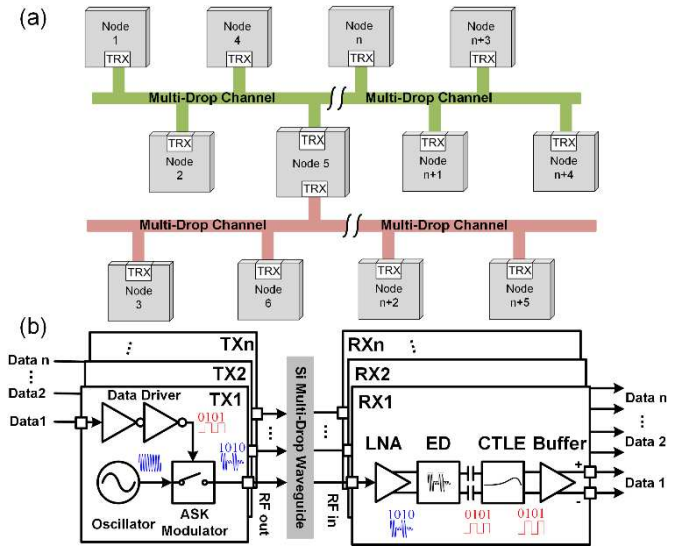


Fig. 1. (a) Networks require multi-drop channels, and (b) the system diagram of the multi-mode multi-drop sub-THz interconnect.

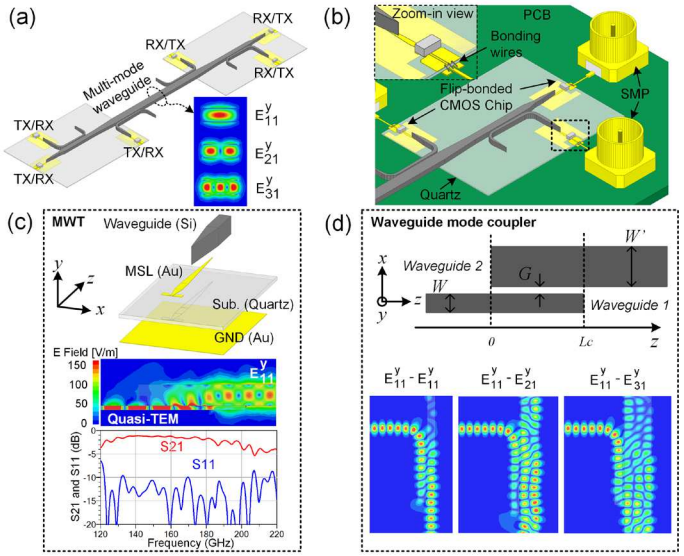


Fig. 2. (a) Architecture and (b) package of the multi-mode multi-drop sub-THz interconnect. (c) MWT and (d) waveguide mode coupler.

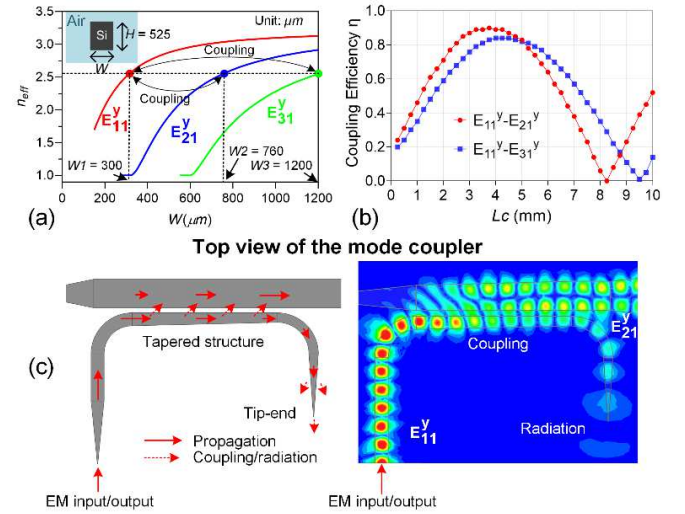


Fig. 3. (a) Simulated effective refractive index n_{eff} at 165GHz versus W. (b) The simulated coupling efficiency versus the coupler length. (c) The mode coupler design and simulated E field.

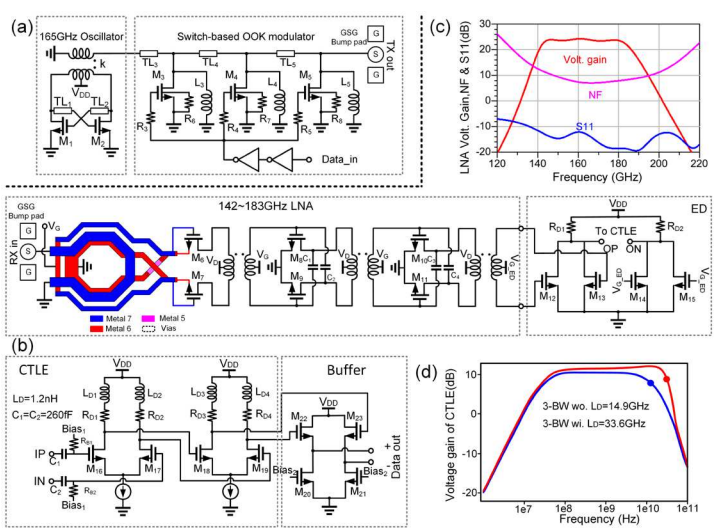


Fig. 4. Schematics of (a) the oscillator, OOK modulator in TX, and (b) the LNA, ED, CTLE and buffer in RX. Simulated performance of (c) the neutralized CG LNA and (d) the inductor based CTLE.

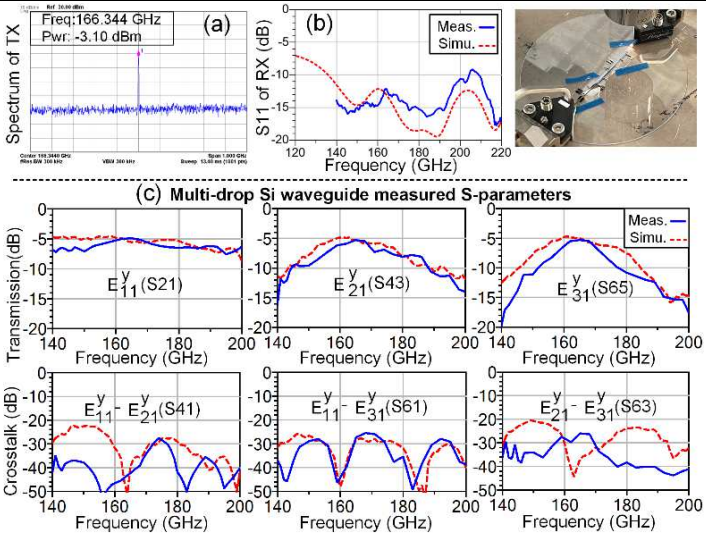
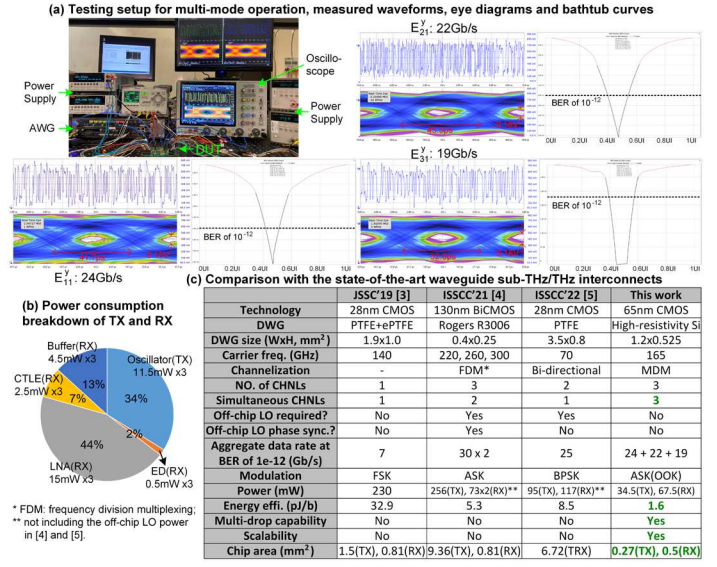


Fig. 5. (a) Measured TX and output power and spectrum, (b) measured S11 of the LNA and (c) measured S-parameters of the multi-drop DWG.



(c) Comparison with the state-of-the-art waveguide sub-THz/THz interconnects

	JSSC'19 [3]	ISSCC'21 [4]	ISSCC'22 [5]	This work
Technology	28nm CMOS	130nm BiCMOS	28nm CMOS	65nm CMOS
DWG	PTFE+ePTFE	Rogers R3006	PTFE	High-resistivity Si
DWG size (WxH, mm²)	1.9x1.0	0.4x0.25	3.5x0.8	1.2x0.525
Carrier freq. (GHz)	140	220, 260, 300	70	165
Channelization	-	FDM*	Bi-directional	MDM
NO. of CHNLs	1	3	2	3
Simultaneous CHNLs	1	2	1	3
Off-chip LO required?	No	Yes	Yes	No
Off-chip LO phase sync.?	No	Yes	No	No
Aggregate data rate at BER of 1e-12 (Gb/s)	7	30 x 2	25	24 + 22 + 19
Modulation	FSK	ASK	BPSK	ASK(OOK)
Power (mW)	230	256(TX), 73x2(RX)**	95(TX), 117(RX)**	34.5(TX), 67.5(RX)
Energy effi. (pJ/b)	32.9	5.3	8.5	1.6
Multi-drop capability	No	No	No	Yes
Scalability	No	No	No	Yes
Chip area (mm²)	1.5(TX), 0.81(RX)	9.36(TX), 0.81(RX)	6.72(TRX)	0.27(TX), 0.5(RX)

Fig. 6. (a)Testing setup and measured data rates and eye diagrams, (b) breakdown of power consumption, and (c) SOA comparison.