Imbalance Compensation for SVPWM-Controlled Four-switch Three-phase Inverters

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***Abstract*— Four-switch three-phase (FSTP) inverters have been investigated as low-cost alternatives to traditional six-switch three-phase (SSTP) inverters for a variety of applications. However, voltage fluctuations at the DC link center tap can significantly degrade the performance of FSTP inverters, which leads to an imbalance in the inverter output. By analyzing the vector trajectory of the output voltage in FSTP inverters, this paper characterizes the imbalance and proposes an adaptive SVPWM algorithm to correct it. The method uses correction factors to adjust control parameters according to the real-time voltage at the DC link center tap. The proposed method is thoroughly discussed, both in terms of theoretical analysis and simulation verification. Experiment results are also presented to further validate the proposed method. As demonstrated by the results, the compensation method is effective even in the presence of substantial voltage ripples at the center tap.**

Keywords—Four-switch three-phase inverter, imbalance compensation, SVPWM, input capacitance

I. INTRODUCTION

Unlike traditional six-switch three-phase (SSTP) inverters, four-switch three-phase (FSTP) inverters have two legs instead of three legs and inherent cost savings due to the reduced number of switches, freewheeling diodes, gate drive circuits, and so on. Thus, as low-cost alternatives to SSTP inverters, FSTP inverters have been studied in a variety of applications [1-11]. However, FSTP inverters are rarely used, because of their susceptibility to imbalances. One of the phase currents in FSTP inverters is carried by the input filter capacitors through the center tap of the DC link. This inevitably causes a sinusoidal voltage ripple at the center tap during capacitor charging and discharging, which further causes an imbalance in the inverters. Large capacitors are often used to stabilize the center tap voltage. Even so, this does not completely solve the problem and results in a bulky system at a higher cost. Some studies have been done in the literature to address this issue [7-14]. There are mainly two categories of methods for mitigating the imbalance, one involves directly regulating the inverter output, and the other involves offsetting the voltage ripple at the center tap. In this paper, a new method based on vector analysis is presented to analyze and comprehend the imbalance in FSTP inverters. Following that, an adaptive Space Vector PWM (SVPWM) is proposed to compensate for the imbalance by adjusting the modulation index of SVPWM according to the real-time voltage at the DC link center tap. Additionally, unified control equations are obtained in this work, in contrast to other techniques where the calculations of control parameters vary in different space vector sections. This significantly reduces the complexity of FSTP inverter control and implementation.

The paper is organized as follows: Section II discusses SVPWM control of FSTP inverters without compensation. Section III focuses on imbalance compensation. Based on the mathematical analysis of the imbalance, a novel compensation method is proposed. Correction factors are established to address the imbalance issue. They are formulated as functions of the control parameters and the ripple voltage at the DC link center tap. Simulations are also used to verify the proposed method. Further experimental validation is presented in Section IV. The final section summarizes the main finding of this work.

II. SVPWM CONTROL OF FSTP INVERTER

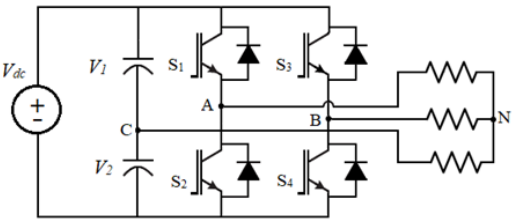

Fig. 1. FSTP inverter topology

Fig. 1 shows the topology of an FSTP inverter. Studying the circuit, the phase output voltages of the inverter can be derived as (1), where S_1 and S_3 are the state variables of the high-side switches of the inverter and their values are "1" for "ON state" and "0" for "OFF state," respectively.

$$\begin{aligned} V_{AN} &= (4S_1 - 2S_3 - 1)\frac{V_{dc}}{6} \\ V_{BN} &= (4S_3 - 2S_1 - 1)\frac{V_{dc}}{6} \\ V_{CN} &= (1 - S_1 - S_3)\frac{V_{dc}}{3} \end{aligned} \tag{1}$$

Using power-invariant Clarke transformation, the three-phase voltage in (1) can be transformed into a vector, **V**, in the $\alpha\beta$-plane as shown in (2) and $\mathbf{V} = V_\alpha + jV_\beta$.

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$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}}\left(S_1 - \frac{1}{2}S_3 - \frac{1}{4}\right) \\ \sqrt{\frac{1}{2}}\left(S_3 - \frac{1}{2}\right) \end{bmatrix} V_{dc} \quad (2)$$

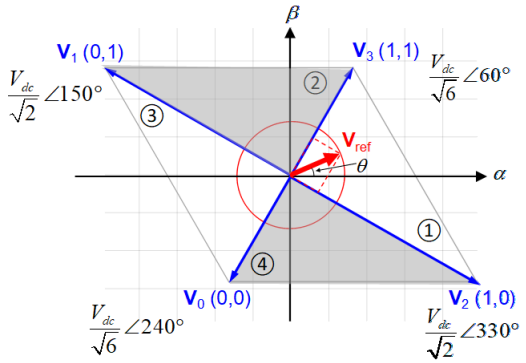


Fig. 2. SVPWM Space vector digram for FSTP inverters

According to the four combinations of the two state variables, four different space vectors ($\mathbf{V}_i$, where i = 0, 1, 2, 3) can be created as shown in Fig. 2. The $\alpha\beta$-plane is divided into four sections (① - ④) by the four space vectors. A zero vector can be created by summing any one of the two pairs of space vectors, $\mathbf{V}_0$ and $\mathbf{V}_3$, or $\mathbf{V}_1$ and $\mathbf{V}_2$. The two space vectors in each section, along with a zero vector, are modulated so that their time-weighted average is equal to a reference vector, which represents the desired output voltage ($\mathbf{V}_{ref}$ in Fig. 2.). By choosing the switching sequence as shown in Fig. 3, unified equations for the switch duty ratios can be found as shown in (3), which are applicable to all the sections rather than each individual section. This is one of the main advantages of the SVPWM algorithm used in this work. More details on this control method can be found in [15, 16].

$$D_{S_1} = \frac{1}{2}\left[1 + m\sin(\theta + 60°)\right],\ D_{S_3} = \frac{1}{2}\left(1 + m\sin\theta\right), \quad (3)$$

where m is amplitude modulation raito.

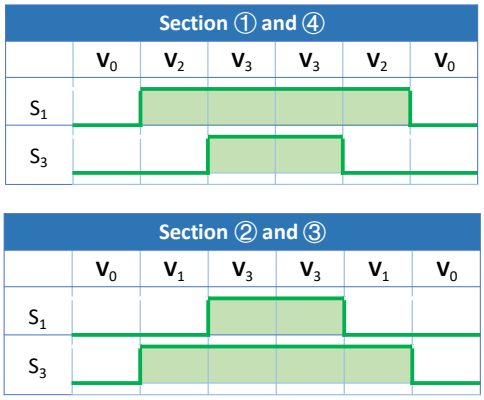


Fig. 3. SVPWM Switching Sequence

If the output voltage vector produced by SVPWM originates at the origin of the $\alpha\beta$ - plane, for example, $\mathbf{V}_{ref}$ in Fig. 2, the three-phase output voltage in the inverter is balanced. This is true only when the DC-link voltage is evenly distributed across the two input capacitors, i.e., V_1=V_2 in Fig. 1. As mentioned earlier, in reality, the two capacitor voltages are never equal. As a result, an imbalance appears in the inverter, which can cause problems in a variety of applications, such as pulsating torque in motor drives [9]. Increasing the capacitance of the input capacitors can reduce the voltage ripple at the center tap (point C in Fig. 1) and so mitigate the imbalance. However, its effectiveness is very limited due to the size and cost limits of the capacitors, especially when the load current is high. Thus, mitigating the DC-link voltage fluctuation is insufficient to fundamentally solve the problem; solutions that can counteract the impact of the fluctuation are required.

III. Imbalance Compensation

A. *Inverter output voltage when there is a voltage ripple at the DC-link center tap*

In order to mitigate the impact of the voltage ripple at the DC link center tap in an FSTP inverter, the inverter output voltage is analyzed while taking the voltage ripple into account. If V_1 and V_2 are assumed to be $V_{dc}/2+\Delta V$ and $V_{dc}/2-\Delta V$ respectively, the phase output voltages can be represented by (4). When compared to that in (1), each phase voltage in (4) contains an additional component as a result of the voltage ripple, ΔV. Accordingly, after the Clarke transformation is applied to (4), the output voltage vector, $\mathbf{V'}_{ref}$, and space vectors, $\mathbf{V'}_i$, are all changed by a vector, $\Delta\mathbf{V}$, as indicated in (5)-(7).

$$\begin{aligned} V'_{AN} &= \left(4S_1 - 2S_3 - 1\right)\frac{V_{dc}}{6} + \frac{\Delta V}{3} = V_{AN} + \frac{\Delta V}{3} \\ V'_{BN} &= \left(4S_3 - 2S_1 - 1\right)\frac{V_{dc}}{6} + \frac{\Delta V}{3} = V_{BN} + \frac{\Delta V}{3} \\ V'_{CN} &= \left(1 - S_1 - S_3\right)\frac{V_{dc}}{3} - \frac{2\Delta V}{3} = V_{CN} - \frac{2\Delta V}{3} \end{aligned} \quad (4)$$

$$\begin{aligned} \begin{bmatrix} V'_\alpha \\ V'_\beta \end{bmatrix} &= \begin{bmatrix} \sqrt{\frac{2}{3}}\left(S_1 - \frac{1}{2}S_3 - \frac{1}{4}\right) \\ \sqrt{\frac{1}{2}}\left(S_3 - \frac{1}{2}\right) \end{bmatrix} V_{dc} + \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} \Delta V \\ &= \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} + \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} \Delta V \end{aligned} \quad (5)$$

$$\mathbf{V'}_{ref} = V'_\alpha + jV'_\beta = \mathbf{V}_{ref} + \Delta\mathbf{V}, \text{ where } \Delta\mathbf{V} = \sqrt{\frac{2}{3}}\Delta V \angle 60° \quad (6)$$

$$\mathbf{V'}_i = \mathbf{V}_i + \Delta\mathbf{V}, \text{ where } i = 0, 1, 2, 3 \quad (7)$$

Fig. 4 plots $\mathbf{V'}_{ref}$, and $\mathbf{V'}_i$, in $\alpha\beta$ - plane in contrast to those space vectors under zero ripple voltage ($\mathbf{V}_i$ in Fig. 2). It can be

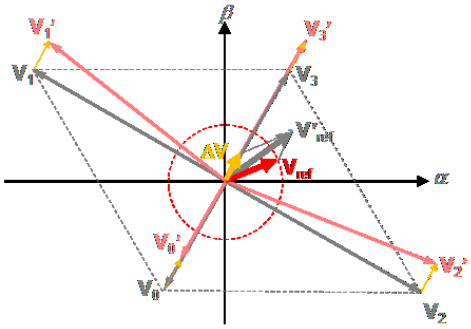


Fig. 4. Space vector diagram in $\alpha\beta$ - plane without compensation when ΔV presents at the DC link center tap

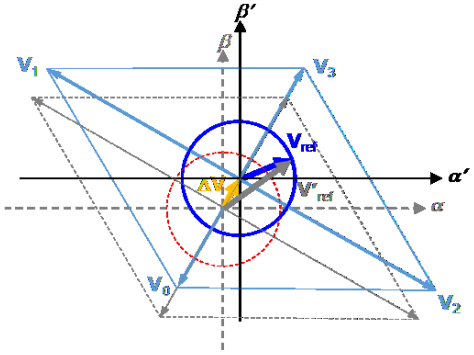


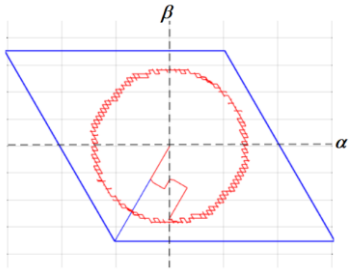
Fig. 5. Coordinate change from $\alpha\beta$ - plane to $\alpha'\beta'$ - plane

seen that implementing the control based on (3) will produce the output voltage, $\mathbf{V'_{ref}}$, rather than the desired output voltage $\mathbf{V_{ref}}$.

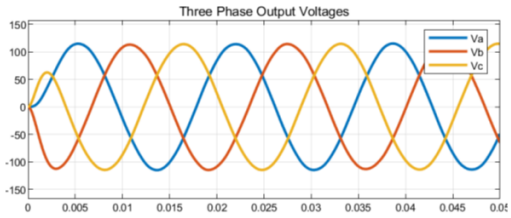
In Fig. 5, a $\alpha'\beta'$ - plane is created by moving the origin of the $\alpha\beta$ - plane to $\mathbf{\Delta V}$. In the $\alpha'\beta'$ - plane, the space vectors, $\mathbf{V'}_i$, have the same values as $\mathbf{V}_i$ in the $\alpha\beta$ - plane. Using $\mathbf{V'}_i$ and (3) to modulate output voltage will result in a similar circular output trajectory as shown in Fig. 2, but with a center at $\mathbf{\Delta V}$ (see Fig. 5). Thus, the effect of $\mathbf{\Delta V}$ is equivalent to introducing a displacement to the $\alpha\beta$ - plane and the implementation of the original SVPWM control in (3) produces a circular output vector trajectory centered at $\mathbf{\Delta V}$. The magnitude of the output vector in the $\alpha\beta$ - plane is no longer constant since its center is not at the origin of the $\alpha\beta$ - plane, and therefore the voltages in different phases become unbalanced. This theory can be verified by simulations. The simulation results for an FSTP inverter with 500 V DC input and 200 V peak line-line output are shown in Figs. 6 and 7. As seen in Fig. 6, the output phase voltages are balanced when the center tap voltage is constant at 250 V. Its output voltage vector trajectory is a circle with its center at the origin. While in Fig. 7, the center tap voltage is shifted by 50 V (ΔV). When the same control approach is used, unbalanced output phase voltages are observed, and the vector trajectory is still circular but with a center offset from the origin by $\mathbf{\Delta V}$.

B. Compensation

To obtain balanced output voltages, the center of the output vector trajectory in Fig. 7 (a) must be moved back to the origin of the $\alpha\beta$ - plane. A compensation vector, $-\mathbf{\Delta V}$, can be added to the reference vector, $\mathbf{V'_{ref}}$. As seen in Fig. 8, this brings $\mathbf{V'_{ref}}$

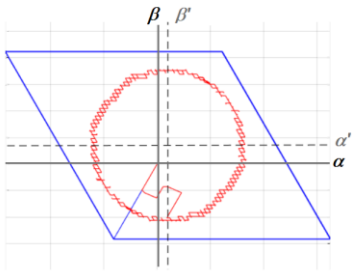


(a) The vector trajectory of the output voltage

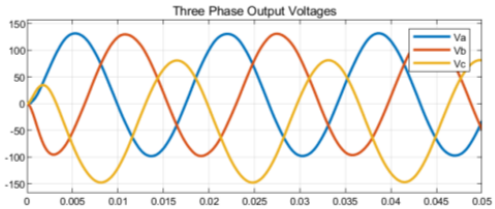


(b) The fundamental output phase voltages

Fig. 6. The FSTP inverter output votage trajectory and waveforms when the voltage ripple at the DC link is zero.



(a) The vector trajectory of the output voltage



(b) The fundamental output phase voltages

Fig. 7. The FSTP inverter output votage trajectory and waveforms when the voltage ripple at the DC link is 50 V

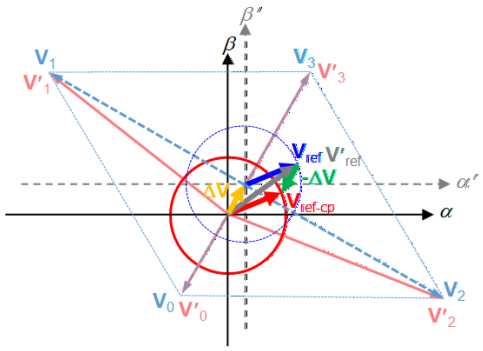
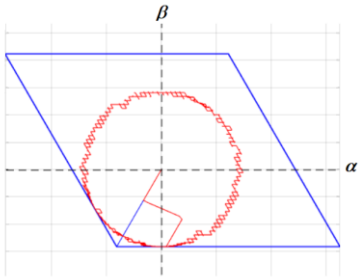


Fig. 8. Space vector diagram with compensation when ΔV presents at the DC link center tap

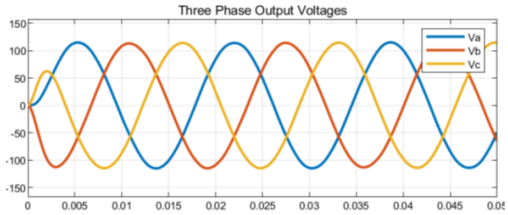
back to $\mathbf{V}_{\mathbf{ref\text{-}cp}}$ which is equal to $\mathbf{V}_{\mathbf{ref}}$, the refer vector without accounting for the voltage ripple. Therefore, instead of $\mathbf{V}_{\mathbf{ref}}$, $\mathbf{V}_{\mathbf{ref}}$ $-\Delta\mathbf{V}$ should be used as the reference representing the desired output voltage while deriving the control equations in (3). As a result, new control equations can be obtained, which are different from those in (3). To account for the differences, two correction factors, A_m and B_θ, are introduced and can be calculated by (8). When implementing the compensation, m and θ in (3) should be replaced by $A_m \cdot m$ and $B_\theta \cdot \theta$, respectively.

$$A_m = \sqrt{1 + \frac{16\Delta V^2}{3m^2 V_{dc}^2} - \frac{8\Delta V}{\sqrt{3} m V_{dc}} \sin(\theta + 30°)}$$
$$B_\theta = \tan^{-1}\left(\frac{\sin\theta - 2\Delta V / m V_{dc}}{\cos\theta - 2\Delta V / \sqrt{3} m V_{dc}} \right) \quad (8)$$

This compensation method has been applied to the same FSTP inverter simulated in section III. A. Fig. 9 demonstrates the simulation results with the compensation when the voltage ripple at the DC link center tap is 50V. As seen in Fig. 9 (a), the center of the output vector trajectory has been moved back to the origin of the $\alpha\beta$- plane and the output voltages become balanced again as seen in Fig. 9 (b).



(a) The vector trajectory of the output voltage

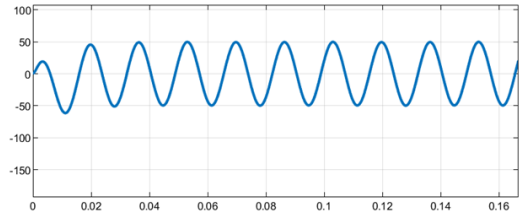


(b) The fundamental output phase voltages

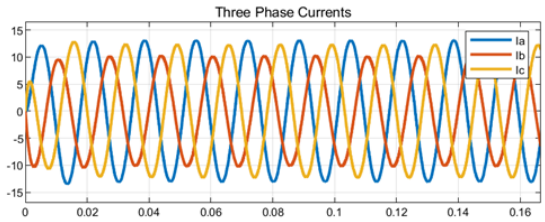
Fig. 9. The FSTP inverter output votage trajectory and waveforms with compensation when the voltage ripple at the DC link is 50 V

C. *Verification and discussions*

The voltage ripple at the DC link center tap in an FSTP inverter is sinusoidal as shown in Fig. 10 (a). The compensation method provided in the previous section is still applicable if the correction factors are adapted to the instantaneous value of the voltage ripple. Simulations have been conducted on an FSTP inverter operating from 500 V DC input and outputting 200 V (line-line peak) to supply an inductive load with a power factor of 0.9. The capacitance of the input capacitors in the inverter is 330 μF. The simulation results are shown in Figs. 10 and 11. Without compensation, the output phase currents in the inverter

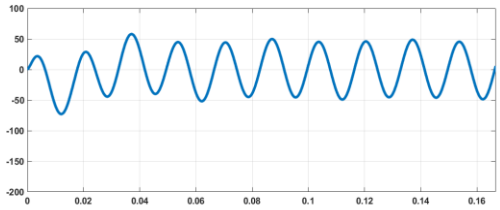


(a) The voltage ripple at the DC link center tap

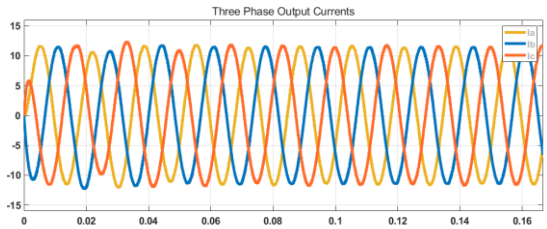


(b) Output phase currents

Fig. 10. The simulation results of the FSTP inverter without compensation



(a) The voltage ripple at the DC link center tap



(b) Output phase currents

Fig. 11. The simulation results of the FSTP inverter with the compensation

are unbalanced, as seen in Fig. 10 (b). The maximum phase current variation is around 13.5%. After implementing the proposed compensation, the output currents become balanced as shown in Fig. 11 (b). Additionally, the compensation does not eliminate the voltage ripple as illustrated in Fig. 11 (a).

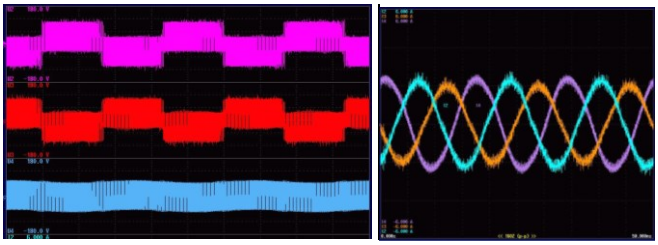
Although increasing the input capacitance can mitigate the imbalance, it takes a capacitance increase of more than tenfold to attain the same level of effectiveness. This is nearly infeasible, especially when the DC link voltage is high. Furthermore, the greater the load current in FSTP inverters, the more voltage ripple there is at the center tap, and then the worse the imbalance is. Thus, imbalance compensation is a must for FSTP inverters in such situations.

IV. EXPERIMENTS

To further validate the simulation results, experiments have been conducted using a 600V/30A IGBT/FRD IPM module.

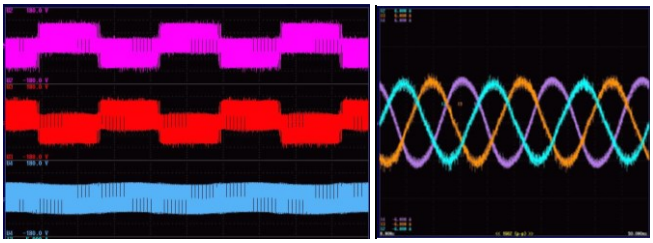
The module is composed of three half-bridge legs. When two legs are used, the module works as an FSTP inverter. The FSTP inverter is controlled by a TMS320F288335 microprocessor implementing the proposed SVPWM control with or without compensation.

The experimental results of the inverter when driving a three-phase inductive load are shown in Figs. 12-15. As seen in



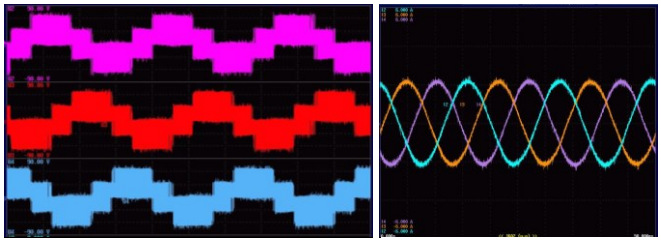
(a) The phase output voltage (b) The phase output currents

Fig. 12. The experimental results of the FSTP inverter without compensation



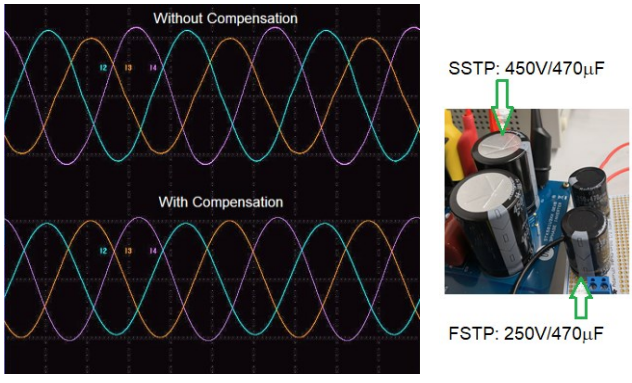
(a) The phase output voltage (b) The phase output currents

Fig. 13. The experimental results of the FSTP inverter with compensation



(a) The phase output voltage (b) The phase output currents

Fig. 14. The experimental results of the SSTP inverter



(a) Fundamental output current (b) Capacitors

Fig. 15. The FSTP inverter waveforms after filtering and capacitors

Fig. 12, without compensation, the output currents of the FSTP inverter are unbalanced. The phase C current is relatively lower compared to the other two phases. The maximum phase current variation is about 10.5%. After the compensation, as shown in Fig. 13 (b), there is no significant current imbalance in the FSTP inverter. Its output currents are comparable to those of the SSTP inverter shown in Fig. 14 (b), which has the same design and has been tested under the same conditions. Fig. 15 (a) shows the inverter output currents after filtering, which illustrates more clearly that the imbalance in the output is effectively corrected.

The FSTP inverter is more efficient than the SSTP inverter in general. Its efficiency is not significantly impacted by the compensation. As shown in Table I, the efficiency improvement is greater when the modulation index is relatively high or low or when the load is light. The maximum efficiency increase is about 3.8%, which is obtained when the modulation index is 0.2. The maximum loss reduction is around 40.7%, which is obtained when the modulation index is 0.8.

TABLE I. EFFICIENCY OF FSTP AND SSTP INVERTERS

Modulation Index (*m*)	**0.8**	**0.5**	**0.2**
FSTP	95.89%	93.84%	85.32%
FSTP with compensation	95.61%	93.61%	84.90%
SSTP	93.07%	93.13%	81.52%

Test conditions: output voltage 50V, switching frequency 10 kHz, the same RL load, PF=0.94.

In addition, the voltage rating of the input capacitors in the FSTP inverter is reduced by half due to the series connection, which significantly reduces the size and cost of DC link capacitors. The capacitors used in the SSTP inverter and the FSTP inverter are presented in Fig. 15 (b). Smaller capacitors and fewer switches make the FSTP inverter much more compact compared to the SSTP inverter.

V. CONCLUSIONS

This paper proposes an adaptive SVPWM algorithm for FSTP inverters that can correct the imbalance caused by the voltage ripple at the DC link center tap. Explicit and unified SVPWM control equations have been derived for FSTP inverters, which remove the barriers between different space vector sections in the modulation and greatly simplify the control and implementation of FSTP inverters. The imbalance compensation of these inverters is implemented by using correction factors that are adapted to the voltage ripple at the DC link center tap. Comprehensive theory and simulation studies are presented and experiments have been conducted to further validate the proposed method. As seen from the results, with the proposed compensation, the FSTP inverters can function just as well as they would if the voltage ripple did not exist. On the other hand, compensating an FSTP inverter enables the use of smaller input capacitors, which leads to a further reduction in size and weight of the inverter.

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