A Highly Efficient 165-GHz 4FSK 17-Gb/s Transceiver System With Frequency Overlapping Architecture in 65-nm CMOS

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***Abstract*— A new four-frequency-shift keying (4FSK) transceiver (TRX) at 145–185-GHz operation frequency is presented. The proposed non-coherent TRX is a fully integrated bit-in–bit-out communication system without the need for separate modulators/demodulators (modems). The transmitter (TX) core includes only one voltage-controlled oscillator (VCO), which can generate four different frequencies based on the two parallel streams of binary data at its input. The receiver (RX) with a frequency overlapping architecture demodulates the 4FSK signal and recovers the two parallel streams of binary data. Both the TX and the RX are designed and fabricated in a standard 65-nm CMOS process. The TX and RX consume 62- and 120-mW power, respectively. The highest achieved data rate is 17 Gb/s at an 18-cm link distance with 10.7-pJ/bit energy efficiency.**

***Index Terms*— 165 GHz, CMOS, data rate, energy efficiency, frequency-shift keying (FSK), millimeter wave (mm-wave), modulation, multi-Gb/s, transceiver (TRX).**

I. Introduction

IMPLEMENTATION of fully integrated millimeter-wave (mm-wave) and sub-terahertz (THz) wireless communication systems is of great interest [1], [2]. The targeted applications for such systems are 4K video streaming, wireless augmented reality (AR), virtual reality (VR), the Internet of Things (IoT), 5G and future 6G communication systems, wireless data centers, and sensors. These applications often require multi-Gb/s data rates, sufficient range, and high energy efficiency. Large available bandwidths in mm-wave and sub-THz frequency bands can be used to achieve multi-Gb/s data rates. In addition, a short wavelength at these frequencies allows for smaller circuit and antenna sizes. Despite the advantages, several challenges exist in utilizing high-frequency bands in designing wireless communication transceivers (TRXs). The limited maximum oscillation frequency $f_{\max}$ of the transistors, low quality factor of varactors, lossy passive elements, and high path loss are among the challenges.

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Efforts have been concentrated on implementing multi-Gb/s data rate TRXs during the past few years [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29]. State-of-the-art multi-Gb/s TRXs mostly employ digital modulation schemes, including phase shift keying (PSK), quadrature amplitude modulation (QAM), and ON–OFF keying (OOK). PSK and QAM modulations are widely used in modern multi-Gb/s TRXs [30], [31], [32], [33], [34], [35], [36], [37] because of their spectral efficiency. The reported PSK/QAM TRXs are spectrally efficient but require coherent TRX architectures, which increases the complexity and power consumption of the systems by demanding accurate synthesizers and I/Q mixers. In addition, in a fully integrated PSK/QAM communication system, an on-chip modem is required, which adds to the complexity and power consumption. These modems are largely analog-to-digital converters (ADC) and digital-to-analog converters (DAC), which are challenging to design at multi-Gb/s data rates. Finally, amplitude changes in the QAM modulation force the power amplifiers to operate in the back-off region, significantly reducing their efficiency.

The OOK TRXs do not require modems, which makes them a good choice for low-power designs [38], [39], [40], [41]. Furthermore, it provides a simple and direct radio frequency (RF) modulation and demodulation scheme, which simplifies the TRX architecture significantly. Nevertheless, despite all the aforementioned advantages of the OOK modulation, it can only provide 1 bit/symbol, limiting the data rate considerably.

Due to these shortcomings, there needs to be a new approach to overcome the challenges and achieve tens of Gb/s data rate with low-complexity hardware and low power consumption in mm-wave TRXs. As such, we focus on utilizing a frequency-shift keying (FSK) modulation scheme to reach such a goal. Due to the scarcity of bandwidth in the RF and microwave frequency bands, the FSK modulation is rarely used in modern high data rate RF TRXs [42]. Nevertheless, large available bandwidths exist at mm-wave and sub-THz bands, which can be utilized to implement an energy-efficient multi-Gb/s communication system. Theoretically, FSK shows better performance in terms of energy efficiency and bit error rate (BER) than PSK/QAM. As such, spectral efficiency can be traded off with energy efficiency and BER performance at mm-wave frequencies using the FSK modulation [42]. In addition, FSK can be implemented non-coherently without

TABLE I
SPECTRAL EFFICIENCY OF THE DIGITAL MODULATION SCHEMES

Modulation	Bandwidth	Spectral Efficiency (bits/s/Hz)	Eb/N0 (dB) (for BER=1E-12)
BPSK	f_b	1	13.8
QPSK	$f_b/2$	2	13.8
QAM	$f_b/2$	2	13.8
8PSK	$f_b/3$	3	17.4
8QAM	$f_b/3$	3	15.8
16PSK	$f_b/4$	4	22
16QAM	$f_b/4$	4	18
FSK	$3f_b$	0.33	17.2
4FSK	$2.5f_b$	0.40	14.5
8FSK	$3f_b$	0.33	12.8
16FSK	$4.25f_b$	0.23	11.3

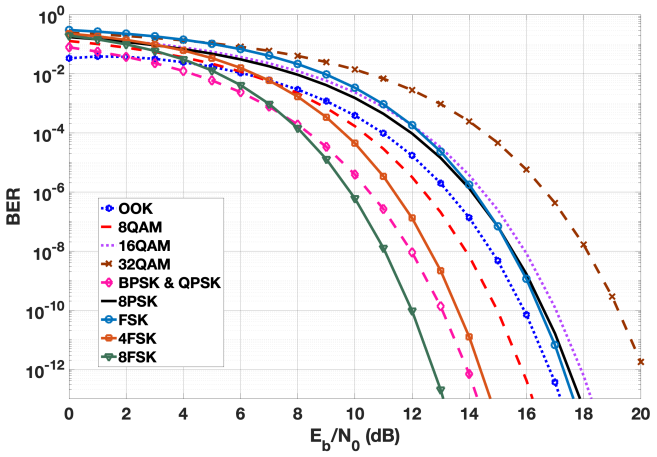


Fig. 1. BER performance versus E_b/N_0 for different modulation schemes.

a need for a separate modem. This eliminates the need for accurate synthesizer, carrier recovery, I/Q mixer, and high-speed data converters, and thus, the complexity and power consumption of the communication system can be further reduced. Moreover, FSK is a constant envelope modulation, and as a result, it can take advantage of high efficiency and non-linear power amplifiers in implementation. Finally, compared to traditional OOK, FSK can transmit more than 1 bit/symbol enabling higher data rate systems.

To the best of the author's knowledge, the fastest wireless FSK transmitter (TX) is presented in [43], which can transmit 10 Gb/s. The fastest non-wireless FSK TRX is also presented in [44] operating at 17.7-Gb/s data rate over a polymer microwave fiber link. In this article, we propose a new four-frequency-shift keying (4FSK) TX and receiver (RX) architecture to implement a 17-Gb/s communication system at 145–185 GHz consuming only 182 mW in a 65-nm CMOS. This novel non-coherent 4FSK architecture removes the need for separate modems reducing power consumption and boosting energy efficiency. A new approach is presented to divide the input signal at the RX into two parallel paths instead of four, reducing the power consumption and chip area even further. To the best of our knowledge, the proposed design is the first multi-Gb/s wireless TRX based on the 4FSK modulation scheme and achieves the highest energy efficiency for reported TRX systems supporting 17 Gb/s or higher.

The rest of this article is organized as follows. Section II discusses the architectural considerations for designing a multi-Gb/s TRX. Section III details the TX design and implementation, and Section IV presents the RX design and implementation. Measurement results are also shown in Section V. Section VI concludes this article.

II. ARCHITECTURAL CONSIDERATIONS

A. Comparison of Digital Modulations

The required bandwidth for a PSK/QAM system is equal to the minimum Nyquist bandwidth. However, there is a more strict bandwidth requirement for the FSK systems than the Nyquist bandwidth. The required bandwidth in M-FSK modulation is called null-to-null bandwidth [45], [46]. Table I summarizes the bandwidth requirement and spectral efficiency of the digital modulation schemes. As the number of bits per symbol increases in PSK/QAM modulation schemes, the required bandwidth decreases. On the other hand, as the number of bits per symbol increases in an M-ary FSK modulation scheme, the required bandwidth becomes larger except for 4FSK. Therefore, PSK and QAM modulations are more spectrally efficient than FSK. However, the BER of the system increases in PSK and QAM as the M increases for the same signal-to-noise ratio (SNR), while the BER of the FSK decreases with an increasing M [42], [46]. The BER performance of different modulation schemes can be seen in Fig. 1. E_b/N_0 is defined as the ratio of energy per bit (E_b) divided by the spectral noise density (N_0). The SNR can be easily found from E_b/N_0 as

$$\text{SNR} = \frac{E_b}{N_0} \cdot \frac{f_b}{\text{BW}}. \tag{1}$$

It can be seen from Fig. 1 that as M increases, the FSK modulation requires less SNR at a fixed BER, while PSK/QAM modulations require more SNR at a fixed BER.

The other important factor in determining the optimum modulation choice in designing a multi-Gb/s TRX is the complexity of the system. M-PSK/QAM modulators and demodulators require coherent I/Q architectures that require data converters, I/Q mixers, and accurate low-noise synthesizers, as shown in Fig. 2(a). As a result, these systems are complex and power consuming to implement. Moreover, the power amplifier has to operate in a back-off region in QAM systems, significantly lowering its efficiency. On the other hand, OOK modulation can be achieved by a simple architecture as shown in Fig. 2(b) without separate modems and with a highly efficient power amplifier. Similarly, M-FSK modulation can be implemented non-coherently, does not require separate modems, and can utilize constant envelope highly efficient power amplifiers.

In this work, we have selected 4FSK modulation for designing a multi-Gb/s TRX. Compared to traditional OOK and BPSK, 4FSK includes 2 bits/symbol enabling higher data rate systems. 4FSK has better energy efficiency than M-PSK/QAM modulation schemes except for BPSK and QPSK. In addition, unlike M-PSK/QAM such as QPSK, the 4FSK modulation

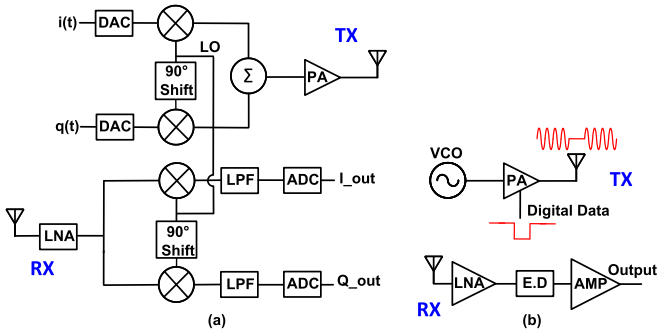


Fig. 2. Block diagram of (a) M-PSK/QAM and (b) OOK modem front ends.

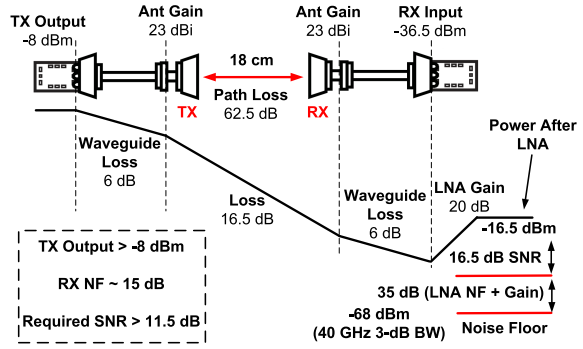


Fig. 3. Level diagram for an 18-cm wireless link between a pair of CMOS 4FSK TRX chips. Target specifications of the TRX are shown in the dotted rectangle.

scheme can be implemented non-coherently without the need for separate modems. 4FSK imposes less stringent requirement for power amplifiers and can potentially increase their efficiency. The 4FSK modulation is less bandwidth efficient than M-PSK/QAM. Nevertheless, large bandwidths are available at mm-wave frequencies, enabling a tradeoff between bandwidth and power efficiency.

B. Link Budget

In this work, for the non-coherent 20-Gb/s 4FSK system, a null-to-null bandwidth from 140 to 190 GHz is considered. This frequency range is selected to make sure that each symbol contains many periods of the carrier signal. If the operation frequency is beyond 200 GHz, designing LNAs and amplifiers will be challenging in the CMOS process. The required E_b/N_0 for BER of 10^{-12} in 4FSK modulation is 14.5 dB, and as a result, the required SNR at the RX's output for a 20-Gb/s data transmission is calculated from (1) to be 11.5 dB. Fig. 3 describes the link budget of the proposed TRX over a distance of 18 cm at a data rate of 20 Gb/s with 4FSK modulation. Here, the experiment is conducted using waveguide probes connected to two horn antennas. As shown in the dotted rectangle in Fig. 3, the minimum output power of the TX is -8 dBm, and the maximum noise figure (NF) of the RX is designed to be 15 dB. The gain of the RX is considered to be 20 dB. As a result, the SNR at the RX's output will be 16.5 dB. This will give us a 5-dB margin to deviate from the 18-cm distance or the specifications for different blocks.

C. Proposed 4FSK TRX

Fig. 4 presents the schematic of a conventional 4FSK TRX [47]. There are four voltage-controlled oscillators (VCOs) in the TX, which are tuned at four different frequencies ($f1$, $f2$, $f3$, and $f4$). The output of the TX is controlled by four switches, which can determine the frequency of the radiated signal. The input of the TX is a pair of parallel streams of binary data, which can be applied to a decoder to create the switch signals. Based on the input data, only one of the switches is ON and the rest are OFF at each moment. As a result, a 4FSK signal can be achieved. On the RX side, the signal is divided into four paths. The LNAs in different paths LNA_A, LNA_B, LNA_C, and LNA_D are tuned at $f1$, $f2$,

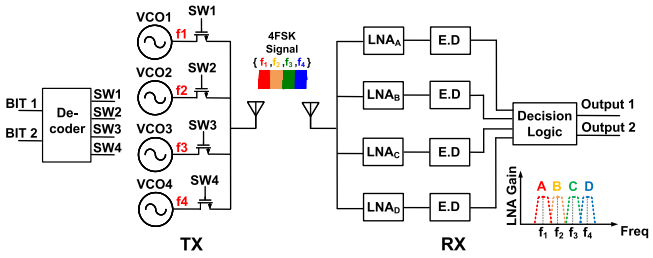
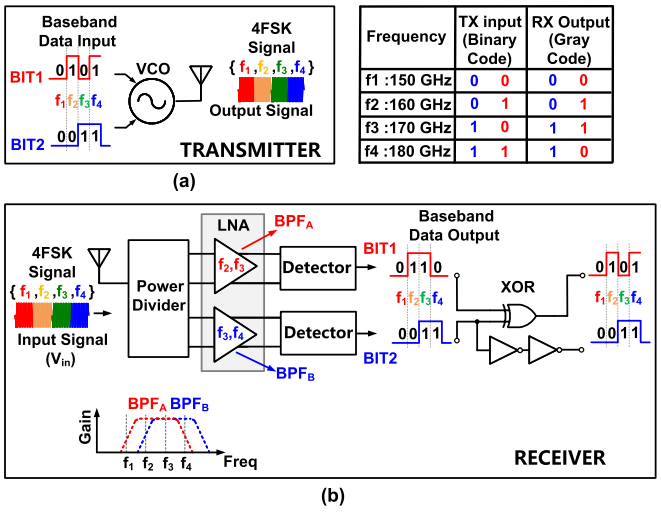


Fig. 4. Block diagram of a conventional non-coherent 4FSK TRX.

$f3$, and $f4$ frequencies, respectively. The following envelope detector can detect the power of the signal and generate data bits accordingly. The four generated data bits are then sent to the decision block to reconstruct the two parallel streams of binary data. The architecture in Fig. 4 has several drawbacks. The four VCOs in the TX increase the power consumption significantly. Moreover, the coupling between the VCOs could cause pulling and corrupt the modulated signal. The switches are lossy, especially at the mm-wave frequencies, and have significant parasitics, which can decrease the output power of the TX and limit the data rate. Switching VCOs create phase discontinuity and spreads the spectrum and increases the required bandwidth. In addition, the four paths in the RX side add to the power consumption and reduces the TRX efficiency significantly.

Here, we introduce a new architecture to implement a 4FSK TRX. Fig. 5 shows the conceptual 4FSK TRX architecture. The TX consists of only one VCO instead of four VCOs. Therefore, the power consumption of the TX is reduced remarkably. Two parallel streams of binary data are directly applied to the VCO varactors, which can change the frequency of the VCO. The VCO generates four distinct frequencies of $f1 = 150$ GHz, $f2 = 160$ GHz, $f3 = 170$ GHz, and $f4 = 180$ GHz for the input data pairs of (0, 0), (0, 1), (1, 0), and (1, 1), respectively, without the need for any switch. As was mentioned in Section II-B, the required null-to null bandwidth for the 20-Gb/s data rate is 50 GHz (140–190 GHz). Therefore, the frequencies of the 4FSK signal are selected as 150, 160, 170, and 180 GHz, which results in the 10-GHz frequency spacing. The TX modulates and upconverts the binary data at



Frequency	TX input (Binary Code)		RX Output (Gray Code)	
f1 :150 GHz	0	0	0	0
f2 :160 GHz	0	1	0	1
f3 :170 GHz	1	0	1	1
f4 :180 GHz	1	1	1	0

Fig. 5. Proposed 4FSK TRX architecture. (a) Transmitter. (b) Receiver.

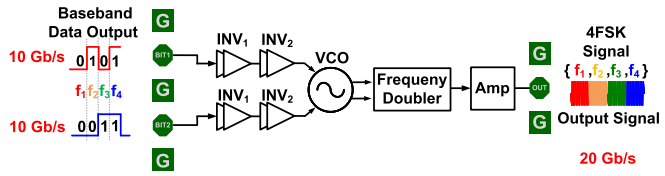


Fig. 6. Block diagram of the proposed 4FSK TX.

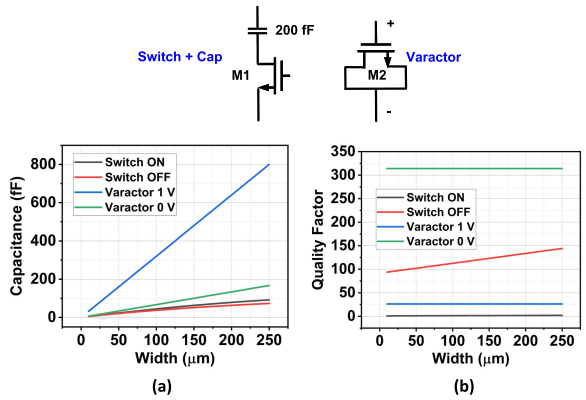


Fig. 7. (a) Simulated capacitance and (b) quality factor of an NMOS switch with $L = 60$ nm in series with an ideal 200-fF capacitor and an NMOS varactor with $L = 200$ nm at 80 GHz.

the same time removing the need for a separate modulator. Furthermore, the TX architecture is simpler to implement in comparison to PSK/QAM TXs.

The conceptual 4FSK RX architecture is shown in Fig. 5(b). The 4FSK signal is divided into two paths instead of four in this RX. Therefore, power consumption can be reduced remarkably. The LNA in the first path is tuned at $f2$ and $f3$ frequencies, while the LNA in the second path is tuned at $f3$ and $f4$ frequencies. Consequently, there is a frequency overlapping between the two paths. Designing such overlapping filters is doable at these frequencies due to the high enough frequency spacing of 10 GHz in the proposed system. The following detector senses the power of the signal at the output of the LNA and generates "1" or "0" bits based on the threshold of the detector, which can be adjusted to clearly distinguish the power of the signal. As a result, (0, 0), (1, 0), (1, 1), and (0, 1) will be generated at the output of the RX for $f1$, $f2$, $f3$, and $f4$ frequencies, respectively. While the data bits at the TX input are binary code, the data bits at the output of the RX are gray code and can be translated to the same binary code using a simple digital logic circuit. The proposed 4FSK RX can demodulate the 4FSK data with only two paths, which simplifies the architecture and reduces the power consumption in comparison to the conventional 4FSK RX. In addition, the proposed 4FSK RX demodulates the signal directly without the need for a separate demodulator or data converter.

The proposed architecture is also different than the traditional 4FSK TRXs in the sense that in this architecture, the RX filters the signal at $f1$ frequency. Thus, despite the fact that the modulator in this architecture generates the $f1$ frequency similar to conventional 4FSK modulators, the RX does not care about the power of the signal at the $f1$ frequency. As a result, the BER performance for the proposed architecture is better than the conventional 4FSK architecture. The reason is that since the RX does not care about the power of the signal at the $f1$ frequency, there is no SNR requirement for the RX to detect the $f1$ frequency as opposed to the conventional 4FSK.

III. Transmitter Design and Implementation

Fig. 6 shows the block diagram of the proposed 4FSK TX. Two parallel streams of binary data, each carrying 10 Gb/s, are applied to the four stages of inverters. The inverters with VDD of 1 V make sure that a near square-waved signal is received by the VCO. The varactors in the VCO are sized such that the VCO generates 75, 80, 85, and 90 GHz if the input data are (0, 0), (0, 1), (1, 0), and (1, 1), respectively. The frequency doubler is used to double the tuning range and the frequency spacing, thus reducing the complexity of the VCO design. The amplifier is also used to increase the output power and to equalize the power for the four output signals by careful matching network (MN) design.

A. Voltage-Controlled Oscillator

The VCO needs to generate 75-, 80-, 85-, and 90-GHz frequencies using the minimum possible dc power. The required tuning range of the VCO has to be around 18%, which is challenging to achieve. Furthermore, the layout of the VCO should be carefully designed such that it receives the parallel data bits from one side and generates the output signal to feed the frequency doubler from the other side. This is to reduce the coupling between the digital signals (data bit streams) and the analog signals (differential output of the VCO) and to make it easier to characterize the chip.

Active and passive mode switching has been used to increase the tuning range of the VCOs [48], [49], [50]. While mode switching can increase the tuning range of the VCO

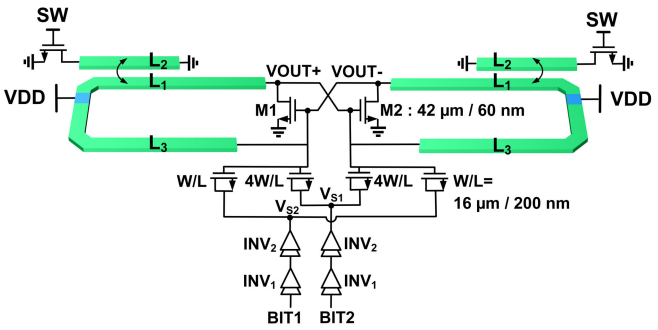


Fig. 8. Schematic of the proposed VCO.

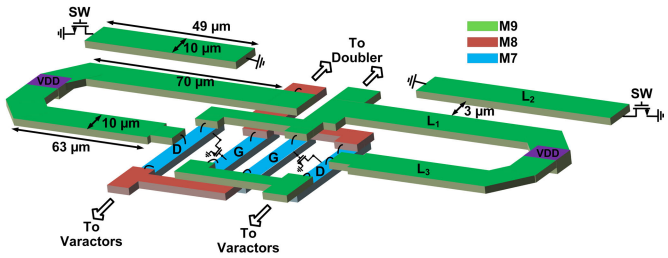


Fig. 9. 3-D view of the VCO.

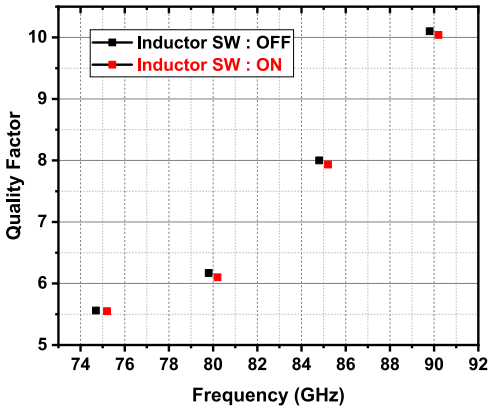


Fig. 10. Simulation result of the quality factor of the VCO's tank.

significantly, the switching speed is limited, making it impossible to use in high data rate applications. Another approach is inductor and capacitor switching, which has been utilized in many previous works [51], [52], [53], [54]. While inductor and capacitive switching is simple to design and straightforward in achieving the 4FSK modulation, it suffers from a tradeoff between the ON resistance of the MOS switches and its parasitic capacitance in the OFF state. This tradeoff becomes more significant at operation frequencies over 50 GHz.

In this design, we have utilized NMOS varactors for frequency tuning. The capacitance of the varactors can be controlled by their voltages, hence eliminating the need for MOS switches. Fig. 7 presents the comparison between an NMOS switch with $L = 60$ nm in series with an ideal 200-fF capacitor and an NMOS varactor with $L = 200$ nm at 80 GHz. In this simulation, the parasitic components of the transistors are not extracted and thus present a higher quality factor compared to real components. The relative performance between the two cases is nonetheless illuminating even with no transistor extraction. It can be seen that the capacitance presented to the VCO tank is small between the ON and OFF states of the switch, while the capacitance change is much bigger when the voltage across varactor changes from 0 to 1 V. Therefore, NMOS varactor provides much larger tuning range than the capacitor switching. The quality factor of the switch in series with the capacitor is much lower than the varactor when the switch is ON, as can be seen in Fig. 7(b). This degrades the performance of the VCO by limiting the tuning range and the VCO's output amplitude. Therefore, our simulations show that using the switching method fails to achieve the required tuning range or data rate.

The schematic of the proposed VCO is shown in Fig. 8. The VCO's core transistors are sized 42 μm/60 nm. Two sets of varactors are connected to the VCO's core to implement the 4FSK modulation. The inverters ensure that the voltage at V_{S1} and V_{S2} is either 0 or 1 V. The V_{S1} and V_{S2} nodes are virtual grounds, and therefore, the output impedance of the inverters is not seen by the VCO at the fundamental oscillation frequency. The size of the smaller varactor is 16 μm/200 nm and the size of the larger varactor is 64 μm/200 nm. The VCO tank includes L1 and L3 transmission lines (TLs) that are in parallel, so the length of L1 and L3 is relatively large for easier and more reliable implementation. The details of the TLs layout are shown in Fig. 9. L1 and L3 TLs are designed to be on the left side and right side of the VCO's core transistors to enable access to data bits and output of the VCO from the bottom and top sides, respectively. The impedance looking into L1 from the tank is a function of the impedance of L2 in series with the switch, SW. In this way, the switch can perform fine frequency tuning. This is especially helpful when the four frequencies are not exactly the required frequencies, due to the process variations. The VDD of the VCO is 1 V and is connected to the VDD plane for adequate ac coupling to ground. The VDD plane is implemented in M3 and M4 metal layers. The whole passive structure shown in Fig. 9 was simulated in HFSS to validate the performance of the VCO. Fig. 10 presents the quality factor of the VCO's tank. The quality factor of the tank is around 10 at 90 GHz and reduces to almost 5.5 at 75 GHz. The reason is that the varactors are more lossy when they provide more capacitance to the tank.

B. VCO Design Considerations

The proposed VCO has to satisfy two criteria. First, the VCO should achieve a fast frequency transition between the four frequencies to be able to support a 20-Gb/s data rate. Second, the VCO has to have enough tuning range to generate the four frequencies with the required spacing.

The transition speed between the frequencies in the proposed VCO depends on two parameters. First, the time it takes for varactors to change their capacitance when their voltage changes. Second, the time it takes for the cross-coupled VCO to adjust the frequency, reacting to the change in the varactor's capacitance. It can be shown that the transition speed, and ultimately the data rate, is mainly limited by the time it takes for the varactors to change their capacitance. In order to verify

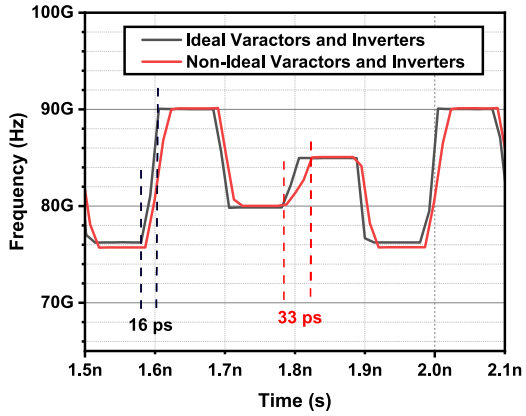


Fig. 11. Simulation result of the frequency transition speed of the VCO for ideal versus non-ideal varactors and inverters for 20-Gb/s data rate.

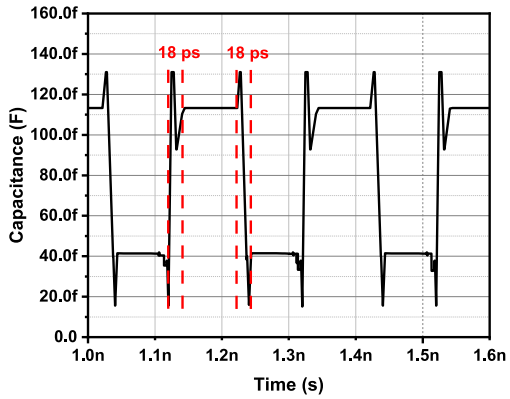


Fig. 12. Simulation result of the varactor's capacitance change versus time. The size of the varactor is 64 μm/200 nm.

that, two simulations are done using the circuit in Fig. 8. In the first simulation, ideal inverters and varactors are used to instantly change the tank capacitance of the VCO. In this simulation, the speed of the frequency transition is determined by the time it takes for the VCO to react to the capacitance changes. The simulation result with the data rate of 20 Gb/s (10 Gb/s for each varactor) is shown in Fig. 11. Here, the worst frequency transition time in the pattern is 16 ps, which is close to one period cycle of the lowest oscillation frequency of 75 GHz. This suggests that the VCO adjusts the frequency almost instantly and it takes one period cycle for the simulator to calculate the new frequency. In the second simulation, non-ideal varactors and inverters are used, and therefore, the speed of frequency transition is a function of the VCO's reaction time in addition to the time it takes for the varactors to change their capacitance values. As shown in Fig. 11, the worst frequency transition time, in this case, is 33 ps. This means that the maximum data rate is mainly limited by the time it takes for the varactors to change their capacitance. The analysis on transient response of a cross-coupled VCO is out of the scope of this work and can be found in [55], [56], [57], and [58].

Fig. 12 shows the simulation result showing the 64-μm/200-nm varactor's capacitance change versus time. In this simulation, the gate voltage of the varactor is kept at 1 V and the drain–source voltage is changed from 1 to 0 V

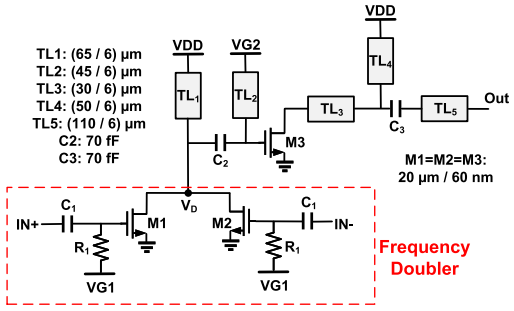


Fig. 13. Schematic of the frequency doubler and amplifier.

by the same inverters shown in Fig. 8 at 10 Gb/s. It can be seen that it takes 18 ps for the varactor to change its capacitance, matching the results in Fig. 11 and reiterating the fact that the maximum data rate is dominantly limited by the speed of the varactor's capacitance change.

The second requirement for the VCO is tuning range. Larger varactors provide more tuning range but limit the data rate because it takes a longer time to charge/discharge a larger varactor. Moreover, it introduces more parasitic capacitors and reduces the oscillation frequency. As a result, the varactors must be sized optimally to balance the tradeoff between the tuning range, the data rate, and the center frequency. This tradeoff can be further alleviated by carefully sizing the inverters to minimize the rise and fall time at V_{S1} and V_{S2}.

C. Frequency Doubler and Amplifier

The configuration of the doubler and amplifier is shown in Fig. 13. The push–push doubler consists of two common-source transistors in parallel. The dc gate voltage of the doubler transistors is set at 0.5 V by R_1 resistors. The simulation results show that higher dc bias for the doubler transistors increases the power consumption significantly but does not increase the gain of the frequency doubler much. TLs TL_1, TL_2, and C_2 form the inter-stage matching between the frequency doubler and the amplifier. The amplifier consists of one-stage common-source configuration with M3 transistor. The gate voltage of M3 is set at 0.8 V. The bias voltage is selected as 0.8 V as a tradeoff between the gain of the amplifier and its power consumption. The output MN includes TL_3, TL_4, TL_5, and C_3. The output MN is designed carefully so that the power of the signals at 160, 170, and 180 GHz is close to each other. It is worth mentioning that the 150-GHz signal is blocked by both paths of the RX. However, generating 150 GHz in the TX is necessary since it makes the frequency transition in the VCO much faster. Because of this, there is little consideration on the power of the 150-GHz signal. The reason that the RX is designed to block 150 GHz and not 180 GHz is that the varactors have higher loss when tuning to 150 GHz. Fig. 14(a) presents the simulated output power of the amplifier when the input power of the frequency doubler is -5 dBm. The frequency doubler and the amplifier provide the maximum gain at around 165 GHz. However, when integrated with the VCO, the doubler and the amplifier have a more equalized output power at the three interested

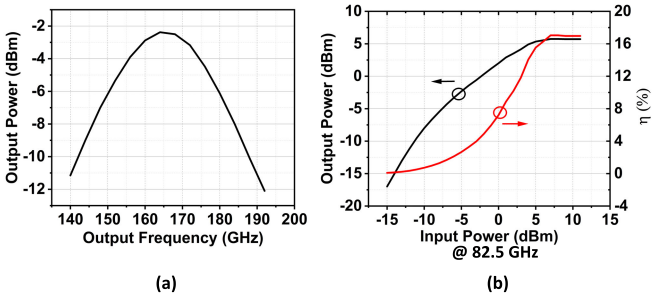


Fig. 14. (a) Simulated output power of the amplifier versus frequency. Frequency doubler's input power is kept at −5 dBm. (b) Simulated output power of the amplifier and drain efficiency of the doubler–amplifier chain at 165 GHz versus the input power of the frequency doubler.

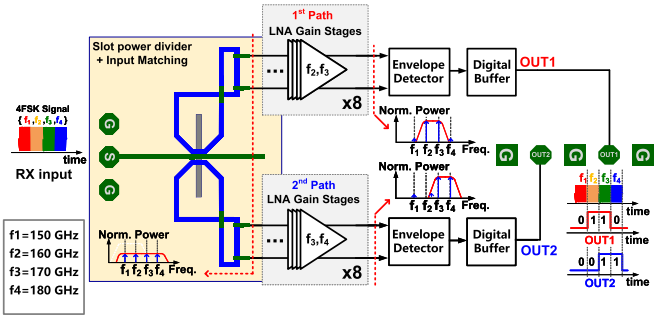


Fig. 15. Block diagram of the proposed 4FSK RX.

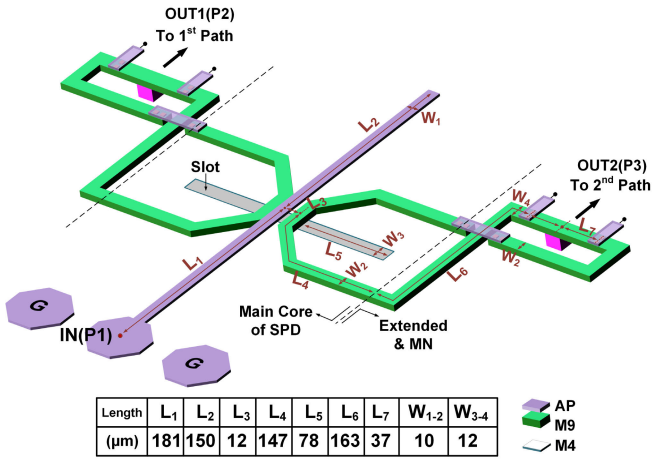
frequencies. This is mostly because the VCO's signal swing is larger at higher frequencies due to lower varactor losses. The typical output power of the TX is around −4 dBm. Fig. 14(b) shows the simulated output power of the amplifier and drain efficiency of the doubler–amplifier chain at 165 GHz versus the input power of the frequency doubler. The output power saturates at around 5.7 dBm. The maximum power-added efficiency (PAE) of the doubler–amplifier chain at 165 GHz is 8%.

IV. Receiver Design and Implementation

Fig. 15 shows the block diagram of the proposed 4FSK RX. A slot power divider (SPD) is used to split the 4FSK signals equally into two different paths. Each path is comprised of an LNA, an envelope detector, a baseband amplifier, and output buffers.

A. Wideband SPD

Previous works have demonstrated that the slot-line-based power divider/combiner can achieve low-loss, wideband, and balanced performance at frequencies over 120 GHz [59], [60]. Given the wideband requirements for this system, an SPD similar to [59] is used at the RX. Fig. 16 shows the proposed SPD. In the main core of the SPD, the input signal is applied to the TL in the AP layer, creating a current in the TL. This current is coupled to the slot in the ground plane (M4 layer) as it travels over the slotline perpendicularly. Conversely, the field generated in the slot is coupled to the green TLs (M9 layer). In this case, the transition is excited by only the odd-mode



Length	L_1	L_2	L_3	L_4	L_5	L_6	L_7	W_{1-2}	W_{3-4}
(μm)	181	150	12	147	78	163	37	10	12

Fig. 16. Proposed SPD with the MN.

TE wave propagating through the slot [60]. The microstrip-to-slotline and slotline-to-microstrip structures can be modeled as two transformers equivalent to simple *LC* tanks [59]. This helps the SPD to achieve a wideband performance by carefully managing the two resonant frequencies of the microstrip-to-slotline structure. The extended lines (L6 and L7) connected to the SPD construct the MN and change the direction of the two outputs of the power divider to be in the same direction. This helps with connecting the following LNA stages to the SPD and making sure that the two output bit streams can be collected from one side of the chip. Fig. 17 shows the simulated and measured performance of the SPD. The insertion loss of the power divider is 1.8 dB at 165 GHz, with a maximum variation of 0.4 dB at the frequency band of interest (150–180 GHz). The simulated $S12$ between the input and output port of the SPD, including the extended lines and MN, is −6.5 dB at 165 GHz. The loss from the extended lines and MN is less than 2 dB. The simulated $S11$ of the SPD is lower than −10 dB from 135 to 190 GHz, which results in 33% fractional bandwidth. The measured $S11$ is also shown in Fig. 17, which is less than −10 dB for the required bandwidth. An N5247A PNA-X network analyzer with a WR-05.1 virginia diodes Inc. (VDI) frequency extender module was used to perform this measurement.

The bandwidth of the SPD covers all the four carrier frequencies, while the bandwidth of the LNA at each path covers only two overlapping frequency ranges. Due to the low port-to-port isolation of the SPD, the bandwidth of the SPD would be limited by the narrowband MNs within the LNA stages at each path. To address this issue, the first LNA stages need to utilize wideband input MN and neutralization technique to provide isolation between the LNA stages and the SPD. Fig. 17 shows that such wideband matching is achieved.

B. LNA

To explore the speed limit of the proposed RX, we consider the worst case, which is the switching between two frequencies pattern. In this case, two sideband signals with frequency spacing of fm from the designated FSK carrier frequency

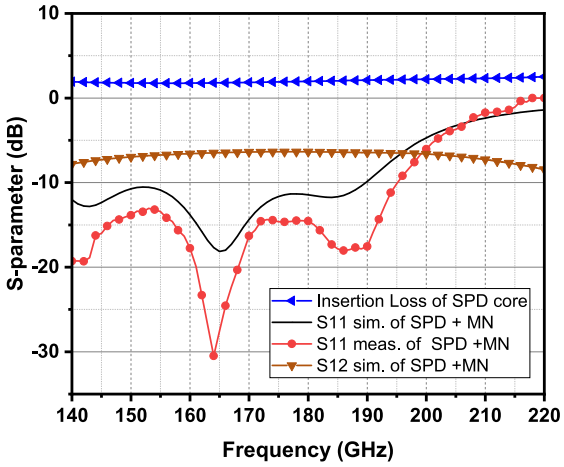


Fig. 17. Measured and simulated performance of the SPD.

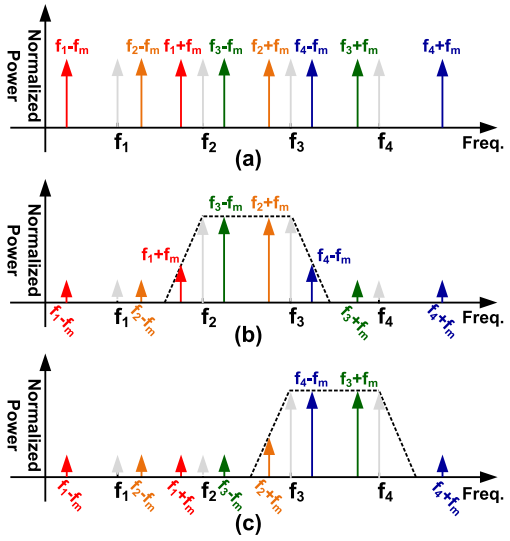
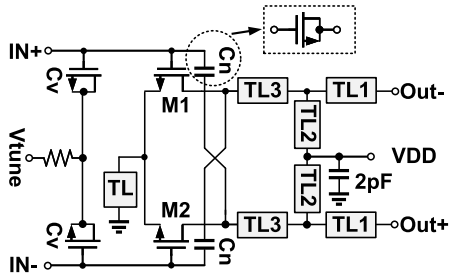


Fig. 18. Bit-switching spectrum analysis of the 4FSK signal at (a) RX input, (b) output of LNA in the 1st path, and (c) output of LNA in the 2nd path.



		Length , Width (μm)	
		@ 1st Path	@ 2nd Path
TL1	AP	87, 8	81, 8
TL2	M9	25, 10	25, 12
TL3	AP	72, 8	69, 8
TL	M9	25, 2	

M1,M2: 10μm/60nm
Cn: 4.3μm/60nm
Cv: 2μm/200nm

Fig. 19. Schematic of the unit cell for LNA stage.

are generated when the data rate is 2fm at each channel. For example, if the bits (0, 0) are changed to bits (0, 1) at the TX, the frequency tones of $f1 \pm$ fm and $f2 \pm$ fm are generated in the 4FSK radiated signal. The RX can extract the data bit information by detecting the corresponding frequency tones and their sidebands. Fig. 18(a) shows all the possible first-harmonic frequency tones at the RX input when the 4FSK frequency spacing is a little more than fm. Since the detected signal depends on the power level of the frequency tones, the power of the sideband frequencies of interest should be significantly larger than other tones within the Rx band. In the 1st path that detects any frequency tones between $f2$ and $f3$, only the sideband frequencies of $f2 +$ fm and $f3 -$ fm should be amplified, while other signals, mainly $f1 +$ fm and $f4 -$ fm, should be suppressed. Similarly, only the sideband frequencies of $f3 +$ fm and $f4 -$ fm should be amplified in the 2nd path. Fig. 18(b) and (c) shows all the possible first-harmonic frequency tones of the 4FSK signal presented at the output of the LNA in the 1st and 2nd paths, respectively. As the fm increases, sideband frequencies get closer to each other, leading to bit errors. For instance, the frequency tones of $f1 +$ fm and $f4 -$ fm will approach the frequency tones of $f3 -$ fm and $f2 +$ fm, respectively. This causes interference in the 1st path of the RX, increasing the BER. This consideration dictates the RX requirements such as bandwidth and roll-off with respect to 4FSK frequency spacing and data rate.

In this work, the 4FSK frequency spacing is 10 GHz, and the data rate is 20 Gb/s resulting in the maximum fm of 5 GHz for each path. For a second-order MN (e.g., "T" MN) used in the RX, the roll-off is 4 dB/GHz (40 dB/decade). To have more than 10-dB gain suppression of the unwanted sidebands, the bandwidth of the LNA should be less than 15 GHz. While lower bandwidth for each path can provide better suppression for the undesired signals and can reduce the integrated noise, it also reduces the data rate by suppressing the desired higher order sidebands. Therefore, the optimum bandwidth of the LNA is designed to be around 15 GHz.

Fig. 19 shows the schematic of the unit cell for the LNA stage. The width and length ratio of the transistor (M1 and M2) is 10 μm/60 nm. While using smaller transistors for the LNA stage can reduce the power consumption of the amplifier, it also requires smaller neutralization capacitors that could be hard to implement. In this case, the capacitor Cn for neutralization is around 4 fF. The current density of the M1 and M2 transistors is 0.5 mA/1 μm as a compromise between the minimum NF and the maximum available gain. A TL (20 μm) is added to the source of the transistors to avoid common mode oscillation. Fig. 20 shows the simulated gain of eight cascade stages of the LNAs. The power supply voltage of the LNA stages is 0.75 V. The simulated maximum gain of the LNA in the 1st path is 35 dB and its 3-dB bandwidth is close to 15 GHz, while the other path has a gain of 27 dB and a bandwidth of 15 GHz. Since the RX demodulation depends on the relative gain of the LNA at different frequencies, the maximum gain for the paths can be different, as long as each path can provide enough amplification for the signal to be detected. The simulated NF of the LNA stages, including SPD in the two RX paths, is also shown in Fig. 20. The simulated

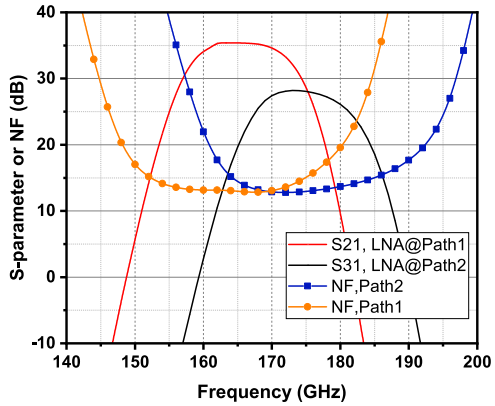


Fig. 20. Simulated gain of eight cascade stages of the LNA including SPD.

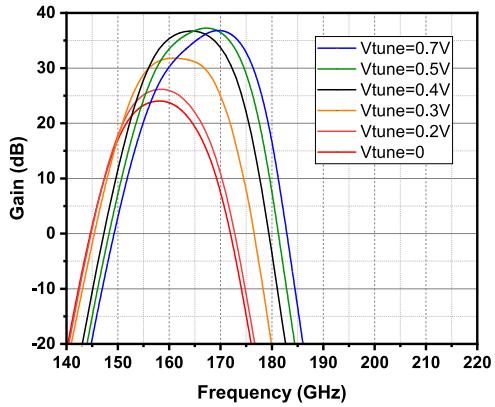


Fig. 21. Simulated gain of the LNA in the 1st path with different tuning voltages.

maximum NF across the frequency bands of interest for both RX paths is less than 15 dB.

The frequency bands of the LNA stage mainly depend on the two resonant tanks created by the "T" MN. Frequency tuning can be achieved by changing the input impedance of the transistors, thus modifying one of the resonance frequencies for the MN. In this design, to compensate for the frequency shifts due to the process variation, NMOS varactors (Cv) are used in the input of the M1 and M2. Fig. 21 shows the simulated gain of the LNA in the 1st path with different tuning voltages. The center frequency can be shifted from 159 to 170 GHz. As the tuning voltage decreases, the input capacitance of the LNA increases, and hence, the frequency band is shifted to lower frequencies. However, increasing the capacitance of the varactors also adds extra loss leading to the gain reduction. The reason is that the varactors are more lossy when they provide more capacitance.

C. Enveloped Detector and Baseband Circuit Design

Fig. 22 shows the schematic of the envelope detector and baseband circuit. The NMOS transistors in the differential envelope detector are class AB biased for better sensitivity [61]. The bandwidth of the R1-CF lowpass network at the output of the detector is designed to be around 25 GHz to allow the recovered data to pass through with minimum ripples. Higher bandwidth helps with the data recovery but at

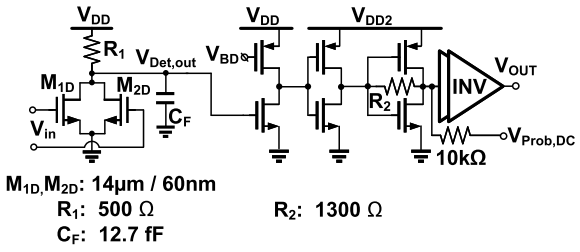


Fig. 22. Schematic of envelope detector and baseband circuit.

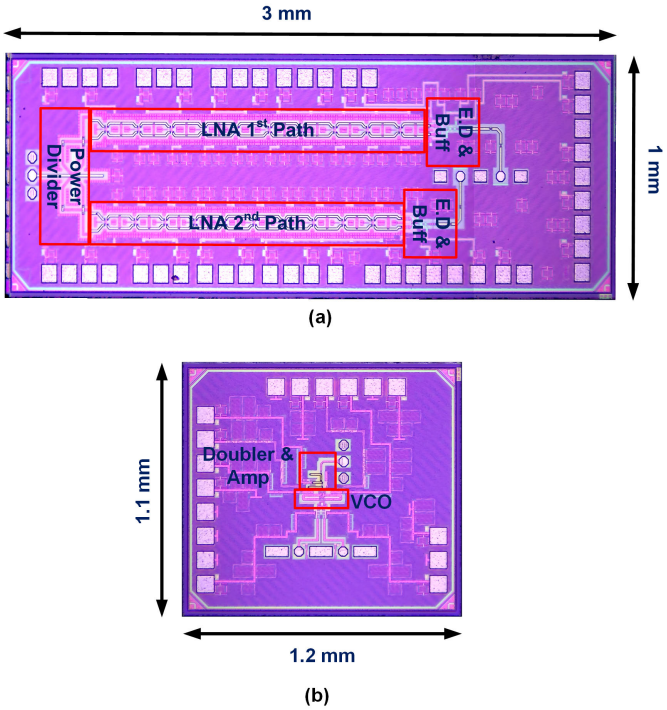


Fig. 23. Chip micrograph of (a) receiver and (b) transmitter.

the same time increases the integrated noise, thus decreasing the SNR.

The following circuit is used to amplify the demodulated signal and convert it into digital signals. The first stage of the buffer is used as a voltage level shifter to tune the threshold of the inverter, calibrating the RX for different input power levels. In order to make the RX dynamically adaptive for different link distances, the LNAs can be designed to have automatic gain control as a function of signal power and hence eliminate the manual threshold tuning of the inverter. The last inverter stage is implemented to drive the 50-Ω loading. Additional dc pads with a large resistor are added to the output of the inverter-based amplifiers for characterizing the frequency response of the RX.

The simulated integrated output noise voltage of the detector over 25 GHz is 0.44 mV. The sensitivity calculation is similar to [62] with assumption of noiseless baseband circuit. Including the conversion gain and NF of the LNA, the sensitivity of the RX for 160, 170, and 180 GHz can be calculated to be −44, −44, and −44.9 dBm, respectively. Due to the limited gain of the baseband and inverter buffers, it is required for

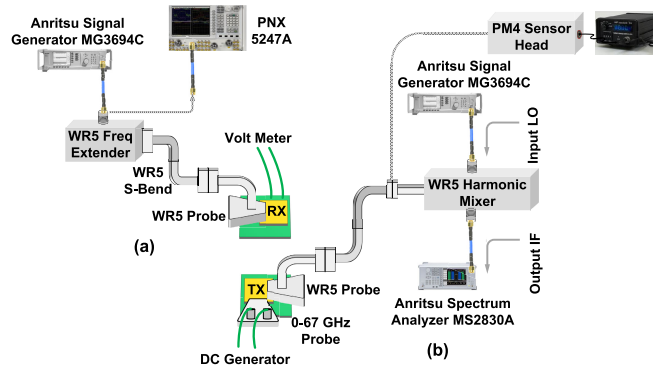


Fig. 24. Measurement setup for characterizing (a) receiver and (b) transmitter.

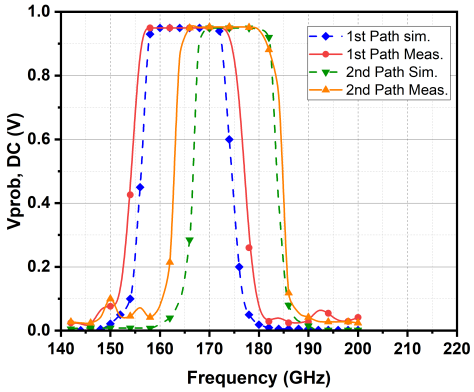


Fig. 25. Simulated and measured normalized gain of the RX.

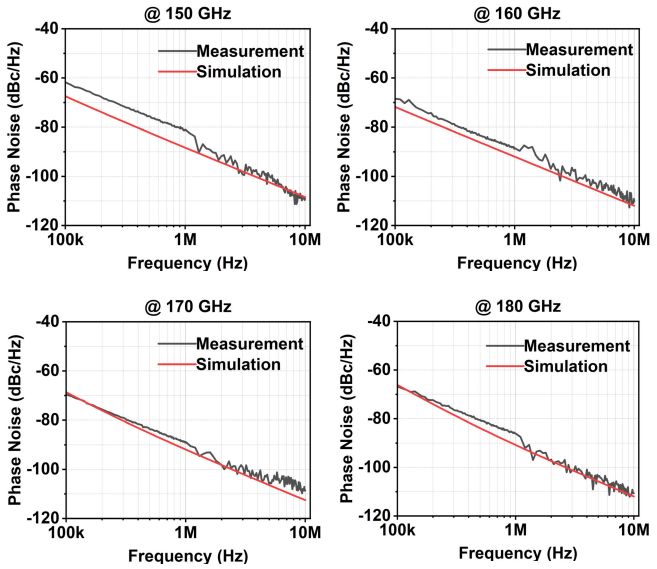


Fig. 26. Measured phase noise of the output of the TX at different frequencies.

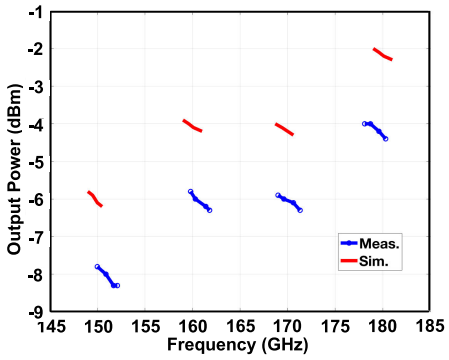


Fig. 27. Measured output power of the TX at distinct frequencies.

the detector output to have an amplitude of more than 50 mV to make sure that the inverters are sufficiently triggered and the data are accurately recovered. This demands higher input power for the RX of −40 dBm compared to the sensitivity of the RX. In other words, the input power of −40 dBm is required to create 50-mV amplitude at the inverters when the data rate is very low. As the data rate increases, we need more than −40-dBm input power to maintain 50-mV amplitude at the inverters. In order to improve the data rate and energy efficiency of the 4FSK TRX, more baseband gain stages could be easily added to the RX architecture in future designs.

V. Measurement Results

The TX and RX circuits are fabricated in a 65-nm CMOS process. Fig. 23 shows the die micrographs. Various measurement setups are used to characterize the performance of the TX, RX, and TRX systems. The chips are wire-bonded to separate printed circuit boards (PCBs) to easily adjust the distance between the TX and RX antennas. Fig. 24 shows the measurement setups for testing the RX and TX chips. An Anritsu MG3694C signal generator, a VDI WR5 frequency extender, and WR5 probe and waveguides are used to provide the RX with 150-, 160-, 170-, and 180-GHz signals. The power of the signal for all the frequencies is kept at −17 dBm, and the dc voltage at the output of the inverter-based amplifiers ($V_{\text{probe,dc}}$) was measured as a function of frequency. Fig. 25 presents the normalized gain of the two paths of the RX. The simulated 3-dB bandwidth of both paths is around 16 GHz, while the measured bandwidth is around 20 GHz with the same biasing conditions. Due to the passive EM modeling errors, the loss of the MNs is underestimated in simulation, increasing the bandwidth in measurement.

Two dc signals are used to change the frequency of the TX, as shown in Fig. 24. The output signal of the TX was down-converted using an oleson microwave labs Inc. (OML) even-harmonic WR5 mixer. An Anritsu MG3694C signal generator was used to generate the local oscillator (LO) signal for the mixer. The down-converted signal was fed to an Anritsu MS2830A spectrum analyzer in order to measure the phase noise and frequency of the signal. The output power of the TX was directly measured using a VDI Erickson PM4 power meter. The phase noise of the TX at the frequencies of interest is shown in Fig. 26. The phase noise at 1-MHz frequency offset is −81, −88, −89, and −86 dBc/Hz at 150, 160, 170, and 180 GHz, respectively. As shown in Fig. 27, the output power of the TX is −6, −4, −4, and −2 dBm at 150, 160, 170, and 180 GHz, respectively. Based on the discussion in Section III, the power of the 150-GHz signal is of little interest. The other three frequencies show similar output power, which helps with the accurate operation of the RX. There is a small

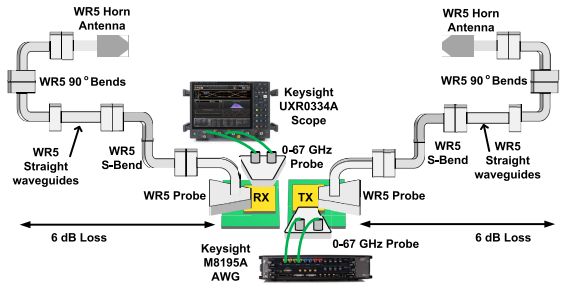


Fig. 28. Measurement setup for characterizing the TRX.

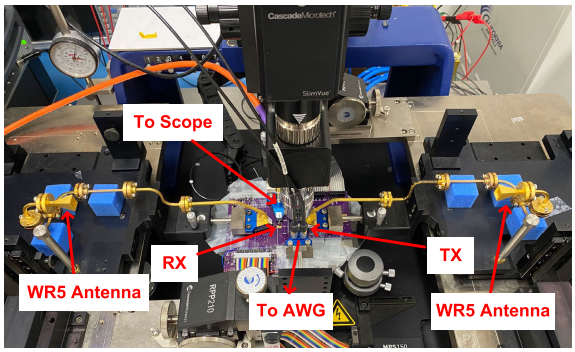


Fig. 29. TRX test setup photograph.

TABLE II
POWER CONSUMPTION OF BLOCKS

Component	Power Consumption (mW)
VCO	40
Freq Doubler	7
Amplifier	15
LNA stages	94
ED & Baseband	26

tuning range at each center frequency, which is achieved by the coupled TLs with switches in the VCO architecture as discussed before.

A Keysight M8195A arbitrary waveform generator (AWG), a Keysight UXR0334A oscilloscope, and WR5 waveguides and horn antennas were employed to perform the eye diagram measurement, as shown in Fig. 28. The photograph of the TRX measurement setup is also shown in Fig. 29. The AWG generates two parallel streams of data bits that are fed to the input of the TX by a dual 67-GHz probe. The output signal of the TX is probed and connected to a WR5 horn antenna with a 23-dBi gain by WR5 waveguides, as shown in Fig. 28. Another horn antenna receives the signal and leads it to the RX's input by WR5 waveguides and probe. The link distance between the two horn antennas can be controlled by adding/removing straight waveguides. The total loss of the WR5 waveguides and probe is around 6 dB for an 18-cm distance. Finally, the two outputs of the RX are sent to the Keysight scope for eye diagram and BER measurement. Time-domain eye diagrams for 18-, 28-, and 40-cm link distances are shown in Figs. 30–32, respectively. The BER was calculated based on the eye diagram measurement results. The maximum realized data rate is 17 Gb/s for an 18-cm distance with a

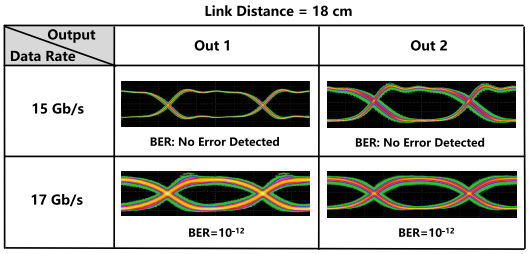


Fig. 30. Measured performance of the 4FSK TRX for 18-cm link distance.

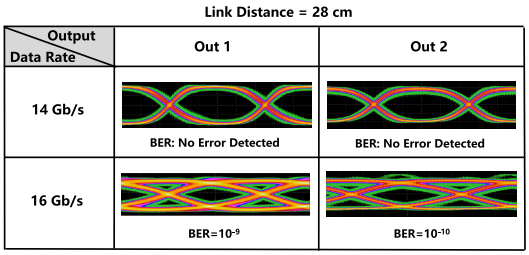


Fig. 31. Measured performance of the 4FSK TRX for 28-cm link distance.

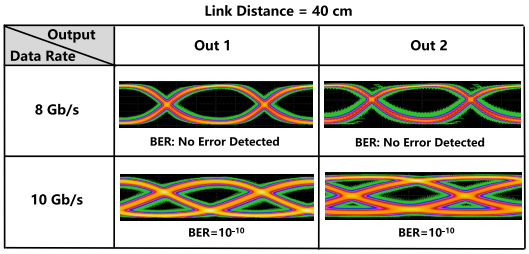


Fig. 32. Measured performance of the 4FSK TRX for 40-cm link distance.

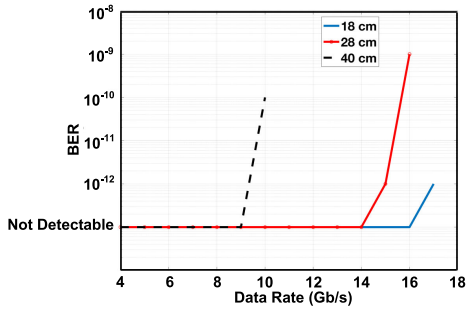


Fig. 33. Measured BER performance versus the data rate.

BER of 10^{-12}. The maximum measured distance is 40 cm with a 10-Gb/s data rate and a BER of 10^{-10}. In addition, the system supports a 16-Gb/s data rate at 28 cm with a BER of 10^{-9}. Fig. 33 summarizes the BER performance of the 4FSK TRX versus data rate. Table II shows the power consumption breakdown of the TRX. The proposed bit-in–bit-out TRX consumes 182 mW without the need for separate modems.

The summary and comparison of the proposed TRX with the state-of-the-art TRXs are presented in Table III. This article presents the first multi-Gb/s wireless TRX system with M-FSK modulation, to the best of our knowledge; Van Thienen et al. [44] presented a 2FSK system with 17.7-Gb/s data rate, and however, the TRX in this reference is not a

TABLE III
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART TRXS

Reference	Frequency [GHz]	Modulation	Integration	Total Antenna Gain [4]	Power Consumption [mW]	Data Rate [Gb/s]	Distance [cm]	BER	Energy Efficiency (TRX) [pJ/Bit]	Core Area [mm^2]	Technology
[23]	135	OOK	TX, RX, LO	Horn [2]	TX: 18 RX: 80	10	10	1E-11	9.8	2	40 nm CMOS
[35]	265	16 QAM	TX, RX, LO, w/o PLL [1]	Horn 18 dBi	TX: 890 RX: 897	80	3	1E-3	22.4	NA	40 nm CMOS
[31]	155	QPSK	TX, RX, LO	Waveguide Probe	TRX:345	20	NA	1E-6	17.25	3.9	45 nm SOI CMOS
[39]	210	OOK	TX, RX, LO	On-Chip 4.5 dBi	TX: 240 RX: 68	10 *	3.5	1E-5	30.8	4.62	32 nm SOI CMOS
[19]	140	16 QAM	TX, LO, Digital BB, Mod	Waveguide Probe	TX:173	160	NA	NA	1.1 (Only TX)	0.75	22 nm FinFET
[26]	140	QPSK	TX, RX, w/o LO [1]	WR06 40 dBi	TX: 165 RX: 192	48	180	2.3E-3	7.43	NA	250 nm InP
[44]	120	2FSK	TX, RX, Mod, Demod	Waveguide Probe	TX: 11 RX: 59	17.7	NA	1E-12	3.95	0.455	40 nm CMOS
[40]	130	OOK	TX, RX, LO, Lens	Package 26 dBi [3]	TX: 59 RX: 38	12.5	500	1E-6	7.76	0.4	55 nm BiCMOS
[4]	240	BPSK	TX, RX, LO, Lens [1]	On-Chip 14 dBi	TX: 375 RX: 575	20	15	6.3E-6	47.5	NA	130 nm SiGe
[32]	190	BPSK	TX, RX w/o LO [1]	On-Chip 5 dBi	TX: 32 RX: 122	50	0.6	3E-4	3.1	1.9	130 nm SiGe
This Work	**165**	**4FSK**	**TX, RX, Digital IO, Mod, Demod**	**Horn 17 dBi**	**TX: 62 RX: 120**	**10**	**40**	**1E-10**	**18.2**	**0.6**	**65 nm CMOS**
						16	**28**	**1E-9**	**11.37**		
						17	**18**	**1E-12**	**10.7**		

[1] Modulator and Demodulator are not integrated
[2] No antenna gain available
[3] Antenna in-package with lens
[4] Gain of the antenna minus measurement setup loss
* Estimated

wireless system. The power consumption and energy efficiency of many of the works reported in Table III do not include the power from the modem, which can be significant at a high data rate. The proposed TRX has one of the best energy efficiencies compared to state-of-the-art TRXs with a data rate of 17 Gb/s or higher and without the need for additional blocks before it can be connected to the digital signal processor on the TX or RX side. The proposed TRX has also achieved a higher data rate than reported OOK systems.

VI. CONCLUSION

A novel low-power and high data rate fully integrated bit-in–bit-out 4FSK TRX has been fabricated and demonstrated. Implemented in a standard 65-nm CMOS, the TRX achieves a 17-Gb/s data rate over a distance of 18 cm consuming only 182 mW. The non-coherent TRX does not need separate modems, therefore reducing the power consumption significantly. The TX core only includes one VCO to generate the 4FSK signal. In addition, a new frequency overlapping RX architecture is introduced for demodulating the 4FSK signal. The TRX is considered the first multi-Gb/s wireless TRX system with M-FSK modulation.

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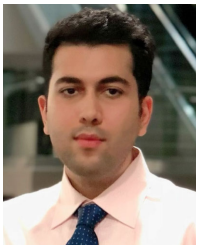

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