Design and Analysis of an On-chip Current-driven CMOS Parametric Frequency Divider

Mengting Yan, *Student Member, IEEE,* Hussein M. E. Hussein, *Student Member, IEEE,* Cristian Cassella, *Member, IEEE,* Matteo Rinaldi, *Senior Member, IEEE,* and Marvin Onabajo, *Senior Member, IEEE.*

***Abstract*—This paper introduces an on-chip current-driven CMOS parametric frequency divider (PFD) that provides 2:1 frequency division with an output frequency of 2.4 GHz. A custom input driver stage with a buffer enables to generate the input current of the PFD core from a digital clock signal or sinusoidal source, and a band-pass filter (BPF) stage suppresses undesirable harmonics at the output. Analyses and discussions of design considerations provide insights into the PFD's input driving conditions, filtering characteristics of the output driver, as well as the effects of the limited quality (Q) factor of passive components and layout parasitics. A prototype chip was fabricated in standard 65-nm CMOS technology and tested. The minimum required supply voltage for the PFD driver is 1.4 V with an input frequency of 4.8 GHz, whereas the PFD has an operating frequency range from 4.5 GHz to 5.1 GHz with a supply voltage of 1.5 V. To the best of the authors' knowledge, the proposed PFD is the first on-chip implementation of a current-driven parametric frequency divider in a standard CMOS process with sub-6 GHz operation, which demonstrates the feasibility of on-chip integration into RF systems.**

***Index Terms*—Parametric circuits, current-mode input, RF frequency divider, on-chip signal generation, parametric filtering.**

I. Introduction

THE growing demand for enhanced performance of devices in the Internet of Things (IoT) has led to explorations of parametric systems to reduce noise levels in narrowband applications. Based on the phenomena of parametric resonance and excitation [1], circuits such as parametric amplifiers [2]–[4] and frequency selective limiters (FSLs) [5], [6] were first investigated to achieve low-noise amplification and frequency-selective limiting. In the past decade, applications of parametric systems in quadrature-phase signal generation [7] and tunable parametric harmonic generation [8] were reported, where exceptional noise performance and controllable phase and/or harmonic frequency tuning were achieved. Applications in frequency conversions of continuous signals have also caught the attention of researchers [9]–[12], which have proven to consume less power compared to transistor-based mixers due to the extensive utilization of passive devices. Furthermore, a new technique aiming to reduce phase noise by utilizing a parametric filter (PFIL) has been reported in [13]–[15], where the phase noise of a noisy oscillator output is greatly suppressed by operating the closed-loop system at special operating points that are close to the Hopf bifurcation region [14]–[16].

Based on a previously reported PFIL for phase noise reduction as demonstrated by the measurements with discrete components in [15], an envisioned on-chip PFIL system utilizing

This work has been funded by the National Science Foundation (NSF) under award #1854573.

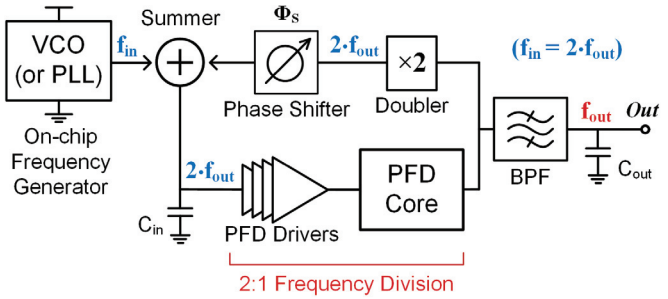

Fig. 1. Envisioned on-chip parametric filter (PFIL) system based on [15], containing a parametric frequency divider (PFD) to reduce the phase noise of oscillators or phase-locked loops (PLLs).

2:1 parametric frequency division is displayed in Fig. 1, which is under development to be integrated into RF CMOS Systems-on-a-Chip (SoCs) such as [17]–[21]. The envisioned system consists of five major building blocks: a summer (power combiner), a parametric frequency divider (PFD) core with drivers, a band-pass filter (BPF) stage, a frequency doubler and a phase shifter. The input signal of the closed-loop PFIL system is internally generated at twice the output frequency ($f_{in} = 2 \cdot f_{out}$) through a voltage-controlled oscillator (VCO) or phase-locked-loop (PLL), which is combined with the $2 \cdot f_{out}$ signal in the feedback loop. The PFD core with driver stages provides a 2:1 frequency division and generates an RF output at $f_{out} = f_{in}/2$, where the multi-stage drivers are implemented to ensure high-efficiency driving while maintaining low load capacitance (C_{in}) at the summer output. The output signal of the PFD core is filtered by a passive BPF centered at f_{out} and becomes the PFIL output, while the frequency doubler and phase shifter in the feedback loop process the PFD output to reconstruct the $2 \cdot f_{out}$ signal that is synchronized with the output of the VCO/PLL (i.e., f_{in}). As one of the most critical building blocks in a PFIL, several implementations of PFDs have been reported; however, most of the existing works are realized with off-chip solutions [22]–[27]. The first on-chip CMOS PFD was reported in [28] with operation at 20 GHz. However, when targeting sub-6 GHz operation, the layout area overhead due to on-chip transmission lines would further increase the chip area due to longer wavelengths at lower operating frequencies. Hence, for the system in Fig. 1, it is desirable to design an on-chip PFD with low input capacitance (C_{in}), avoidance of transmission lines, and the ability to drive the PFD utilizing on-chip digital or sinusoidal signals.

In this work, the first current-driven PFD design is presented for the sub-6 GHz frequency range, which does not utilize on-chip transmission lines or matching networks. A current-mode PFD driver with a clock (CLK) buffer stage was designed, where the input capacitance of the CLK buffer is minimized

such that it can be driven by a common digital signal or an on-chip VCO/PLL with sinusoidal-like output signal. A class-B band-pass filtering (BPF) output stage was implemented to extract the divided signal directly from the resonator core, providing the capability to drive subsequent on-chip blocks while circumventing the load on the PFD core. New PFD design insights are given through the analyses and discussions of the current-mode operation, the suppression of the signal at $2 \cdot \mathrm{f_{out}}$ in the class-B BPF output stage, as well as the impact of the degraded quality factors of the passive devices on the 2:1 frequency division. The experimental results reported in this paper indicate the feasibility of the proposed PFD to provide a 2:1 parametric frequency division at 4.8 GHz, and to be integrated into RF SoCs such as an on-chip closed-loop PFIL for phase-noise reduction envisioned in Fig. 1.

The remainder of this paper is organized as follows: Section II provides a general background on the fundamental concepts of parametric amplification and frequency division. Section III describes the design considerations and theoretical analyses of key building blocks of the CMOS PFD with a current-mode input. Section IV describes the topology of the PFD with further implementation-related design considerations. Measurement results of the fabricated PFD are presented and discussed in Section V. Section VI draws the conclusions.

II. Background

A. Fundamentals of Parametric Amplification

Parametric amplifiers are used for low-noise amplification that relies exclusively on reactive components such as capacitors and inductors, leading to a significant improvement of the noise figure due to the absence of thermal noise from transistors and resistors. Parametric amplification can be triggered by mixing an RF large-signal (pump) with an RF small-signal (input) using a nonlinear reactance. Consequently, part of the pump signal's power is transferred to the input signal through the mixing products, generating a gain at the output. In the simplified embodiment of a parametric amplifier shown in Fig. 2, the varactor serves as nonlinear reactance and is modulated by the pump signal. Here, the small input signal and the pump signal are injected through band-pass filter (BPF) sections, and the amplified output signal is received through a BPF that is tuned to the frequency of the desired mixing product. The BPF sections can be implemented with lumped components, transmission lines or other devices capable of resonance. For the case of an up-converter amplifier, the output BPF is extracting the $\mathrm{f_{LO}} + \mathrm{f_{sig}}$ component, where $\mathrm{f_{LO}}$ is the pump frequency and $\mathrm{f_{sig}}$ is the input signal frequency. In this case, the maximum achievable parametric gain can be estimated as follows [29]:

$$Gain = 1 + \frac{f_{LO}}{f_{sig}} \tag{1}$$

B. Parametric Frequency Division Concepts

A parametric frequency divider (PFD) is a circuit that leverages the nonlinear dynamics of modulated reactances to passively generate a frequency division. A simplified schematic

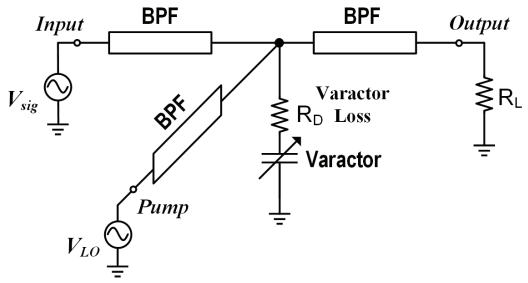

Fig. 2. Generalized representation of a parametric amplification circuit.

of a PFD is displayed in Fig. 3, which consists of input and output BPF sections connected at a common node with a branch that includes a series combination of an impedance and a modulated reactance (i.e., the diode's capacitance in this case). The input BPF is designed such that it allows the pump power to be delivered to the diode's reactance while blocking any leakage from the output branch. Similarly, the output BPF is tuned such that it delivers the subharmonically generated signal to the load while blocking the input (pump) power from passing directly to the output port.

Given that a pump voltage of $\mathrm{V_d} \cdot \sin(\omega \mathrm{t})$ is resulting across the varactor-diode, then the modulated varactor-diode capacitance can be expressed as $\mathrm{C(t)} = \mathrm{C_0}/[1 - \mathrm{V_d}/\phi \cdot \sin(\omega \mathrm{t})]^{\gamma}$ [23], where $\mathrm{C_0}$ is the zero-biased capacitance, γ is the capacitance exponent (e.g., $\simeq 0.5$), and ϕ is the barrier potential ($\simeq 0.7\mathrm{V}$). According to [23], the network with the varactor diode can be converted and modeled by a single RLC resonator tank (Fig. 3), where $\mathrm{C_T}$ represents the varactor's inherent capacitance, $\mathrm{L_T}$ is the derived parallel equivalent inductance from $\mathrm{Z_{BPF1}}||\mathrm{Z_{BPF2}}$ at $\omega/2$ (where $\omega = 2\pi \mathrm{f_{in}}$), and $\mathrm{R_T}$ models the equivalent shunt resistance at the varactor diode. The negative resistance ($\mathrm{R_N} < 0$) resulting from the pumped varactor diode reaches $|\mathrm{R_N}| = \mathrm{R_T}$ as the parametric oscillation enters the steady state, and the total voltage across the diode can be approximated using the following equation from [23]:

$$V_{tot}(t) \simeq V_{dt} \cdot sin(\omega t + \pi/2) + V_{ds} \cdot sin(\omega t/2), \tag{2}$$

where:

V_{dt} is the peak steady-state pump voltage,

V_{ds} is the peak subharmonic voltage at the diode.

The peak voltage of the pump signal at steady state is defined as $\mathrm{V_{dt}} = 4\phi/(\omega \mathrm{C_0 R_T} \gamma)$, and the peak volt-

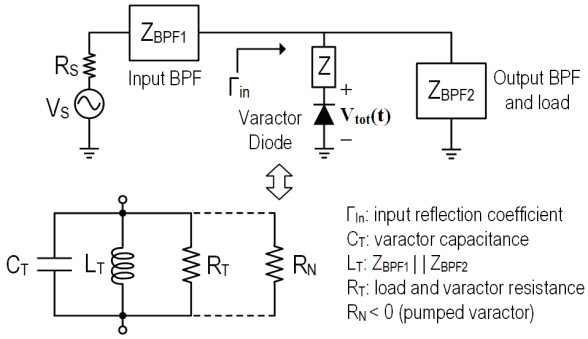

Fig. 3. Generalized representation of a parametric frequency divider and its RLC equivalent circuit model.

age of the subharmonic component at $f_{in}/2$ is defined as $V_{ds} = [R_T V_{dt}^2 |\Gamma_{in}|^2 / R_S]^{0.5}$, where Γ_{in} and R_s are the reflection coefficient and the pump impedance labeled in Fig. 3.

In order for the subharmonic frequency generation to be activated, the input pump power needs to exceed a certain value known as the power threshold (P_{th}). This P_{th} mainly depends on the total losses of the filter sections and the diode according to the following equation from [30]:

$$P_{th} = \frac{1}{8R_S} \left| \frac{4C_0^2 R_{in} R_{out} \omega_{out}^2}{C_d} \right|^2 \quad (3)$$

In equation (3), C_0 is the zero-bias capacitance, C_d is the tuning range of the varactor-diode's capacitance, ω_{out} is the resonance frequency of the output BPF, R_S is the terminal resistance of the input port, R_{in} and R_{out} are the equivalent resistances of both the input and output BPFs at resonance. The value of P_{th} can be optimized to obtain the minimum possible threshold value for a given PFD circuit as in [30]. Equation (3) provides insights for the selection of the critical nonlinear components (i.e., varactor diode) as well as the optimization of the input/output BPFs, such that a low input pump power can be achieved. A corresponding design strategy has also been verified in previous works [30], [31].

III. Proposed PFD: Design Considerations and Analyses of Key Characteristics

The PFD core in this work originates from the classic single-ended topology, which has been used in several variants with discrete components [13], [14], [23], [30], [32]. The efficient realization in CMOS technology required new auxiliary circuits and design strategies, which are described in this section. Impedance matching networks are avoided at the direct input and output of the PFD core to minimize layout area. Instead, the input driver and output stages are designed for on-chip transfer of input voltage (converted to current) and output voltage without 50-Ω terminations. Thus, contrary to our differential CMOS PFD design assessed through simulations in [31], the single-ended architecture in this paper does not include an LC-matching network and is current-driven to ease on-chip integration. Furthermore, the single-ended architecture avoids the impact of mismatches associated with differential driving signals, and consumes half of the die area and driving power compared to a differential implementation.

As indicated in recent PFD assessments [22], [30], [33], one of the top priorities during PFD design is to reduce the minimum input power/voltage (P_{th}/V_{th}) that is required to trigger the parametric frequency division. However, when transitioning from off-chip to on-chip realizations of parametric circuits, there are challenges that must be overcome to achieve operation with low voltage (or current) thresholds, which are related to three main aspects: 1) large chip area due to on-chip inductor/capacitor sizes, 2) reduced quality factor (Q) of on-chip inductors, and 3) layout parasitic resistance due to metal routing and vias connecting metal layers. Meanwhile, the driving of parametric systems in published works mainly relied on high-performance off-chip signal generators [13]–[15], [27], [28], [34], the use of on-chip transmission lines [8], [28], [35]–[37], and discrete matching/transformation networks on the test board [32], [33], [38], [39]; which create design barriers for on-chip integration into SoCs. Hence, a more area- and power-efficient approach with minimal hardware resources is required to accomplish the integration of PFDs within SoCs such as the on-chip phase noise reduction system in Fig. 1.

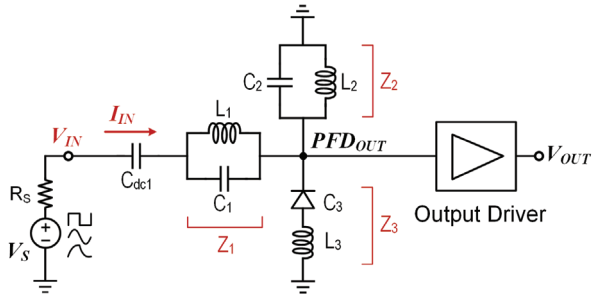

Fig. 4. PFD driving scheme exploration with three different types of input signals: square wave, sinusoidal wave, and the actual voltage waveform created by the PFD input driver in this work.

TABLE I
Component Parameters of the PFD Core (Fig. 4)

Inductor	Values	Capacitor	Values
L_1	2.65 nH	C_1	1.82 pF
L_2	0.954 nH	C_2	1.12 pF
L_3	2.59 nH	C_3^*	1.14 pF

C_3^*: capacitance of the P-type diode with zero bias at 2.4 GHz.

Fig. 4 displays the schematic of a classic single-ended PFD [30]–[32] within a preliminary simulation test bench to study the frequency division efficacy. An ideal RF source is connected to the input of the PFD, while the output is buffered using a macro-modeled output driver with negligible input impedance at the core node (i.e., PFD_{OUT}). The single-ended PFD core consists of three major resonant tanks: Z_1, Z_2 and Z_3, which are designed to get as close as possible to the following desired resonance conditions (derived in [30]) such that the 2:1 frequency division can be triggered with minimum RF power: (1) $Z_1 \to \infty$ at f_{out}, (2) $Z_2 \to \infty$ at f_{in}, (3) $Z_1 + Z_3 \to 0$ at f_{in}, and (4) $Z_2 + Z_3 \to 0$ at f_{out}. The selection of the varactor diode (C_3) and the corresponding optimization of the PFD core follow the same strategy as we outlined in [31], where it was found that a zero DC bias on the varactor diode will result in a minimum voltage threshold (V_{th}) in this process (i.e., 65-nm CMOS). A DC blocking capacitor (C_{dc1}) is located at the PFD input, which isolates the driving stage (V_S) from the DC ground formed by L_1 and L_2. The component parameters of the PFD core ($Z_1 \sim Z_3$) are listed in Table I. Considering area constraints in addition to limited Qs of on-chip inductors, we propose to drive the PFD without implementing an on-chip input matching network. However, since the input impedance of the PFD is relatively low at the input frequency (f_{in}) [30], [31], considerable amount of current can be drawn from the previous stage (i.e., I_{IN} drawn from V_S) given the same voltage threshold (i.e., $V_{IN,th}$). Therefore, an evaluation of the PFD input characteristics is required in advance of designing the input driving stage. Furthermore, the equivalent input capacitance of the PFD drivers (i.e., C_{in} in Fig. 1) should be minimized. The proof-of-concept PFD was designed to operate at $f_{in} = 4.8$ GHz with an output of $f_{out} = 2.4$ GHz in consideration of the abundant wireless standards around 2.4 GHz.

A. Current-mode PFD Driver with Inverter-based CLK Buffer

To evaluate the minimum required current to trigger the 2:1 frequency division (i.e., $I_{IN,th}$), we swept the input root-mean-square (RMS) current of the PFD (I_{IN}) by adjusting the ideal input voltage amplitude (V_{IN}) generated by V_S in Fig. 4. Both, square and sinusoidal, waveforms were tested as ideal driving signals to assess which driving conditions are more advantageous, where the square wave models the output of an ideal digital logic gate while the sinusoidal wave mimics a flawless output of a linear analog/RF stage (which would consume excessive power to meet linearity requirements). The corresponding simulation results are displayed in Fig. 5, where the PFD output voltage (V_{OUT}) at $f_{out} = 2.4$ GHz is plotted against the RMS input current (I_{IN}) of the PFD. The -60 dBV (1 mV) level is defined as the minimum detectable voltage level considering the signal-to-noise ratio (SNR) of the system in the presence of thermal/system noise. Correspondingly, the minimum RMS current that results in $V_{OUT} > -60$ dBV is defined as the low current threshold ($I_{IN,th}$) of the PFD. Note that the 2:1 frequency division can also cease at a high current limit due to the altered effective capacitance of the varactor diode ($C_{3,eff.}$) in the presence of large voltage swings across it. As can be seen in Fig. 5, the PFD driven by the ideal square wave has a 5.2 mA higher $I_{IN,th}$ value compared to the ideal sine wave, which is expected due to the unutilized power contents at multiple harmonics at frequencies other than $f_{in} = 4.8$ GHz. Hence, we can conclude that it is preferred to drive the PFD core with a pure sinusoidal signal that has high linearity.

However, designing a linear RF input driver stage that creates a sinusoidal output with an RMS current of 8.2 mA (Fig. 5) is not trivial with regards to linearity, bandwidth, on-chip biasing requirements; and would lead to significant power and area overhead compared to a driver that relies on switching operations. Therefore, instead of driving the PFD core with a linear stage such as a wide bandwidth power-hungry operational transconductance amplifier (OTA), we generate the required current ($I_{IN,th,RMS}$) by periodically switching the PFD input terminal between ground and a local DC voltage at $f_{switching} = f_{in}$. Fig. 6 displays the proposed PFD driver with an inverter-based clock signal (CLK) buffer

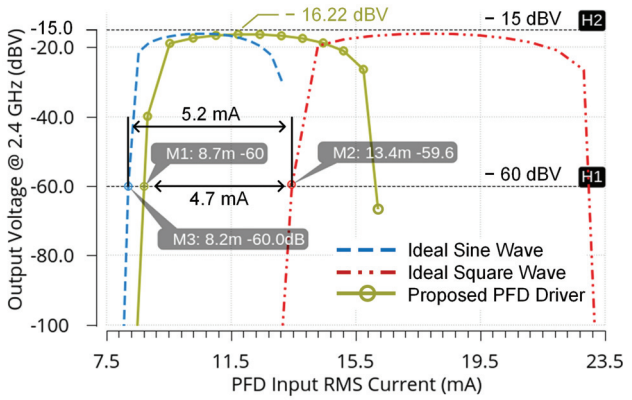

Fig. 5. Simulated PFD output voltage amplitude at $f_{out} = 2.4$ GHz vs. RMS input current with three different types of input signals as illustrated in Fig. 4.

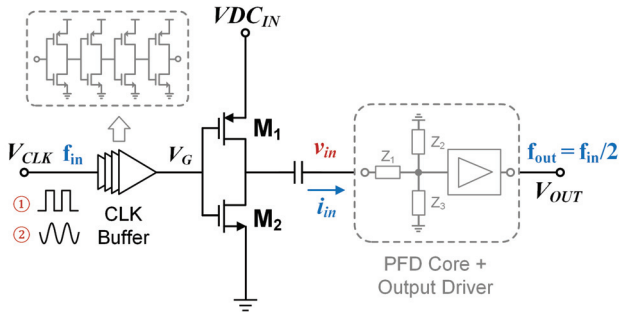

Fig. 6. PFD driver with inverter-based CLK buffer stage, which can be driven by either a square wave or a sinusoidal wave input signal.

TABLE II
COMPONENT PARAMETERS OF THE PROPOSED PFD DRIVER (FIG. 6)

Transistor	Dimensions
M_1	50 µm / 0.065µm
M_2	10 µm / 0.065µm

stage. VDC_{IN} is the local DC supply that is regulated and can be adjusted off-chip in this prototype. Transistors M_1 and M_2 alternately connect the PFD input to VDC_{IN} and ground, respectively. Both transistors share the common gate-control signal (V_G) and switch between the cutoff and linear regions to deliver currents. When V_G is low, then M_1 is turned on and the PFD core (i.e., $Z_1 \sim Z_3$) is directly charged by VDC_{IN}. On the other hand, the core will be discharged through M_2 when V_G is high. A DC blocking capacitor ensures that the input signal of the PFD core has a zero DC offset with time-varying voltage and current amplitudes of v_{in} and i_{in}, respectively. The switching transistors M_1 and M_2 are sized to minimize their resistance (R_{on}) when turned on. On the other hand, the potential impacts due to parasitic gate and drain capacitances of M_1 and M_2 were considered during transistor sizing, such that the output impedance of the driver (particularly due to the total parasitic capacitance) does not jeopardize the parametric resonance conditions, which ensures that the current threshold ($I_{IN,th}$) remains at a minimum.

The component parameters of M_1 and M_2 are included in Table II, where $R_{on,1} = 6.9\ \Omega$ and $R_{on,2} = 5.9\ \Omega$ were obtained through simulation. The equivalent output impedance of the PFD driver (i.e., M_1 and M_2) at $f_{in} = 4.8$ GHz is $19.58 + j3.88\ \Omega$, which was obtained through load-pull analysis. The simulated input impedance of the PFD core (Fig. 4) at $f_{in} = 4.8$ GHz is $39 + j9.5\ \Omega$. The V_{OUT} versus $I_{IN,RMS}$ curve of the PFD core driven by the proposed driver (Fig. 6) is plotted in Fig. 5 alongside those from simulations with ideal sine and square waves, where a $I_{IN,th}$ of 8.7 mA is obtained. Since the current flow through the on-resistances of M_1 and M_2 into the PFD core at resonance creates a sinusoidal-like voltage waveform, the proposed PFD driver presents a significant amount of reduction in RMS current compared to driving the PFD with an ideal square wave. The corresponding VDC_{IN} value is defined as the minimum required voltage threshold (i.e., $VDC_{IN,th}$) that delivers $I_{IN,th,RMS} = 8.7$ mA to the input of the PFD core. Simulations have confirmed that the input of the CLK buffer stage can be driven by either a rail-to-rail square wave or a rail-to-rail sinusoidal wave with a DC offset of $VDC_{IN}/2$ (Fig. 6), both of which have a negligible

difference (≤ 0.1 mA) with regards to their $I_{IN,th,RMS}$ values.

A 4-stage inverter-based CLK buffer was designed to drive the gate of M_1 and M_2 (Fig. 6). The minimum width and length allowed in this process were selected for the NMOS/PMOS in the first stage (here, $W_P = 200$ nm, $W_N = 120$ nm, $L = 65$ nm) such that the input capacitance (C_{in}) of the CLK buffer presents negligible loading on the previous stage. A W/L ratio scaling factor of $s \approx 4$ is applied to each stage of the inverters in the chain within the CLK buffer, which ensures the driving capability between stages as well as to generate the control gate (V_G) for M_1 and M_2. Thanks to the LC resonant tank at the PFD input (Z_1 in Fig. 4), the 3rd-harmonic (HD_3) of v_{in} generated with the proposed PFD driver with the abovementioned 4-stage CLK buffer is 32 dB in post-layout simulation, where the DC blocking capacitor and PFD core are included as output load.

B. Design of a Class-B Band-pass Filtering Output Stage

The analysis and supporting simulations in this subsection focus on the suppression of undesired harmonic components in order to provide insights into the design of band-pass filtering stages within PFDs. To suppress undesired signal components at the PFD output such as the residual component at f_{in} and other harmonics, and to maintain decent isolation with minimal power consumption, a class-B band-pass filtering (BPF) output stage was designed to extract the desired output frequency component directly from the PFD core (Fig. 7). A gate-to-ground bias resistor (R_{bias}) ensures that the NMOS transistor (M_3) remains off when there is no signal at its input. M_3 is sized to minimize the potential loading on the previous stage (i.e., PFD core) due to the gate capacitance. Alongside layout area considerations, the L and C values are selected following equation (4) such that the resonant frequency (f_0) is centered at f_{out} for optimal filtering. Table III provides the component parameters of the class-B BPF output stage design. Assuming an ideal LC tank with high quality (Q) factor that is close to infinity, the bandwidth (BW) of the tank is minimized such that the output harmonics at frequencies other than f_0 are greatly suppressed.

$$Z_{LC}(j\omega) = Z_L || Z_C = \frac{j\omega}{1-\omega^2 LC} \quad , \quad \omega_0 = \sqrt{\frac{1}{LC}} \tag{4}$$

However, the Q factors of on-chip inductors and capacitors are limited and further reduced by parasitic resistances due to

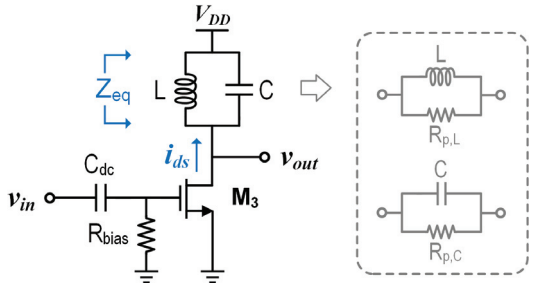

Fig. 7. Class-B BPF output stage with an inductor-capacitor (LC) tank in which passives are modeled with finite quality factors.

TABLE III
COMPONENT PARAMETERS OF THE PROPOSED CLASS-B BPF OUTPUT STAGE (FIG. 7)

Component	Values
M_3	50 µm / 0.5 µm
L	1.1 nH
C	4 pF
R_{bias}	10 kΩ
V_{DD1}	0.6 V

metal routing and contacts at device terminals. For this reason, finite Q_L and Q_C were defined using the parallel equivalent models as in [40], where $R_{p,L} = Q_L \cdot \omega L$, $R_{p,C} = Q_C/(\omega C)$, and the equivalent impedance of the LC tank can be obtained as $Z_{eq} = j\omega L || \frac{1}{j\omega C} || R_{p,L} || R_{p,C}$ (Fig. 7):

$$Z_{eq}(j\omega) = \frac{Q_L Q_C \omega L}{Q_L \omega^2 LC + Q_C + jQ_L Q_C(\omega^2 LC - 1)} \tag{5}$$

Fig. 8 displays the frequency responses of the load LC tank obtained from 1) calculation in MATLAB using equation (5), and 2) post-layout simulation in Cadence. The calculated 3-dB bandwidth (BW) of the LC tank is 130 MHz, ranging from 2.337 GHz to 2.467 GHz; while the simulated tank has a BW of 118 MHz, ranging from 2.342 GHz to 2.46 GHz. Both $|Z_{eq}|$ values peak at $f_0 = 2.4$ GHz, while the simulated $|Z_{eq}|_{max}$ is 0.8 dB higher than the calculated value in MATLAB, which is reasonably close for estimations during the early design process.

The small-signal output voltage (v_{out}) of the class-B BPF stage can be expressed as $v_{out} = i_{ds} \cdot Z_{eq}$, where i_{ds} represents the small-signal drain current that flows into the LC tank. Consequently, a suppression factor (F) can be defined to evaluate the band-pass filtering effect of the load LC tank for the reduction of the undesired input frequency component relative to the desired output component, where

$$F = \left| \frac{v_{out}(j\omega_{out})}{v_{out}(j\omega_{in})} \right| = \left| \frac{Z_{eq}(j\omega_{out})}{Z_{eq}(j\omega_{in})} \right| \tag{6}$$

The complete expression of F can be obtained by substituting $\omega = \omega_0, 2\omega_0$ while using equations (4) and (5) for the evaluations and rearrangements within equation (6):

$$F = \left| \frac{4Q_L + Q_C + j3Q_L Q_C}{2(Q_L + Q_C)} \right| \tag{7}$$

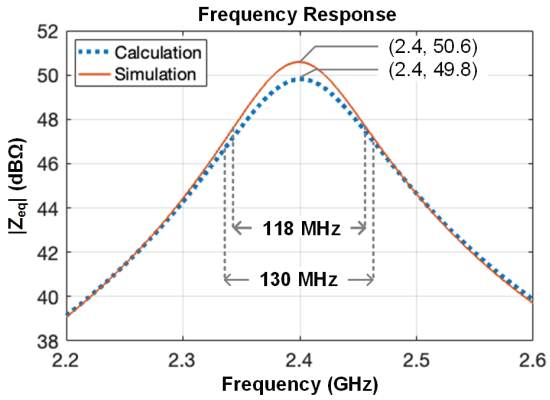

Fig. 8. Frequency responses of the load LC tank (in the class-B BPF stage) obtained from post-layout simulation and calculation based on equation (5).

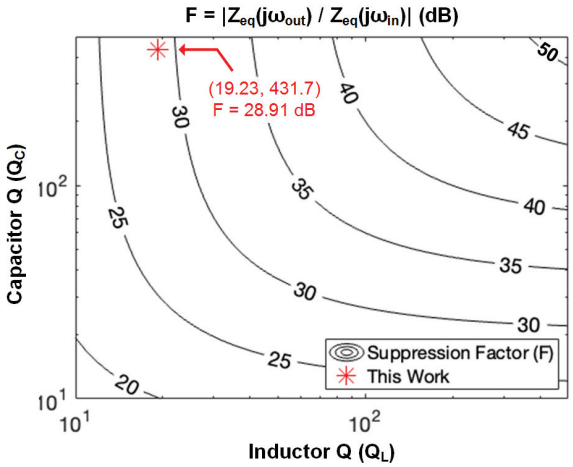

Fig. 9. Analytically calculated suppression factor F (in dB) considering finite quality factors due to parasitic resistance in the LC tank.

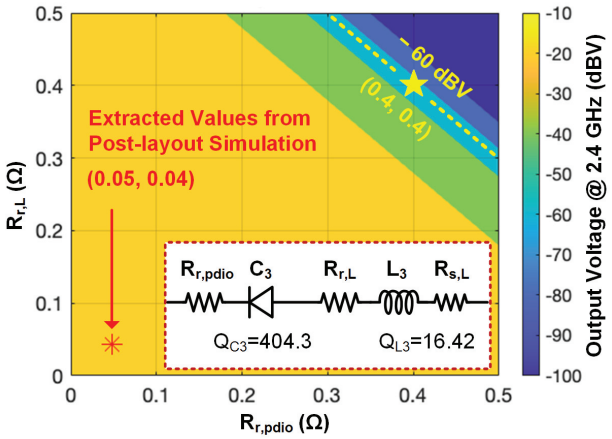

Fig. 10. Simulated output voltage (in dBV) at $f_{out} = 2.4$ GHz when series parasitic resistances within Z_3 are considered: $R_{r,pdio}$ and $R_{r,L}$ are the series parasitic routing/contact resistance of the P-type diode and inductor; and $R_{s,L}$ is the inherent series parasitic resistance within the inductor.

From the above equation, it can be observed that F is independent of L and C values but strongly relies on the Qs of the passive devices. The F versus Q_L and Q_C relationship [i.e., equation (7)] is illustrated in Fig. 9 using a contour map. Q_L and Q_C in the proposed class-B BPF driver are 19.23 and 431.7, respectively, which were extracted through post-layout simulations. These values correspond to an F factor of 28.91 dB as labeled in Fig. 9. On the other hand, an F value of 29.89 dB was obtained in post-layout simulations, where the small differences are due to the more complex and specific device models from the process design kit as well as impacts from the transistor parasitics.

C. Impact from Parasitic Resistances of the Series Diode-Inductor Connection in the PFD Core

Compared to the LC resonators with a metal-insulator-metal (MIM) capacitor and an inductor, the diode-inductor connection (i.e., C_3-L_3 as in Fig. 4) within the PFD core is more susceptible to parasitic resistances due to routing and via contacts between the high-level metal and diffusion layers, especially when the inductor is constructed with top-level metal. Following the series equivalent models in [40], ideal resistors that model parasitic resistance due to layout routing are included in-series with L_3 and C_3 (i.e., $R_{r,pdio}$ and $R_{r,L}$ as in Fig. 10) to assess the impact of parasitic resistances on parametric frequency division. Note that $R_{s,L}$ represents the inherent series resistance of the foundry-supplied model of inductor L_3, whereas that of the P-type diode selected in this work is negligible (i.e., $R_{s,pdio} \approx 0$).

Fig. 10 displays the simulated output voltage (in dBV) observed at 2.4 GHz in the presence of varying $R_{r,pdio}$ and $R_{r,L}$ values, where the PFD core and input/output driver stages are designed to ensure an optimal 2:1 frequency division with $f_{in} = 4.8$ GHz. As mentioned in Section III-A, since the minimum detectable output voltage at 2.4 GHz (i.e., $f_{out} = f_{in}/2$) is assumed to be -60 dBV here, it can be observed that the parametric frequency division will cease when $R_{r,pdio} + R_{r,L} > 0.8\ \Omega$. Considering that lower Q factors due to layout parasitic resistances will lead to higher V_{th} requirements to trigger the parametric frequency division [30], three particular layout design approaches were utilized for Z_3, such that the extracted parasitic resistance can be minimized as evaluated with post-layout simulations: 1) the diffusion area of the diode's cathode was expanded through layout customization to accommodate a larger via stack that connects the top-level metal to the bottom diffusion region (to minimize $R_{r,pdio}$), 2) multiple metal connections were added to the same layout node using top-level metal such that the equivalent contact resistance ($R_{r,pdio}$) is reduced through parallel routing connections, and 3) maximum path width was used to connect C_3 and L_3 on the thicker top-level metal with lower resistivity such that $R_{r,L}$ is minimized. With the above-mentioned strategies, the extracted quality factors and corresponding series-parasitic resistances due to routing/via contacts can be curbed at $R_{r,L} = 0.043\ \Omega$ and $R_{r,pdio} = 0.048\ \Omega$, which are listed in Table IV. Furthermore, post-layout simulations have confirmed that $R_{r,dio}$ can be reduced from 13.165 Ω to 0.048 Ω through layout customization, which ensures unimpaired frequency division after layout. Note that the output voltages in Fig. 10 were obtained with the complete PFD circuit, including the input/output drivers, which will be discussed in Section IV.

TABLE IV
EXTRACTED PARASITIC RESISTANCE AND Q FACTOR OF Z_3

	L_3	C_3
Q	16.42	404.3
$\mathbf{R_r^*}$	0.043 Ω	0.048 Ω

*R_r: series parasitic resistance due to metal routing and via contacts.

Alongside layout customizations to minimize parasitic resistances, a P-type diode was selected as the varactor diode (C_3) in this work. This has the benefit of allowing separate bulk connections in the layout (i.e., individual P-substrate within an N-well instead of a shared P-substrate with all NMOS devices), with which the PFD core having a 2.4 GHz output can be better isolated from the input driver chain that operates at 4.8 GHz.

TABLE V
COMPARISON WITH PREVIOUSLY REPORTED PFDS ON PCBS

Ref.	f_{in} (GHz)	P_{IN} (dBm)*	$I_{IN,RMS}$ (mA)**	Input TERM.	L_{max} (nH)	C_{max} (pF)
[13][a]	0.227	9	12.6	50-Ω	135	2.6
[14][a]	0.227	10.5	14.98	50-Ω	135	2.6
[26][a]	0.65	6	8.92	50-Ω	46	16
[27][b]	2	−16	0.71	50-Ω	*n/a*	*n/a*
[30][a]	0.2	−15	0.79	50-Ω	742.5	6.6
[41][a]	0.85	4	7.08	50-Ω	56	4.7
This[†]	**4.8**	*n/a*	**8.7**	**High-Z**	**2.65**	**1.82**

[a] Implemented on a PCB [b] Implemented using microstrip
[†] CMOS implementation *n/a*: not applicable or not reported

* Power level that appears at the input of the passive PFD core.
** Calculated RMS current at the PFD input based on the termination impedance.

D. Comparison of CMOS and PCB-level PFD Characteristics

The simulated specifications of this work are compared to other reported PFDs with discrete components in Table V. The RMS input current ($I_{IN,RMS}$) was calculated with the reported input power P_{IN} (dBm) and termination impedance, which in our case was extracted through simulations as discussed in Section III-A (Fig. 5). The maximum inductance (L_{max}) and capacitance (C_{max}) values utilized in each work are listed because the size of the inductors and capacitors is of practical relevance, particularly for on-chip implementations. Please note that P_{IN} in Table V represents the actual input power that is delivered to the passive PFD core, which is not applicable in our case because the proposed PFD core is driven by the custom-designed current-mode driver (Section III-A) instead of off-chip RF signal sources. Hence, $I_{IN,RMS}$ is included alongside P_{IN} for comparison.

Based on the summarized parameters in Table V, it can be observed that PFDs with microstrips [27] and off-the-shelf components ([13], [14], [26], [30], [41]) tend to be more suitable for operation at lower frequencies due to board-level parasitics. On the other hand, the CMOS PFD in this work allows to realize parametric frequency division with a 4.8 GHz input, as well as to balance the trade-off between operating frequency and chip area with relatively low inductor values. Furthermore, the relatively high input impedance of the PFD driver (Fig. 6) was designed to be capacitive (i.e., parasitic capacitance from transistor gates), such that it can be driven by either a square wave (e.g., common digital signal) or a sinusoidal wave input (e.g., on-chip VCO output) on the chip instead of relying on high-performance off-chip signal sources with 50-Ω termination.

IV. CMOS PFD IMPLEMENTATION ASPECTS

The complete schematic of the proposed on-chip PFD is displayed in Fig. 11, where the three key building blocks discussed Section III are cascaded in a chain: a current-driven PFD input driver with an inverter-based CLK buffer stage, a passive PFD core consisting of three LC resonators (i.e., $Z_1 \sim Z_3$), and a class-B band-pass filtering (BPF) output stage with a center frequency of 2.4 GHz. Considering the high target operating frequency (i.e, $f_{in} = 4.8$ GHz), $R_G = 50\ \Omega$ and $C_G = 20.2$ pF were added to the input stage of the CLK buffer to provide 50-Ω input impedance, which allows direct terminations with standard off-chip equipment that has 50-Ω ports. During measurements of the prototype chip, an RF signal generator was used alongside a passive bias-tee to generate the input signal for the CLK buffer. Within an SoC, the digital inverters in the CLK buffer can either be driven with an on-chip digital signal or a large-swing VCO/PLL output signal. Note that the DC level of the CLK buffer input (V_{CLK} in Fig. 11) is $VDC_{IN}/2$ such that the duty cycle of the CLK signal is 50%.

TABLE VI
COMPONENT PARAMETERS OF DC BLOCKING CAPACITORS (FIG. 11)

Component	Values	Dimensions
$\mathbf{C_{dc1}}$	1.01 pF	22 μm × 22.5 μm
$\mathbf{C_{dc2}}$	10.2 pF	71 μm × 71 μm
$\mathbf{C_{dc3}}$	5.02 pF	50 μm × 50 μm
$\mathbf{C_{dc4}}$	1.01 pF	22 μm × 22.5 μm

TABLE VII
COMPONENT PARAMETERS OF THE COMMON-SOURCE (CS) OUTPUT DRIVER FOR OFF-CHIP TESTING NEEDS (FIG. 11)

Component	Values
$\mathbf{M_4}$	70 μm / 0.13 μm
$\mathbf{M_5}$	20 μm / 0.12 μm
$\mathbf{R_F}$	500 Ω
$\mathbf{V_{DD2}}$	1.2 V

Simulations were also conducted to confirm the robustness of the PFD with different input signal conditions. When driven by a rail-to-rail sinusoidal wave with a passive DC bias-tee (i.e., as in Fig. 11), the input DC level must remain within $0.38\ V \sim 0.77\ V$ to maintain the parametric frequency division with stable output amplitude. On the other hand, a duty cycle range of 38%∼67% is required if the input stage is driven directly by a rail-to-rail square wave (e.g., from a digital CMOS logic gate). Both cases were evaluated under nominal operating conditions (i.e., $f_{in} = 4.8$ GHz, $VDC_{IN} = 1.2$ V, room temperature, typical process corner).

DC-blocking capacitors were inserted in the signal paths (i.e., C_{dc1} to C_{dc4}) to eliminate the undesired current paths from voltage supplies to ground and to ease the biasing of individual stages. L_2 and L_3 provide the zero DC-bias for the varactor-diode (C_3) as mentioned in Section III, which has been shown to be optimal to achieve minimum V_{th} for the triggering of the 2:1 frequency division [30], [31]. The cutoff frequency of the high-pass filter formed by R_{bias} and C_{dc2} is 1.6 MHz, which presents negligible attenuation to the frequency of interests (here, $f_{in} = 4.8$ GHz and $f_{out} = 2.4$ GHz). Table VI lists the dimensions and capacitance values of all DC blocking MIM capacitors. Simulations have confirmed that C_{dc1} was sized to assure an optimum PFD operation at a 2.4 GHz output frequency. The total loss due to the insertions of $C_{dc2} \sim C_{dc4}$ as well as layout parasitic capacitances/resistances is negligible ($\leq$ 0.1 dB) based on post-layout simulations.

A self-biased complementary common-source (CS) amplifier was added at the output only to drive the 50-Ω off-chip load for testing purposes (i.e., V_{TEST}). Hence, the actual load at the PFD output (i.e., V_{OUT}) comes from the equivalent input impedance of the CS output driver. Table VII summarizes the component parameters of the CS output driver. Note that

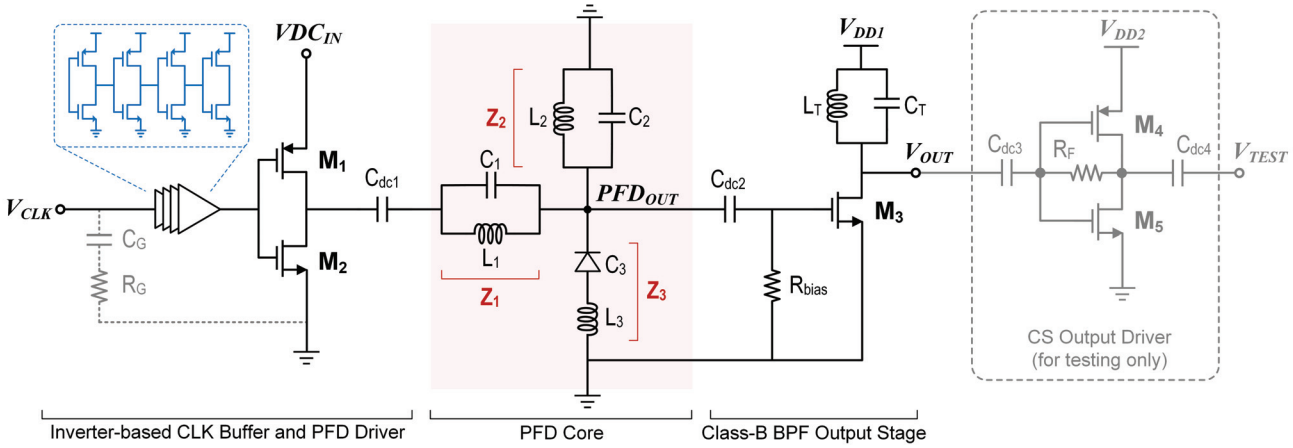

Fig. 11. Schematic of the proposed current-driven PFD designed for 2.4 GHz output frequency, consisting of a current-mode PFD input driver with an inverter-based CLK buffer stage, a completely passive PFD core, a class-B BPF output stage with a center frequency of 2.4 GHz, and a complementary common-source (CS) output driver (only required for off-chip measurements).

the DC voltage of the PFD input driver ($\mathrm{VDC_{IN}}$) and the clock input ($\mathrm{V_{CLK}}$) are both adjustable on the printed circuit board (PCB) for this prototype in order to investigate the optimal operating points for the evaluation of parametric frequency division, as discussed in Section V.

The performance of the PFD was evaluated in the presence of process-voltage-temperature (PVT) variations, where we selected three process corners [SS, TT, FF] and three temperature corners [$-40°$C, $27°$C, $85°$C] to assess the impacts of nine process-temperature (P-T) combinations on PFD characteristics including the center of the operating frequency range ($\mathrm{f_{out}}$) and the current threshold ($\mathrm{I_{IN,th,RMS}}$). The simulated PFD center frequency ($\mathrm{f_{out}} = \mathrm{f_{in}}/2$) varies from 4.4 GHz to 5.2 GHz, whereas all P-T corners provide a decent output voltage at $\mathrm{f_{in}}/2$ (i.e., ≥ -26 dBV). Correspondingly, the current threshold ($\mathrm{I_{IN,th,RMS}}$) varies from 6.21 mA to 9.98 mA. Furthermore, simulations with supply voltage variations ($\mathrm{V_{DD1}}$ and $\mathrm{V_{DD2}}$) were conducted at the nominal corner [TT, $27°$C], in which both supply voltages were varied by $\pm 5\%$ based on their nominal values (i.e., $\mathrm{V_{DD1}} = 0.57$ V, 0.6 V, 0.63 V; $\mathrm{V_{DD2}} = 1.14$ V, 1.2 V, 1.26 V). In the presence of simulated supply voltage variations for $\mathrm{V_{DD1}}$ and $\mathrm{V_{DD2}}$, the $\mathrm{V_{OUT}}$ value at $\mathrm{f_{out}} = 2.4$ GHz varies from -18.23 dBV to -16.22 dBV.

Following the same layout optimization strategy as discussed in Section III-C, individual ground connections and layout pads were assigned to the input driver, PFD core, and output driver; which helps enhance the isolation among the input stages, resonating core, and output stage. Note that this design process did not involve electromagnetic (EM) simulations. Standard foundry-supplied device models were used for active and passive devices during circuit simulations, parasitic extractions and post-layout simulations with Cadence tools.

V. Measurement Results and Discussion

A prototype PFD chip was fabricated in a standard 65-nm CMOS process. Fig. 12 displays the micrograph of this PFD, where $\mathrm{Z_1}$, $\mathrm{Z_2}$ and $\mathrm{Z_3}$ of the PFD core, as well as the resonant LC tank of the class-B BPF output stage (Fig. 11), are placed in a concentric circle for efficient layout area use. The

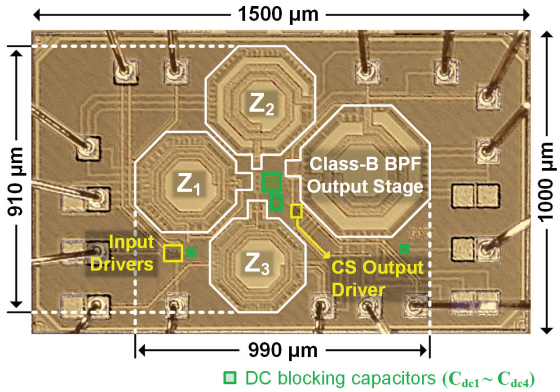

Fig. 12. Micrograph of the fabricated PFD die with the circuits in Fig. 11.

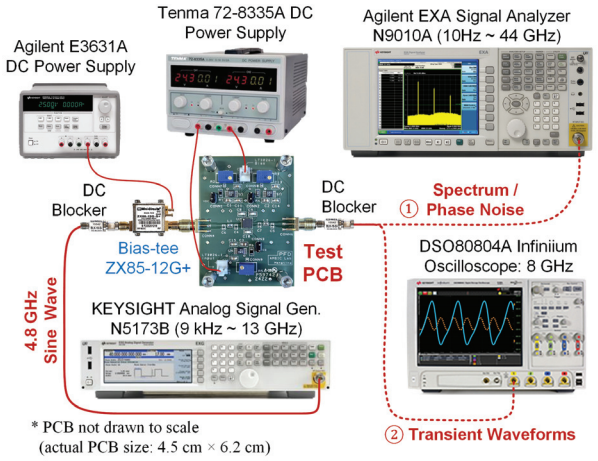

Fig. 13. Measurement setup for the prototype chip characterization.

input/output drivers are placed in the periphery of the inductors to shorten the signal paths. Multiple ground pads are connected to the inductor bulks and PFD ground pins to reduce the effective inductance due to bonding and to evenly distribute on-chip current flows to low-impedance ground. The active area of the complete PFD is 0.99×0.91 mm^2, excluding bonding pads and electrostatic discharge (ESD) protection devices, whereas the complete prototype chip occupies 1.5×1 mm^2.

The measurement setup to test the prototype PFD chip is displayed in Fig. 13, where the test equipment is arranged to evaluate: (1) the PFD output spectra and phase noise, and (2)

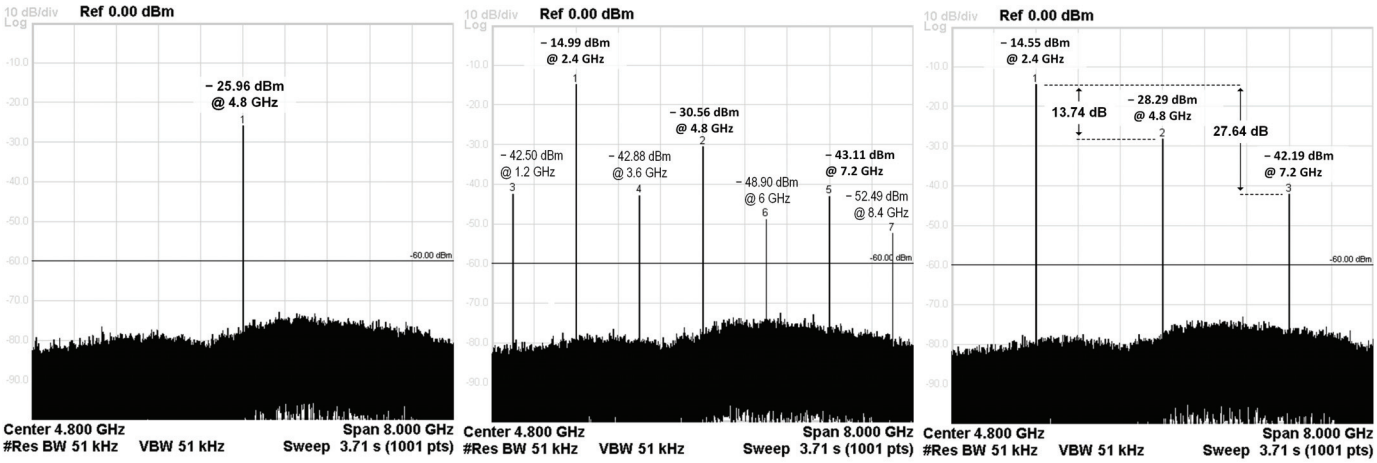

Fig. 14. Measured output spectra of the PFD operating at $f_{in} = 4.8$ GHz with a driver supply voltage of (a) VDC_{IN} = 1.3 V ($< VDC_{IN,th}$), (b) VDC_{IN} = 1.4 V ($\approx VDC_{IN,th}$), and (c) VDC_{IN} = 1.5 V ($> VDC_{IN,th}$), respectively.

the transient waveforms of the PFD output under different operating conditions (i.e., when PFD is dividing and not dividing). Note that only one of the instruments is connected to the PFD output during each measurement (i.e., either the N9010A signal analyzer or the DSO80804A oscilloscope). As illustrated in Fig. 13, the sinusoidal input signal of the PFD was generated with an N5173B signal source with zero DC offset. The gate bias of the digital CLK buffer in Fig. 11 is provided by a DC power supply (E3631A) through a passive off-chip bias-tee (ZX85-12G+). The second DC power supply (72-8335A) provides the supply voltages for the off-chip voltage regulators on the printed circuit board (PCB), such that VDC_{IN}, V_{DD1} and V_{DD2} in Fig. 11 are well-regulated.

Fig. 14 displays the measured output spectra of the PFD operating at $f_{in} = 4.8$ GHz, where the supply voltage of the PFD driver (VDC_{IN} in Fig. 6 and Fig. 11) was swept to locate the voltage threshold ($VDC_{IN,th}$) that triggers the 2:1 frequency division. It can be observed that the parametric frequency is triggered when $VDC_{IN} \approx 1.4$ V [Fig. 14 (b)], where three frequency components including $f_{in}/2$, f_{in} and $3 \cdot f_{in}/2$ (here, 2.4 GHz, 4.8 GHz and 7.2 GHz, respectively) stand out alongside multiple harmonic components of $N \cdot f_{in}/4$ ($N = 1, 3, 5, 7$). When VDC_{IN} is increased to 1.5 V, the power difference between f_{in} and $f_{in}/2$ is maximized under this test condition, whereas the $N \cdot f_{in}/4$ components ($N = 1, 3, 5, 7$) are completely suppressed. Therefore, we can conclude that the presented PFD has an inherently low threshold of $VDC_{IN,th} = 1.4$ V at $f_{in} = 4.8$ GHz, while the optimum operating point is $VDC_{IN} = 1.5$ V, where a power difference of 13.74 dB is achieved between f_{in} and f_{out}. The corresponding CS driver output power (P_{out}) at 2.4 GHz is -14.55 dBm, as labeled in Fig. 14 (c). The 3rd harmonic distortion (HD_3) of the PFD output (at $3 \cdot f_{out} = 7.2$ GHz) is 27.6 dB lower than the fundamental output frequency component. Note that the power at $f_{in} = 4.8$ GHz includes the feed-through due to the package/board parasitics on the test PCB. Despite of the feed-trough component of -28.29 dBm at 4.8 GHz [Fig. 14 (c)], the obtained PFD output shows negligible deviations at its zero-crossing points in the time domain, which was also confirmed by simulating the complete PFD

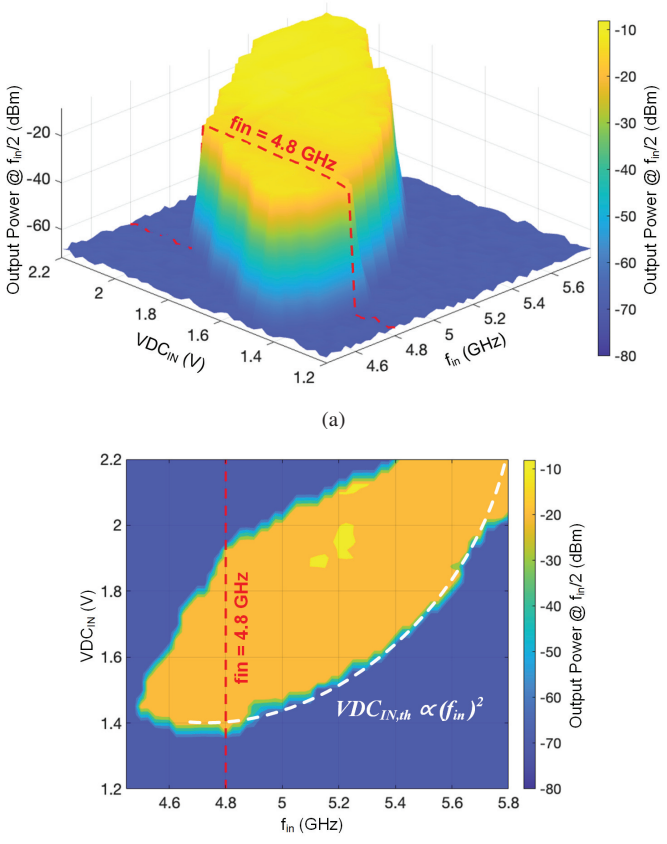

Fig. 15. Measured PFD output power at $f_{out} = f_{in}/2$ when sweeping the input clock frequency (f_{in}) alongside a varying supply voltage of the PFD input stage (VDC_{IN} in Fig. 11): (a) 3D-view and (b) contour map.

(with bonding pads and ESD protections devices) and comparing the simulated zero-crossing value to an ideal 2.4 GHz signal with and without modeled input-output feed-trough at 4.8 GHz. The transient measurement results reported at the end of this section provide further confirmation. Meanwhile, the measured power consumption at the optimum operating point is 9.1 mW, which includes the 400 µW that is consumed by the class-B BPF stage with a 0.6 V supply (Fig. 7, Table III).

To explore the full-scale operating range of the fabricated

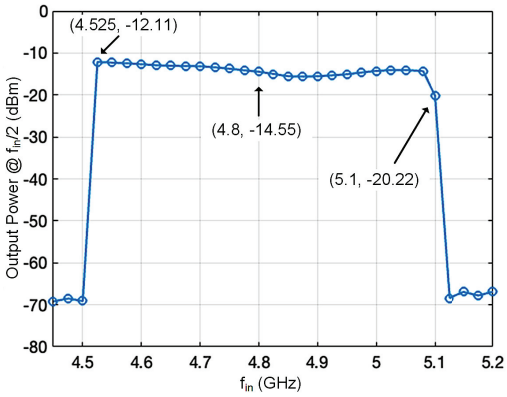

Fig. 16. Measured output power (P_{out}) at $f_{out} = f_{in}/2$ versus input frequency (f_{in}), where $VDC_{IN} = 1.5$ V.

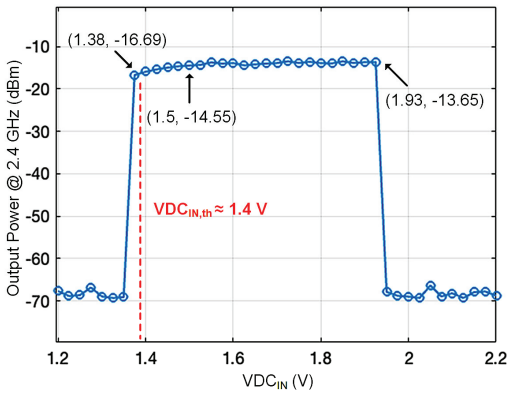

Fig. 17. Measured output power (P_{out}) at $f_{out} = 2.4$ GHz versus local DC supply voltage (VDC_{IN}) of the PFD input driver.

PFD, both input frequency (f_{in}) and driver supply (VDC_{IN}) were swept over a wide range: f_{in} was swept from 4.45 GHz to 5.8 GHz, while VDC_{IN} was swept from 1.2 V to 2.2 V. The power level of the PFD output at $f_{out} = f_{in}/2$ was measured with a spectrum analyzer and used to construct the power map in the presence of varying f_{in} and VDC_{IN}. The resulting 3-dimensional (3D) power map and contour map are displayed in Fig. 15 (a) and (b) respectively, from which we can observe that the PFD output power at $f_{in}/2$ is at a significantly higher level when the 2:1 frequency is triggered. It can be noticed that the minimum required DC supply of the PFD (i.e., $VDC_{IN,th}$) and corresponding input RMS current (referred to as $I_{IN,th}$ in Section III-A) are proportional to the square of the PFD input frequency $(f_{in})^2$, which agrees with the analytical quadratic relationship between V_{th} and f_{in} derived in [30]. An operating bandwidth of around 600 MHz is also observed over half of the VDC_{IN} range as in Fig.15 (b). $f_{in} = 4.8$ GHz is labeled in both Fig. 15 (a) and (b) as the frequency-by-design, where the lowest $VDC_{IN,th}$ can be obtained at ($VDC_{IN} \approx 1.4$ V, $f_{in} = 4.8$ GHz).

Fig. 16 displays the measured operating frequency range of the PFD when 1.5 V of VDC_{IN} is applied to the input stage, where the PFD output power at $f_{in}/2$ is plotted against f_{in}. An average output power of -15 dBm can be observed between $f_{in} = 4.525$ GHz and $f_{in} = 5.1$ GHz, which represents an operating bandwidth of 575 MHz. The center operating frequency of the PFD with $VDC_{IN} = 1.5$ V is 4.8 GHz, where the output power at $f_{out} = 2.4$ GHz is -14.55 dBm. Fig. 17 shows the measured operating voltage range of the PFD at $f_{out} = 2.4$ GHz, where the voltage threshold of $VDC_{IN,th} \approx 1.4$ V can be observed. The PFD operates within a range of DC voltages (VDC_{IN}) for the input driver in Fig. 11. During characterization measurements, VDC_{IN} was increased from 1.2 V (no division) until a clear parametric frequency division is visible at $VDC_{IN} \approx 1.4$ V, which implies that the PFD driver shown in Fig. 11 is delivering the minimum required input RMS current ($I_{IN,th,RMS}$) to the PFD core with $VDC_{IN} = 1.4$ V. Note that the corresponding $VDC_{IN,th}$ range also varies at different input frequencies as illustrated in Fig. 15. The PFD stops dividing at $VDC_{IN} \approx 1.9$ V with $f_{in} = 4.8$ GHz as a result of the altered effective capacitance of the varactor diode (C_3) in the PFD core (Fig. 11) due to the large voltage swing across the varactor.

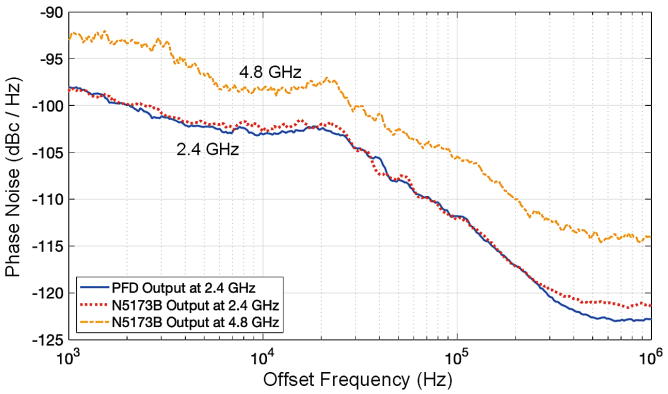

Fig. 18. Measured PFD output phase noise compared to the phase noise of the RF signal generator with –14.55 dBm signal power.

The phase noise of the PFD output was measured over an offset frequency range of 1 kHz∼1 MHz, which is displayed in Fig. 18. With $f_{in} = 4.8$ GHz as the operating frequency by design, the carrier frequency during the phase noise measurement was set to the 2.4 GHz output frequency. For comparison, the phase noise curves of the RF signal generator at both 4.8 GHz and 2.4 GHz with the same power level as the PFD output (i.e., -14.55 dBm) are plotted alongside that of the PFD output. The expected phase noise reduction through frequency division can be observed when comparing the results at the two frequencies. Furthermore, the small phase noise difference between the PFD output and RF source signal at the same frequency of interest (i.e., 2.4 GHz) demonstrates that the phase noise contribution due to active devices (i.e, transistors) in the proposed PFD is negligible, which is particularly helpful for the primary target application (Fig. 1) such that the closed-loop system can lead to overall phase noise reduction [13]–[15]. The phase noise of the PFD output shows slight improvement at high offset frequencies (0.3 MHz to 1 MHz) due to the inherent filtering of passive LC resonators.

The transient waveforms of the fabricated PFD were captured using a high-frequency oscilloscope (DSO80804B). Two output conditions of the PFD are displayed in Fig. 19 with the peaks and periods labeled: 1) $f_{in} = 4.8$ GHz, $VDC_{IN} = 1.5$ V, where the 2:1 frequency division is triggered; 2) $f_{in} = 4.8$ GHz, $VDC_{IN} = 1.3$ V, where the PFD is

TABLE VIII
COMPARISON WITH OTHER REPORTED ON-CHIP FREQUENCY DIVIDERS

Ref.	**Division Ratio**	**CMOS Process** (nm)	$\mathbf{f_{in}}$ (GHz)	**Area** (mm^2)	$\mathbf{P_{in}}$ (dBm)	**Power** (mW)	$\mathbf{V_{DD}}$ (V)	**Power Eff.** (GHz/mW)
[28]	2	130	18.5 - 23.5	0.24	*n/a*	9.6 (buffer)	1.2	1.93 - 2.45
[42]	3	180	4.39 - 8.82	1.035	0	6.76	0.9	0.64 - 1.3
[43]	2	180	1.82 - 2.04	0.65	0	4.5	0.75	0.4 - 0.453
[44][a]	2	65	0.1 - 5.3	*n/a*	0	0.55	1	0.18 - 9.63
[45]	2	180	5.65 - 11.89	0.66	0	2.57	0.6	2.2 - 4.63
[46][b]	3	65	14.85	0.09	*n/a*	1.56	1.2	9.52
[47]	2	130	5	0.001	*n/a*	0.47	1.2	10.64
[48]	3	180	1 - 3.0	0.1	3	12.6 (core)	1.8	0.08 - 0.24
[49]	2	180	5.8	0.002	0	3.24	1.8	1.79
This Work	**2**	**65**	**4.8**	**0.81**	**0**	**8.7 (driver) + 0.4 (buffer)**	**1.4***	**0.53**

[a] post-layout simulation [b] simulation *n/a*: not applicable or not reported
* Minimum required VDC_{IN} for the PFD input driver, whereas the V_{DD} of the BPF buffer and test output driver are 0.6 V and 1.2 V respectively.

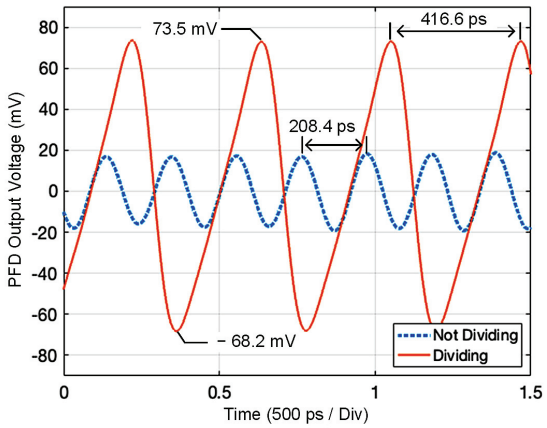

Fig. 19. Measured transient PFD output waveforms when dividing / not dividing with $f_{in} = 4.8$ GHz.

not dividing. The average value of the measured zero-crossing in Fig. 19 (when the PFD is dividing) deviates from the ideal zero-crossing instant by 0.4 ps, which is approximately 0.1% shift of the nominal period of the 2.4 GHz signal. Therefore, the slight deviations in the measured PFD output still allow sufficient capability in applications such as local oscillator signal generation for hard-switching mixers or clock signal generation based on zero crossings.

Table VIII summarizes the measured parameters of the proposed PFD alongside other reported CMOS frequency dividers (measurement results unless mentioned otherwise). Compared to injection-locked frequency dividers (ILFDs) [42]–[47] and digital frequency dividers ([48], [49]), on-chip parametric frequency dividers including [28] and this work tend to consume more power and die area. However, the exploration of on-chip PFDs and their characteristics serves as the cornerstone of new integrated applications such as phase noise reduction (i.e., PFIL) [13]–[15], frequency-selective limiters [33], as well as sensors with high sensitivity and tunable threshold [22]. The proposed PFD driver (with 8.7 mW of power consumption) achieves the on-chip excitation of the purely passive PFD core. The high-impedance input of the PFD driver can be connected to either a conventional digital clock signal or the output of an on-chip VCO. Apart from the avoidance of using area-consuming transmission lines, this PFD can be integrated into systems without off-chip signal sources, discrete matching networks or 50-Ω terminations. Even though it is outside the scope of this paper, 4-phase IQ signal generation can be explored in future works by converting the proposed single-ended PFD to a fully differential topology, since IQ signal generation has been demonstrated with parametric capacitance modulation in [7]. Compared to digital frequency dividers, the built-in filtering from the on-chip LC resonators allows to achieve lower noise and reduced output harmonics, which will benefit in the primary target applications. Nonetheless, instead of aiming to replace conventional frequency dividers in systems such as PLLs, the proposed PFD was designed as the key building block for the envisioned on-chip PFIL system and for other systems based on unique parametric properties.

VI. CONCLUSION

An on-chip current-driven parametric frequency divider (PFD) in a standard 65-nm CMOS process has been demonstrated for the first time in the sub-6 GHz frequency range. The complete PFD consists of a resonator core, a current-mode input driver with a CLK buffer stage, and a class-B output stage with bandpass filtering, which is designed to operate at 4.8 GHz with a 1.5 V supply and to provide a 2:1 frequency division. The input-driving conditions were assessed and a current-mode input driver circuit was constructed, which can be operated with on-chip digital or large-swing analog voltage waveforms. The current-mode driver triggers the parametric frequency divider with an input RMS current of 8.7 mA. Furthermore, a class-B BPF output stage was designed to extract the PFD output signal without an on-chip matching network, and the bandpass filtering benefit of the class-B stage was analyzed and discussed. The degradation in the quality factor (Q) of passive devices due to metal routing and via contacts in the layout was evaluated, and corresponding design suggestions were provided for the resonator core.

The fabricated PFD occupies an area of 0.99×0.91 mm^2, excluding pads and ESD circuitry. The PFD architecture is scalable for different frequency ranges (limited by on-chip inductor and capacitor values) because it does not contain on-chip transmission lines. The measurement results demonstrated the feasibility and performance of the PFD design approach. The input frequency and the supply voltage of the input driver

were swept from 4.45 GHz to 5.8 GHz and 1.2 V to 2.2 V in order to characterize the operating range of the 2:1 parametric frequency division. A minimum required supply voltage of $\mathrm{VDC_{IN}} = 1.4$ V was achieved for the triggering of the 4.8 GHz to 2.4 GHz frequency division, which leads to a total power consumption of 9.1 mW. The optimum operating point of the PFD is at $\mathrm{f_{in}} = 4.8$ GHz with a supply voltage of $\mathrm{VDC_{IN}} = 1.5$ V, where the PFD output power at 2.4 GHz is -14.55 dBm.

ACKNOWLEDGMENT

The authors thank Dr. Keng Chen, Dr. Mahmoud A. A. Ibrahim, and Thomas Gourousis for valuable discussions.

REFERENCES

[1] M. E. Hines, "The virtues of nonlinearity-detection, frequency conversion, parametric amplification and harmonic generation," *IEEE Trans. Microw. Theory Tech.*, vol. 32, no. 9, pp. 1097–1104, Sept. 1984.

[2] A. Cullen, "A travelling-wave parametric amplifier," *Nature*, vol. 181, no. 4605, pp. 332–332, Feb. 1958.

[3] R. F. Miracky and J. Clarke, "Simulation of the noise rise in three-photon josephson parametric amplifiers," *Appl. Physics lett.*, vol. 43, no. 5, pp. 508–510, June 1983.

[4] B. Yurke, L. Corruccini, P. Kaminsky, L. Rupp, A. Smith, A. Silver, R. Simon, and E. Whittaker, "Observation of parametric amplification and deamplification in a josephson parametric amplifier," *Physical Rev. A*, vol. 39, no. 5, p. 2519, Oct. 1989.

[5] A. Giarola, D. Jackson, R. Orth, and W. Robbins, "A frequency-selective limiter using magnetoelastic instability," *Proc. IEEE*, vol. 55, no. 4, pp. 593–594, Apr. 1967.

[6] K. Kotzebue, "Frequency-selective limiting," *IRE Trans. Microw. Theory Tech.*, vol. 10, no. 6, pp. 516–520, Nov. 1962.

[7] K. Bhardwaj and T. H. Lee, "A phase-interpolation and quadrature-generation method using parametric energy transfer in CMOS," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 62, no. 5, pp. 1250–1259, Apr. 2015.

[8] N. Zhang, L. Belostotski, and J. W. Haslett, "Relations of time-varying circuit parameters and idlerless parametric harmonic generation for reconfigurable frequency multipliers," *IEEE Trans. Microw. Theory Tech.*, vol. 69, no. 5, pp. 2554–2568, Mar. 2021.

[9] S. Magierowski, H. Chan, and T. Zourntos, "Subharmonically pumped RF CMOS paramps," *IEEE Trans. Electron. Devices*, vol. 55, no. 2, pp. 601–608, Jan. 2008.

[10] S. Magierowski, T. Zourntos, J.-F. Bousquet, and Z. Zhao, "Compact parametric downconversion using MOS varactors," in *Proc. IEEE MTT-S Int. Microw.Symp. Dig.*, pp. 1377–1380, July 2009.

[11] Z. Zhao, S. Magierowski, and L. Belostotski, "35.5 GHz parametric CMOS upconverter," *IEEE Microw. and Wireless Components Lett.*, vol. 22, no. 9, pp. 477–479, Aug. 2012.

[12] Z. Zhao, J.-F. Bousquet, and S. Magierowski, "Coherent parametric RF downconversion in CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, pp. 377–380, May 2010.

[13] C. Cassella, N. Miller, J. Segovia-Fernandez, and G. Piazza, "Parametric filtering surpasses resonator noise in ALN contour-mode oscillators," in *Proc. IEEE Int. Conf. on Microelectromech. Syst. (MEMS)*, pp. 1269–1272, 2014.

[14] C. Cassella and G. Piazza, "Low phase-noise autonomous parametric oscillator based on a 226.7 MHz AlN contour-mode resonator," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 62, no. 4, pp. 617–624, Apr. 2015.

[15] C. Cassella, S. Strachan, S. W. Shaw, and G. Piazza, "Phase noise suppression through parametric filtering," *Appl. Physics Lett.*, vol. 110, no. 6, p. 063503, Feb. 2017.

[16] J. Guckenheimer and P. Holmes, *Nonlinear oscillations, dynamical systems, and bifurcations of vector fields*. Springer Science & Business Media, 2013.

[17] K. Wang, B. Otis, and Z. Wang, "A 580-μW 2.4-GHz ZigBee receiver front end with transformer coupling technique," *IEEE Microw. and Wireless Components Lett.*, vol. 28, no. 2, pp. 174–176, Feb. 2018.

[18] E. Kargaran, D. Manstretta, and R. Castello, "A sub-1V, 220 μW receiver frontend for wearable wireless sensor network applications," in *Proc. IEEE Int. Symp. on Circuits and Syst. (ISCAS)*, pp. 1–5, 2018.

[19] L. Xu, C.-H. Chang, and M. Onabajo, "A 0.77 mW 2.4 GHz RF front-end with −4.5 dBm in-band IIP3 through inherent filtering," *IEEE Microw. and Wireless Components Lett.*, vol. 26, no. 5, pp. 352–354, May 2016.

[20] M. A. Ibrahim and M. Onabajo, "A low-power BFSK transmitter architecture for biomedical applications," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 67, no. 5, pp. 1527–1540, May 2019.

[21] M. A. Ibrahim and M. Onabajo, "A 0.061 nJ/b 10 Mbps hybrid BF-PSK receiver for Internet of Things applications," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 69, no. 5, pp. 1919–1931, Feb. 2022.

[22] H. M. Hussein, M. Rinaldi, M. Onabajo, and C. Cassella, "Capturing and recording cold chain temperature violations through parametric alarm-sensor tags," *Appl. Physics Lett.*, vol. 119, no. 1, p. 014101, July 2021.

[23] G. R. Sloan, "The modeling, analysis, and design of filter-based parametric frequency dividers," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 2, pp. 224–228, Feb. 1993.

[24] A. Lipparini, E. Marazzi, and V. Rizzoli, "A new approach to the computer-aided design of nonlinear networks and its application to microwave parametric frequency dividers," *IEEE Trans. Microw. Theory Tech.*, vol. 30, no. 7, pp. 1050–1058, July 1982.

[25] G. Sarafian and B. Kaplan, "The dynamics of parametric frequency divider and some of its practical implications," in *Proc. Conv. of Elect. Electron. Eng. in Israel*, pp. 523–526, Nov. 1996.

[26] L. Pantoli, A. Suarez, G. Leuzzi, and F. Di Paolo, "Complete and systematic simulation tools for frequency divider design," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 11, pp. 2442–2452, Oct. 2008.

[27] Z. Heshmati, I. C. Hunter, and R. D. Pollard, "Microwave parametric frequency dividers with conversion gain," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 10, pp. 2059–2064, Oct. 2007.

[28] W. Lee and E. Afshari, "Distributed parametric resonator: a passive CMOS frequency divider," *IEEE J. of Solid-State Circuits*, vol. 45, no. 9, pp. 1834–1844, Sept. 2010.

[29] J. P. Oliveira and J. Goes, *Parametric analog signal amplification applied to nanoscale CMOS technologies*. Springer Science & Bus. Media, 2012.

[30] H. M. Hussein, M. A. Ibrahim, G. Michetti, M. Rinaldi, M. Onabajo, and C. Cassella, "Systematic synthesis and design of ultralow threshold 2:1 parametric frequency dividers," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 8, pp. 3497–3509, Aug. 2020.

[31] M. Yan, H. M. Hussein, C. Cassella, M. Rinaldi, and M. Onabajo, "Design of a CMOS parametric frequency divider with 2.4-GHz output frequency for RF Systems-on-a-Chip," in *Proc. IEEE Int. Symp. on Circuits and Syst. (ISCAS)*, May 2022.

[32] A. Suárez and R. Melville, "Simulation-assisted design and analysis of varactor-based frequency multipliers and dividers," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 3, pp. 1166–1179, Mar. 2006.

[33] H. M. Hussein, M. A. Ibrahim, M. Rinaldi, M. Onabajo, and C. Cassella, "Reflective parametric frequency-selective limiters with sub-dB loss and μWatts power thresholds," *IEEE Trans. Microw. Theory Tech.*, June 2021.

[34] W. Lee and E. Afshari, "Low-noise parametric resonant amplifier," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 58, no. 3, pp. 479–492, Mar. 2010.

[35] D. Shim, W. Choi, J.-W. Lee, *et al.*, "Self-dynamic and static biasing for output power and efficiency enhancement of complementary antiparallel diode pair frequency tripler," *IEEE Microw. and Wireless Components Lett.*, vol. 27, no. 12, pp. 1110–1112, Oct. 2017.

[36] Z. Ahmad and K. Kenneth, "0.65–0.73 THz quintupler with an on-chip antenna in 65-nm CMOS," in *Symp. VLSI Circuits*, June 2015.

[37] S. Kabir, S. Magierowski, G. G. Messier, and Z. Zhao, "A direct 100 GHz parametric CMOS tripler," *IEEE Microw. and Wireless Components Lett.*, vol. 23, no. 10, pp. 557–559, Apr. 2013.

[38] Z. Zhao, J.-F. Bousquet, and S. Magierowski, "100 GHz parametric CMOS frequency doubler," *IEEE Microw. and Wireless Components Lett.*, vol. 20, no. 12, pp. 690–692, Nov. 2010.

[39] M. Pontón and A. Suarez, "Optimized design of frequency dividers based on varactor-inductor cells," *IEEE Trans. Microw. Theory Tech.*, vol. 63, no. 12, pp. 4458–4472, Nov. 2015.

[40] B. Razavi and R. Behzad, *RF Microelectronics*, vol. 2. Prentice-Hall New York, 2012.

[41] F. Ramirez, R. Melville, A. Suarez, and J. S. Kenney, "Nonlinear analysis and design of frequency selective limiters based on parametric circuits," in *Proc. IEEE MTT-S Int. Microw.Symp. Dig.*, pp. 947–950, June 2008.

[42] S.-L. Jang, W.-C. Cheng, and C.-W. Hsue, "Wide-locking range divide-by-3 injection-locked frequency divider using sixth-order RLC resonator," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 7, pp. 2598–2602, Jan. 2016.

[43] Y.-H. Chuang, S.-H. Lee, R.-H. Yen, S.-L. Jang, J.-F. Lee, and M.-H. Juang, "A wide locking range and low voltage CMOS direct injection-locked frequency divider," *IEEE Microw. and Wireless Components Lett.*, vol. 16, no. 5, pp. 299–301, May 2006.

[44] N. Rezaei-Hosseinabadi, R. Dehghani, S. A. Khajehoddin, and K. Moez, "A wideband frequency divider with programmable odd/even division factors and quadrature/symmetrical outputs," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 67, no. 6, pp. 1857–1866, Jan. 2020.

[45] S.-L. Jang, W.-C. Lai, Y.-L. Ciou, J. C. Hou, and J.-W. Syu, "Divide-by-2 injection-locked frequency dividers using the electric-field coupling dual-resonance resonator," *IEEE Trans. Microw. Theory Tech.*, vol. 68, no. 3, pp. 844–853, Dec. 2019.

[46] A. Garghetti, A. L. Lacaita, and S. Levantino, "A novel single-inductor injection-locked frequency divider by three with dual-injection secondary locking," *IEEE Trans. on Circuits and Syst. I: Reg. Papers*, vol. 66, no. 5, pp. 1737–1745, Oct. 2018.

[47] J. Lee, S. Park, and S. Cho, "A 470-μW 5-GHz digitally controlled injection-locked multi-modulus frequency divider with an in-phase dual-input injection scheme," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 19, no. 1, pp. 61–70, Oct. 2009.

[48] P. Dekate, W. Redman-White, D. M. Leenaerts, and J. R. Long, "Broadband odd-number CMOS prescalers with quadrature/symmetrical outputs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 7, pp. 399–403, June 2012.

[49] T.-H. Chien, C.-S. Lin, C.-L. Wey, Y.-Z. Juang, and C.-M. Huang, "High-speed and low-power programmable frequency divider," in *Proc. IEEE Int. Symp. on Circuits and Syst. (ISCAS)*, pp. 4301–4304, Aug. 2010.

Mengting Yan (Graduate Student Member, IEEE) received the B.E. degree in electronics information engineering from Beijing University of Aeronautics and Astronautics (BUAA), Beijing, China, in 2016. He is now pursuing the Ph.D. degree in electrical engineering at Northeastern University, Boston, USA.

In 2020, he joined Qorvo Inc., Chelmsford, MA, USA as an RF/Analog SOI Design Intern, where he was involved in the design of low-insertion-loss RF switches and supporting analog control circuitry. Since Jan. 2023, he has been working as a senior analog design engineer in the mixed-signal design engineering team at Analog Devices Inc. in Chandler, AZ. His current research interests include parametric circuits, on-chip hardware Trojan detection, low-power ADCs, design of analog/mixed-signal ICs, and machine learning.

Hussein M. E. Hussein (Graduate Student Member, IEEE) received the B.S. and M.Sc. degrees in electrical engineering from Cairo University, Giza, Egypt, in 2013 and 2017, respectively. He is currently pursuing the Ph.D. degree at the Electrical and Computer Engineering Department, Northeastern University, Boston, MA, USA.

He is currently working on the development of parametric circuits for enhanced wireless sensing and far-field identification. He is also working on employing parametric circuits in RF signal processing and in developing phase noise reduction techniques for RF systems.

Cristian Cassella (Member, IEEE) received the B.S.E. and M.Sc. degrees (Hons.) from the University of Rome Tor Vergata, Rome, Italy, in 2006 and 2009, respectively, and the Ph.D. degree from Carnegie Mellon University, Pittsburgh, PA, USA, in 2015.

In 2011, he was a Visiting Scholar with the University of Pennsylvania, Philadelphia, PA, USA. In 2015, he was a Post-Doctoral Research Associate with Northeastern University. In 2016, he became an Associate Research Scientist. He is currently an Assistant Professor with the Electrical and Computer Engineering Department, Northeastern University, Boston, MA, USA. He is the author of 83 publications in peer-reviewed journals and conference proceedings. Two of his peer-reviewed journal articles published on the *IEEE Journal of Microelectromechanical Systems (JMEMS)* were selected as the Papers of Excellent Quality (JMEMS RightNowPapers), hence being released as open-access. One of his journal articles was chosen as the cover for the Nature Nanotechnology October 2017 Issue. Another one of his journal articles was selected as a featured article by the *Applied Physics Letters* magazine. He holds five patents and two patent applications in the area of acoustic resonators and RF systems. In 2018, he was awarded by the European Community (EU) the Marie-Sklodowska-Curie Individual Fellowship. In 2021, he was a recipient of the NSF Career Award. He received the Best Student Paper Award at the *IEEE International Frequency Control Symposium* in 2013, 2021 (with his student), and 2022 (with his student). He is a Technical Reviewer of several journals, such as *Applied Physics Letters*, *IEEE Transactions On Electron Devices*, *IEEE Transactions on Ultrasonics, Ferroelectric and Frequency Control*, *IEEE Journal of Microelectromechanical Systems*, *IEEE Electron Device Letters*, *Journal of Micromechanics and Microengineering*, *Journal of Applied Physics*, *IEEE Sensors Letters*, *and Review of Scientific Instruments*.

Matteo Rinaldi (Senior Member, IEEE) received the Ph.D. degree in electrical and systems engineering from the University of Pennsylvania, Philadelphia, PA, USA, in December 2010.

He worked as a Post-Doctoral Researcher at the University of Pennsylvania in 2011. He joined the Electrical and Computer Engineering Department, Northeastern University, Boston, MA, USA, as an Assistant Professor, in January 2012. His group has been actively working on experimental research topics and practical applications to ultralow-power MEMS/NEMS sensors (infrared, magnetic, chemical, and biological), plasmonic microelectromechanical and nanoelectromechanical devices, medical microsystems and implantable microdevices for intrabody networks, reconfigurable radio frequency devices and systems, phase change material switches, and 2-D material-enabled micromechanical and nanomechanical devices. The research in his group has been supported by several federal grants (including DARPA, ARPAE, NSF, and DHS), the Bill and Melinda Gates Foundation, and the Keck Foundation with funding of $14+M since 2012. He is the Founder and the CEO of Zepsor Technologies, Boston, MA, a startup company that aims to bring to market zero standby power sensors for various Internet-of-Things applications, including distributed wireless fire monitoring systems, battery-less infrared sensor tags for occupancy sensing and distributed wireless monitoring systems of plant health parameters for digital agriculture. He is also the Owner of Smart MicroTech Consulting LLC, Boston, MA, a company that routinely provides consulting services to government agencies, large companies, and startups in the broad areas of microtechnologies and nanotechnologies, the Internet of Things, wireless communication devices and systems, radio frequency devices and systems, and sensors. He is currently a Professor with the Electrical and Computer Engineering Department, Northeastern University, and the Director of Northeastern SMART, a university research center that, by fostering the partnership between university, industry, and government stakeholders, aims to conceive and pilot disruptive technological innovation in devices and systems capable of addressing fundamental technology gaps in several fields, including the Internet of Things (IoT), 5G, quantum engineering, digital agriculture, robotics, and healthcare. He has coauthored more than 140 publications in the aforementioned research areas. He holds ten patents and more than ten device patent applications in the field of MEMS/NEMS.

Dr. Rinaldi was a recipient of the IEEE Sensors Council Early Career Award in 2015, the NSF CAREER Award in 2014, and the DARPA Young Faculty Award class of 2012. He also received the Best Student Paper Award at the 2009, 2011, 2015 (with his student), and 2017 (with his student) IEEE International Frequency Control Symposiums, the Outstanding Paper Award at the 18th International Conference on Solid-State Sensors, Actuators and Microsystems, Transducers 2015 (with his student), and the Outstanding Paper Award at the 32nd IEEE International Conference on Micro Electro Mechanical Systems, MEMS 2019 (with his student).

Marvin Onabajo (Senior Member, IEEE) is an Associate Professor in the Electrical and Computer Engineering Department at Northeastern University. He received a B.S. degree (*summa cum laude*) in Electrical Engineering from The University of Texas at Arlington in 2003 as well as the M.S. and Ph.D. degrees in Electrical Engineering from Texas A&M University in 2007 and 2011, respectively.

From 2004 to 2005, he was Electrical Test/Product Engineer at Intel Corp. in Hillsboro, Oregon. He

joined the Analog and Mixed-Signal Center at Texas A&M University in 2005, where he was engaged in research projects involving analog built-in testing, data converters, and on-chip temperature sensors for thermal monitoring. In the spring 2011 semester, he worked as a Design Engineering Intern in the Broadband RF/Tuner Development group at Broadcom Corp. in Irvine, California. Marvin Onabajo has been at Northeastern University since the Fall 2011 semester. His research areas are analog/RF integrated circuit design, on-chip built-in testing and calibration, mixed-signal integrated circuits for medical applications, data converters, and on-chip sensors for thermal monitoring. He currently serves as Associate Editor on the editorial boards of the *IEEE Transactions on Circuits and Systems I* (TCAS-I, 2016-2017, 2018-2019, 2020-2021 and 2022-2023 terms) and of the *IEEE Circuits and Systems Magazine* (2016-2017, 2018-2019, 2020-2021 and 2022-2023 terms). During the 2014-2015 term, he was on the editorial board of the *IEEE Transactions on Circuits and Systems II* (TCAS-II). He received a 2015 CAREER Award from the National Science Foundation, a 2017 Young Investigator Program Award from the Army Research Office (ARO), and the 2015 Martin Essigman Outstanding Teaching Award from the College of Engineering at Northeastern University.