

Quasi-Nondestructive Read Out of Ferroelectric Capacitor Polarization by Exploiting a 2TnC Cell to Relax the Endurance Requirement

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Abstract—In this work, we exploit a 2TnC ferroelectric random access memory (FeRAM) cell design to realize the quasi-nondestructive readout (QNRO) of ferroelectric polarization (P_{FE}) in a capacitor, which can relax the endurance requirement of the ferroelectric thin film and exploits the benefits of both FeRAM and ferroelectric FET (FeFET). We demonstrate that: i) QNRO sensing of P_{FE} is conducted successfully in experiment with a ON/OFF ratio (I_{ON}/I_{OFF}) $> 10^3$, $I_{ON} > 10 \mu A$, and read endurance $> 10^6$ cycles, which can relax the FeRAM endurance requirement by 10^6 x; ii) optimization of the cell performance can be realized by tuning the metal-ferroelectric-metal capacitor (MFM) capacitor to read transistor area ratio and read transistor threshold voltage (V_{TH}); iii) the 2TnC cell structure is 3D-compatible, enabling integration of highly dense memory solution; iv) the 2TnC cell structure also enables compute-in-memory (CIM) applications of FeRAM, which has not been widely explored. With this technology, storage and memory-centric computing can be enabled.

Index Terms—Ferroelectric random access memory (FeRAM), quasi-nondestructive readout (QNRO).

I. INTRODUCTION

FERROELECTRIC HfO_2 has revived interests in high performance and low power ferroelectric memory devices, including capacitor based FeRAM and transistor based FeFET [1], [2], [3]. HfO_2 based FeRAM with 1 transistor and 1 MFM

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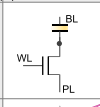
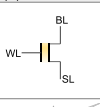
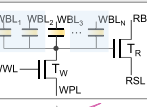
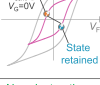
	(a) 1T-1C FeRAM	(b) 1T FeFET	(c) Proposed: 2Tn-C FeRAM
Memory structure			
Sensing mechanism			
Sensing method	Destructive	Non-destructive	Quasi-nondestructive
Endurance req.	$> 10^{15}$	Relaxed ($> 10^8$)	Relaxed ($> 10^{15}$)
Write perf.	Excellent	Poor (V_{write} reliability)	Excellent

Fig. 1. (a) FeRAM's destructive read requires high endurance. (b) FeFET suffers from poor write performance and reliability. (c) Our 2TnC FeRAM realizes QNRO with good write performance.

capacitor structure, as shown in Fig.1(a), is promising for its excellent write performance, such as low operating voltage and high reliability [4], [5], [6], [7]. However, to sense the stored P_{FE} of a MFM capacitor, it is necessary to switch the polarization and then measure the resulting switching current (Fig.1(a)). The destructive sensing process thus demands a write-back operation to restore P_{FE} after every read operation. Therefore, it is crucial that FeRAM should ideally endure more than 10^{15} write cycles [8], which is a nontrivial engineering effort and yet achieved.

In contrast, the ferroelectric polarization can be sensed out non-destructively in a FeFET as the P_{FE} sets the device threshold voltage (V_{TH}), which can be easily read out through the channel current [2], [3]. Applying a small read gate bias, the read disturb to P_{FE} is negligible allowing almost infinite read cycles, thus relaxing the write endurance requirements for FeFET to around 10^8 cycles. However, FeFET suffers from its high write voltage and poor reliability mainly associated with the large charge mismatch between the ferroelectric layer and the semiconductor [9], [10]. To avoid the challenges of both devices while exploiting their advantages, a 2TnC FeRAM cell is exploited in this article, which can support multiple read cycles before the need of writing back, hence called quasi-nondestructive readout (QNRO).

The 2TnC cell, shown in Fig.1(c), consists of a write transistor (T_W), a read transistor (T_R) and multiple MFM capacitors. During the write process, T_W is turned on and the selected MFM's P_{FE} is set to different states by applying V_{WBL} (write bit line) and V_{WPL} (write plate line) pulses, as shown in Fig.2(a). The write process of 2TnC FeRAM is similar to the conventional 1T-1C FeRAM, therefore the

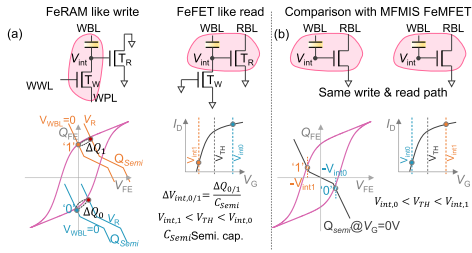


Fig. 2. (a) QNRO of FeRAM relies on the difference of ΔQ_0 and ΔQ_1 in a MFM capacitor. Compared with (b) FeMFET, 2TnC FeRAM has a lower V_{Write} , higher retention time, and higher memory density due to T_W/T_R sharing.

same write performance is expected. The idea of QNRO of FeRAM, as proposed in [11], [12], and [13], is to switch small but enough polarization to turn ON a read transistor channel such that multiple read cycles can be supported before a write-back is needed. The read is conducted by turning OFF the T_W , applying a V_R to the WBL, and then sensing T_R current. If the P_{FE} is positive (i.e., point to channel, bit '1'), a positive V_R will cause almost zero P_{FE} switching (i.e. ΔQ_1 or the effective capacitance of the state '1' is small) [11]. As a result, the internal voltage (V_{int}) sees a small change, thereby leading to a small T_R current [12], [13]. On the other hand, if P_{FE} is negative (i.e., point to gate), more P_{FE} switching is induced (i.e. ΔQ_0 is large enough), albeit still significantly lower than conventional FeRAM sensing. As a result, V_{int} will be high, leading to a large T_R current. By utilizing this approach, P_{FE} can be read multiple cycles before accumulative P_{FE} switching leads to the destruction of the state '0'.

It is worth noting that there is a significant difference between the 2TnC FeRAM structure and the ferroelectric-metal FET (FeMFET) [14]. FeMFET utilizes the same path for both writing and reading process and stores information on the V_{int} , modulated by P_{FE} , as shown in Fig.2(b). However, this approach may be prone to retention loss induced by leakage [15], [16], [17]. In comparison, the 2TnC FeRAM leverages two separate write and read paths, exploiting FeRAM's excellent write performance and approximating FeFET's non-destructive read operation. In addition, it is important to distinguish the 2TnC design from many similar reported 2T1C designs [18], [19], [20]. In previous designs, the sensing of P_{FE} , though done through the T_R , is still conducted through full polarization switching, similar to conventional FeRAM, thus not addressing the excessive endurance requirement. Combining the previously reported QNRO of P_{FE} and the 2TnC structure is a unique contribution of this work. The 2TnC structure also provides the advantage of sharing the (T_W) and (T_R) among multiple MFM capacitors, thereby enhancing the integration density.

II. EXPERIMENTAL DEMONSTRATION OF QNRO

The QNRO operation is verified using a 2T1C cell built discretely with a 10nm thick $Hf_{0.5}Zr_{0.5}O_2$ MFM capacitor and two discrete transistors (i.e., ALD1103). The fabrication process of $Hf_{0.5}Zr_{0.5}O_2$ MFM capacitor is shown in [21]. The hysteresis loop of $Q_{FE}-V_{FE}$ (Fig.3(a)) and the dynamic capacitance obtained by taking the derivative of Q_{FE} with respect to V_{FE} (Fig.3(b)) reveal the difference in capacitance between state '0' and '1', which is the origin of QNRO operation. Fig.3(c) shows the T_R I_D-V_G curves. The MFM capacitance is about $3\times$ larger than the T_R gate capacitance.

Fig.3(d) illustrates a transient waveform that corresponds to

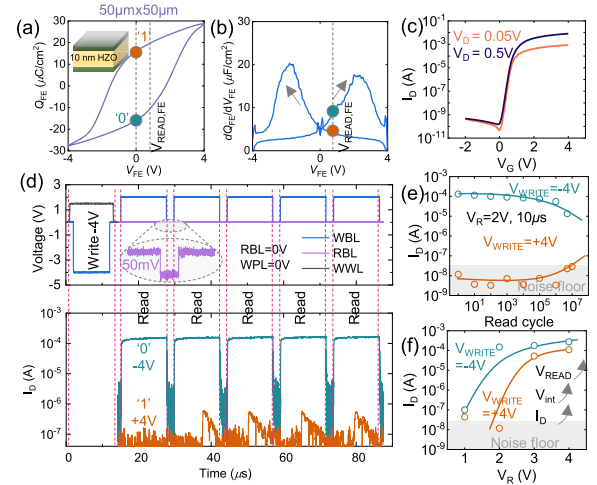


Fig. 3. (a) $Q_{FE}-V_{FE}$ and (b) dQ_{FE}/dV_{FE} hysteresis loop. (c) I_D-V_G of T_R (d) Waveform shows correct sensing of '0' and '1'. (e) Read cycle can reach 10^7 . (f) I_{ON} , I_{OFF} rises with increasing V_R . The curves in (e) and (f) are for visual guidance and not fitting curves.

the writing of the MFM capacitor, which is then followed by five cycles of QNRO sensing. The operational principle remains the same as depicted in Fig.2(a), where the WWL provides a voltage of 1.5V to activate T_W , and a voltage of $+4/-4V$ is applied to WBL to write a bit '1' or '0'.

Shortly after programming, the T_W is switched OFF, and V_R is applied to WBL. Fig.3(c) shows that the state '0' (i.e., written with -4V) has a higher current than state '1' (i.e., written with +4V), opposite to FeMFET. Fig.3(d) shows the evolution of sensed current over multiple read cycles, indicating that the read endurance of the device is greater than 10^6 cycles with no significant degradation in sensing margin. This indicates that the endurance requirement for HfO_2 FeRAM can be relaxed by $>10^6$ times, making HfO_2 FeRAM more practical for various applications. Additionally, an optimal V_R exists, as shown in Fig.3(e) and (f), to achieve the maximum I_{ON}/I_{OFF} as a too low V_R shuts OFF the T_R ; while a too high V_R turns ON T_R , irrespectively of the P_{FE} .

III. DESIGN SPACE EXPLORATION OF 2TnC CELL

To investigate the design space for the 2TnC cell, a hybrid SPICE model is built. T_W and T_R are simulated using 45nm PTM model [22] and capacitor is modeled with a calibrated Monte Carlo model [23] capturing the domain distribution and switching stochasticity. Two parameters (i.e., area ratio of MFM capacitor to the T_R (A_{MFM}/A_{TR}) and V_{TH} of T_R ($V_{TH,TR}$)) are studied with the goal of high I_{ON} , large ON/OFF ratio, and small polarization change when sensing state '0' (i.e., ΔQ_0). Without loss of generality, the area of the T_R (A_{TR}) is kept at $2\mu m^2$, while the A_{MFM} is adjusted to tune the voltage division between the MFM and T_R during read operation.

Fig.4 shows the design space of the 2T1C cell in terms of I_{ON}/I_{OFF} ratio (Fig.4(a)), I_{ON} (Fig.4(b)), and ΔQ_0 (Fig.4(c)) for fixed write ($\pm 2V$, $5\mu s$) and read pulse ($1.2V$, $5\mu s$). Since only one capacitor is read at a time while the others are floating, 2T1C, being equivalent to 2TnC, is studied here for the readout while 2TnC operation is studied in Fig.5. Note that the slow speed is because the MFM model is calibrated with switching dynamics of a large MFM capacitor with significant parasitics [23] and by no means the intrinsic operation limit as sub-ns switching has been demonstrated [24], [25]. As the A_{MFM} increases, its capacitance also increases, resulting in a

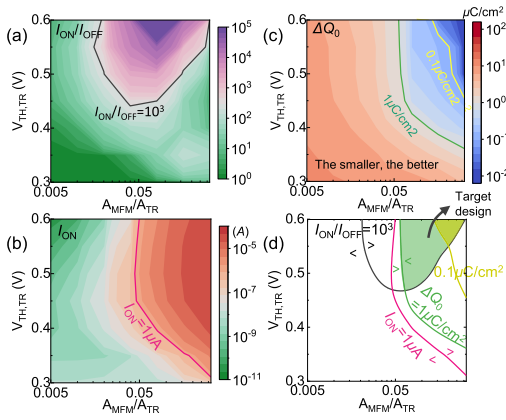


Fig. 4. Design space of 2TnC cell for QNRO against two design parameters, A_{MFM}/A_{TR} and $V_{TH,TR}$. (a) I_{ON}/I_{OFF} , (b) ΔQ_0 and (c) I_{ON} are presented. (d) Target design parameters are obtained.

higher V_{int} and lower V_{FE} [14], [26], [27]. This phenomenon accounts for the observed increase in I_{ON} , shown in Fig.4(b), and decrease in ΔQ_0 , shown in Fig.4(c), with an increase in the A_{MFM}/A_{TR} ratio. The I_{ON}/I_{OFF} ratio, which is extracted at a $V_{TH,TR}$ of 0.5V, displays a peak at a given A_{MFM} . This is because a small A_{MFM}/A_{TR} results in a low V_{int} even for ON state while a large A_{MFM}/A_{TR} causes a high V_{int} even for the OFF state. Both cases reduces the I_{ON}/I_{OFF} ratio. The $V_{TH,TR}$ is another parameter that affects voltage division between MFM and the T_R , thus modulating V_{int} by ensuring charge conservation between the two. When considering different values of $V_{TH,TR}$, it was observed that while both the I_{ON} and ΔQ_0 tend to saturate after 0.5 V due to the simultaneous increase of V_{int} and $V_{TH,TR}$, the I_{ON}/I_{OFF} ratio continues to increase within a reasonable range of $V_{TH,TR}$.

The target design parameters, which are illustrated in Fig.4(d), were obtained to achieve an $I_{ON}/I_{OFF} > 10^3$, $\Delta Q_0 < 1 \mu C/cm^2$ for QNRO, and $I_{ON} > 1 \mu A$ simultaneously. Note that modeling results aim at unraveling the mechanisms of the device and do not necessarily match the experimental results as the devices differ significantly. The model verification will be conducted with fully integrated 2TnC cells in future work. In case engineering $V_{TH,TR}$ is not practical, the read operation can be augmented with a pre-charge phase, where V_{int} can be set to an initial value, equivalent to $V_{TH,TR}$ engineering. The simulation results are omitted here due to space limit. Fig.5(a) shows the transient waveform of writing and reading a 2T8C cell. It shows successful memory operation and the small P_{FE} change during read, thus demonstrating its QNRO characteristics. The simulation results of 16, 32 and 64 MFM capacitors per 2TnC cell, shown in Fig.5(b), also indicate that a large I_{ON}/I_{OFF} can be obtained with QNRO with a high integration density. The simulated device variation is based on different sampling of the domain distribution function and only accounts for intrinsic variation sources [23].

In an 2TnC array, T_W and T_R are shared across multiple cells. When writing, half-selected MFM capacitors in the same row or column of the target cell get $V_w/2$, while unselected capacitors remain undisturbed. Disturb-free reading is achieved by selecting the target WBL and floating other WBLs, allowing column-wise operation.

It should be noted that the 2TnC cell is compatible with dense 3D integration, as shown in Fig.6(a). Each string corresponds to a 2TnC cell. By hiding the T_R and T_W footprint in the vertical 3D structure, the memory density

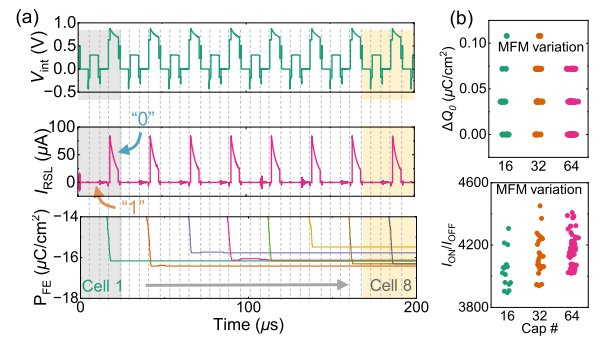


Fig. 5. (a) The waveform verifies 2T8C FeRAM's functionality. (b) ΔQ_0 and I_{ON}/I_{OFF} for 16, 32, and 64 MFM capacitors.

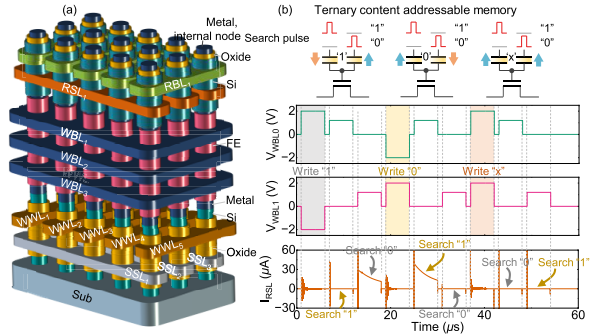


Fig. 6. (a) The 2TnC structure can be integrated in 3D. (b) One potential CIM application of 2TnC cell is TCAM. By encoding write and read pulses, TCAM operation is validated.

can be enhanced. This compatibility allows for the potential of enabling dense memory. Detailed array operation, disturb management, geometry scaling, and impact of parasitics are dedicated to our future work. In addition, the proposed QNRO scheme allows FeRAM to be utilized in compute-in-memory (CIM) applications, which has long been limited by the destructive read operation in conventional FeRAM technology. The CIM implementation has the same design requirements as the memory as long as only a single MFM capacitor in the 2TnC cell is active at a time. For instance, by using two MFM capacitors, a ternary content addressable memory (TCAM) can be constructed, as shown in Fig.6(b), similar to prior work in [28]. For the state 0 and 1 storage, the information is stored as complementary P_{FE} states in the two capacitors, while for the state X storage, both capacitors are programmed to positive P_{FE} . Then, the search information is encoded as which capacitor receives the read pulse. In this way, the successful TCAM operation was verified, which allows to detect whether the stored information matches the search query. Compared to other FeFET-based TCAM implementations, e.g., 2FeFET [29], 2FeFET-1T & 2FeFET-2T [30], our design reduces write voltage and improves reliability.

IV. CONCLUSION

We have exploited and validated a 2TnC FeRAM cell to sense a capacitor polarization in a quasi-nondestructive manner, which can allow multiple read cycles before a write-back operation is needed. This working principle can potentially push the HfO₂ based FeRAM into a technology by relaxing the endurance requirement to a practical level. A comprehensive design space exploration is conducted for the better design of the cell. A potential 3D structure and a compute-in-memory example are proposed. This QNRO memory therefore paves the way for wider application of FeRAM technology.

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