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Nonconformal Electrochemical Memristor through Vapor Phase Polymerization of Pyrrole

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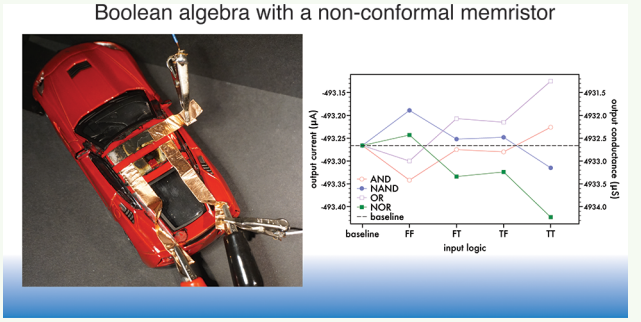
ABSTRACT: A nonvolatile organic synaptic memristor was fabricated utilizing a vapor phase polymerization technique for synthesizing polypyrrole. This synaptic memristor employed a bottom synaptic electrode in order to "read" the device's conductance, termed the synaptic weight of this neuromorphic-capable device. Through a programming pulse of +1 V amplitude and a 1 s duration to the "writing" electrode, or top synaptic electrode, a resolution of 0.245 μS occurs per change for each programmed state. This organic synaptic memristor consumes a minimum programming power of 4.16 fJ mm^{-2} and can be further decreased via advanced patterning and layer deposition techniques. Operational applications are demonstrated for this organic synaptic memristor, including Boolean algebra (AND, NAND, OR, and NOR logic gates), as well as abacus calculations (addition, subtraction, and division).



KEYWORDS: *conjugated polymer, organic synapse, memristor, arithmetic, Boolean algebra*

1. INTRODUCTION

Memristors were initially theorized in 1971 as a fundamental passive 2-terminal electronic device that functions as a nonvolatile tunable resistor.[1] Memristive devices are characterized by the capability to act as a resistive switching device at low operating powers.[1,2] A 2-terminal memristor is defined as a nonlinear component that relates electric charge to magnetic flux.[1] This definition has since been expanded to 3-terminal devices that demonstrate the same correlation as a memristive nonvolatile device. Besides the 2-terminal devices, various types of 3-terminal memristive devices have been suggested and developed recently.[3−8] The 3-terminal memristive structures incorporate a third terminal, where switching characteristics are separately controlled. Recent efforts have reported on memristive devices that are based on field-effect transistors (FET)[9−11] and organic electrochemical transistors (OECT)[12−14] architectures. These transistors consist of a 3-terminal device geometry with gate, drain, and source electrodes and one or two active layers separated by a dielectric (FET) or electrolyte (OECT). The working principle of an OECT is that with voltage applied to the gate, the drain and source (channel) active layer is electrochemically (de)doped to modulate the resistance (or conductance) state.[15−17] By slightly modifying the OECT design approach with two active conjugated polymer layers separated by an electrolyte, many neuromorphic-capable OECTs have been reported.[3,18,19] The top gate conjugated polymer layer acts as a reservoir of electrons used to supply the bottom channel film. The state of charge of the conjugated polymer coating the channel electrodes determines the electrical conductivity of this memristive system. The electrolyte, with an applied bias on the device, acts as an injection-extraction pathway for ions between the top gate and bottom channel electrodes in order to modulate the doping (redox) state. With no bias applied, the electrolyte disconnects the two layers where the electronic charge remains unaltered, and the electrolyte acts as an energy barrier to prevent further recombination effects. Analogous to biological nervous systems where neurons and synapses are the building blocks for computation and memory, memristive devices can perform similar complex operations with low power consumption.[20]

Biologically inspired synaptic architectures function based on synaptic weights that are modulated by either the number or frequency of incoming stimuli.[21] Similar to biological synapses, memristors have been shown to share a common role in which they exhibit reliable and repeatable analog tuning properties which include nonabrupt switchable transitions,

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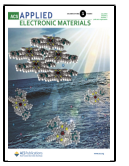

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continuously programmable resistance states, and predictable and well-established responses.[21−24] Biological neurons and synapses function as an integrated system to perform learning and memory through a highly energy-efficient mechanism of modulating their synaptic weights in response to any and all biological inputs. This drives forward the need to create new low-energy neuromorphic-capable devices where operation is <10 fJ per stimulus.[21] Many organic memristive systems have been reported where key parameters, such as device reproducibility, state stability, scalability, power consumption, and speed, often are lacking compared to many inorganic-based systems.[24] For this reason, redox-based systems are being studied, as they satisfy many of these base requirements for neuromorphic computation.[25]

The ability to deposit semiconducting films is crucial where the reliability of thin, even coatings is necessary. Most commonly used film deposition procedures involve solution-processable spin coating, dip coating, or various printing techniques; however, conjugated polymers (CPs) are typically difficult to suspend in solution, making uniform films difficult to form.[26] To this end, polymer derivatives have been established with either varying side chain groupings[27−30] or doping of various polyelectrolyte materials[31−34] playing the role of a solubilizer while impacting the performance of the material's electronic properties or adding more complexity to processing parameters. To resolve these issues, synthesis through a chemical oxidative *in situ* polymerization technique has been established for various CPs[26,35−38] referred to as vapor phase polymerization (VPP). This technique is often achieved via coating the substrate with an oxidant by solvent-processed spin coating and subsequently exposing the oxidant-coated substrate to monomer vapor. The freedom of design leads to the ability to overcoat more complicated surface geometries and architectures, where other techniques do not succeed. Ferric *p*-toluenesulfonate (FeToS) is a well-suited oxidant used in previous efforts for VPP CPs[39] where, after deposition and cleaning, trace amounts of sulfonate are present and essential for the conducting nature for these CPs.[26] By controlling the crystallite formation of FeToS post-spin-coating, a versatile route for fabricating both smooth and highly conductive films is achievable.[26]

Through the process of VPP, the vaporized monomer is delivered onto the desired substrate to chemically form a smooth and uniform polymer film, functionalizing the materials' surface.[26,40] The ease of this fabrication process, along with the capability to scale up, leads to the ability to form complex devices over arbitrary substrates with conformal and nonconformal substrates without running into common surface wetting or surface tension issues from solution-based processing.[40−42] VPP films are capable of widespread application across many facets where highly mechanically rigid films with uniform smooth coatings are required. A recent report details the use of an electronic-capable conformal substrate based on a nanocellulose composite.[43] The nanocellulose composite provides a robust, transferable template that can adhere to most biological surfaces for use as a flexible display, environmental tags, microaeronautics, or biological sensors. These are significant steps leading toward the integration of electronics into everyday items to transform common appliances and utilities into smarter technologies.

In recent literature, a 3-terminal electrochemical neuromorphic organic device reports synaptic-like behavior via a counter-redox reaction across its architecture.[3] By varying the (de)doping levels of each layer, various redox-active species can be implemented into these 3-terminal synaptic-like memristive devices, which will exhibit neuromorphic computation attributes. Another recent report presents a 3-terminal conjugated polymeric-based electrochemical memristor (cPECM) where, utilizing a PEDOT derivative that is self-doped and water-soluble, both Boolean algebra and elementary algebra were implemented to demonstrate the device's potential as a candidate for neuromorphic computers.[4] To that end, a 3-terminal conjugated polymeric organic synaptic memristive device is presented in this effort that utilizes a VPP deposition of polypyrrole (PPy) over conformal and non-conformal substrates. The PPy-based synaptic memristor is capable of achieving highly distinct and symmetric linear conductance states that can be tailored into neuromorphic and advanced operational techniques.

2. EXPERIMENTAL SECTION

2.1. Materials. All chemical materials were purchased from Fisher Scientific, VWR, Alfa Aesar, and Sigma-Aldrich and used without further purification or processing. Deionized water (DI-H_2O) exhibited a resistivity value of 10^{18} Ohm^{-1} cm^{-1} from a Nanopure System.

2.2. Vapor Phase Polymerization of Polypyrrole. Prior to any coatings, all substrates were cleaned in a sonication bath of DI-H_2O followed by acetone and then isopropyl alcohol for 10 min each, dried under N_2 gas, and then plasma cleaned for 10 min in a Harrick PDC-32G plasma cleaner on high. VPP techniques for various conjugated polymers have been previously reported.[26,36,41,42,44] Herein, a simple procedure for the polymerization of pyrrole (Py) via VPP is reported. FeToS was mixed in methanol (MeOH) at a concentration of 250 mg/mL and shaken until it was fully in solution. The FeToS/MeOH mixture was spun cast onto the conformal substrates at a speed of 3000 rpm for 40 s. Following spin coating, the substrates are soft-baked at 90 °C for 3 min. The films appear as a yellow color and transition to orange after the soft-bake. The oxidant-coated substrates are mounted over a small vial containing 200 μL of Py and loaded inside a model 5851 National Appliance Co. vacuum oven. The oxidant-coated slides are exposed for 2 h under ca. 25 in. of Hg pressure at a temperature ca. 90 °C. After the vaporization of Py liquid to a gas phase, the orange oxidant film transitions to a green-purple film, indicative of the formation of an oxidative species. To remove the oxidant, the slides are fully submerged in a MeOH bath for 3 min before drying with N_2 gas. This process is repeated twice to ensure proper removal of the FeToS oxidant.

2.3. Film Characterization. All films were characterized via UV−vis spectroscopy and thin-film profilometry. Removal of the FeToS oxidant from the PPy film was verified by using UV−vis spectroscopy. A PerkinElmer Lambda 950 was used for all UV−vis spectroscopy experiments, with a glass substrate used as the reference and sample substrate. Chemical reduction of a PPy film was done via a secondary vapor doping of polyethylenimine (PEI, M_W = 800) on a hot plate at 250 °C for 10 min and sealed with a large glass Petri dish cover at atmospheric pressure. To characterize the film thickness, a KLA Tencor step height profilometer was used with the same glass substrates. The spun-cast FeToS oxidant film, the VPP PPy film, and the rinsed PPy film were measured to be ca. 0.9 μm, 1.0 μm, and 100 nm thick, respectively. Film thickness reported is an average thickness of 10 scans over a 12.7 mm × 25.4 mm × 0.7 mm coated-glass slide.

2.4. Device Fabrication. Similar device fabrication has been previously reported.[4] In short, indium tin oxide (ITO)-coated glass (Part Number: CG-50IN-S107) was purchased from Delta Technologies, Limited, with a sheet resistance of 8−12 Ω/sq. In order to remove any unwanted ITO, both the top and bottom synaptic electrodes were acid-etched by using hydrochloric acid (36%) poured over zinc metal. The top synaptic electrode was patterned using polyimide tape (12 mm wide). The bottom synaptic electrode was templated using a positive photoresist such that a channel length of

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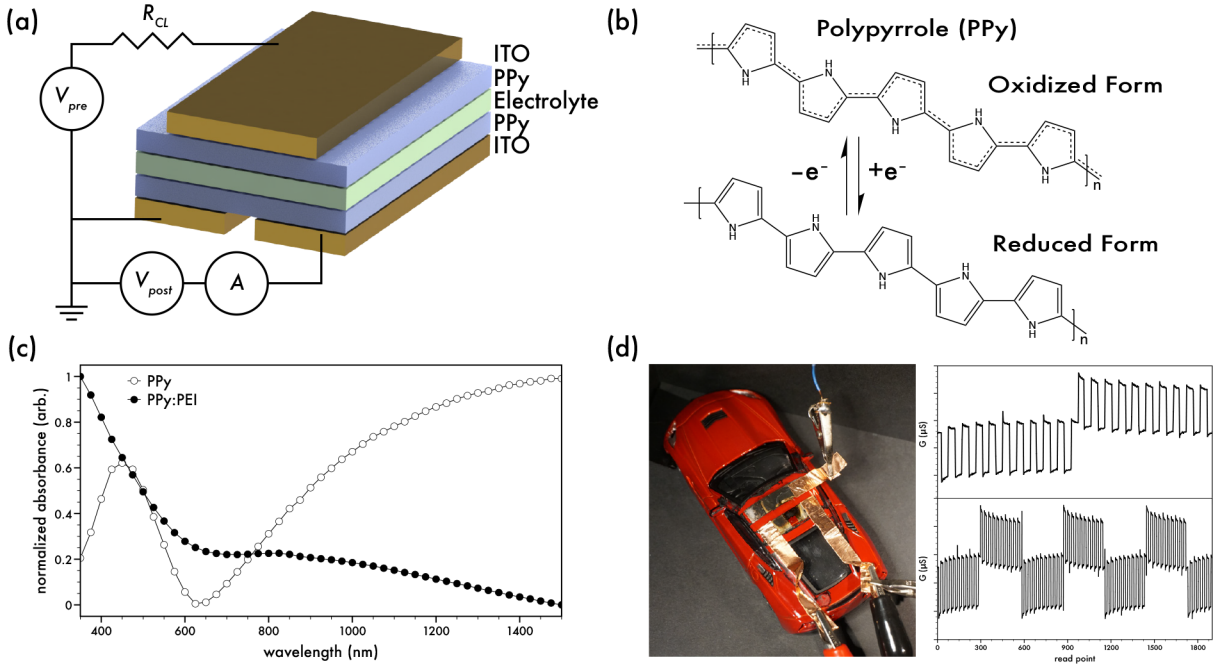

Figure 1. (a) 3D schematic for the PPy-based three-terminal synaptic device and the equivalent circuit. (b) Chemical structure of polypyrrole in its oxidized and reduced form. (c) Optical photophysical properties of an oxidized (○) and reduced (●) PPy thin film. (d) Optical image of a toy car turned into a device with 3 aluminum electrodes and vapor polymerized PPy and overcoated with a polymeric gel electrolyte. Copper tape is used to connect alligator clips for testing to the 3 terminals. Data presented on the top demonstrate the conductance of the toy-based device for a single cycle of 10 + V_{pre} pulses followed by 10 − V_{pre} pulses programmed to the top synaptic electrode. Conductance is measured across the bottom synaptic electrode with a −0.1 V potential. Data presented on the bottom demonstrate the symmetry of the device over repeated cycle testing.

100 μm separation bifurcates a single substrate into two separate ITO electrodes. After the top and bottom synaptic electrodes were properly overcoated with PPy, the substrates were mated with a 125 μm Parafilm spacer. The Parafilm had a well cut out with dimensions of 12 × 20 mm, defining the device's active area as 240 mm^2. The well is filled in with a PEG-based gel containing a tetrabutylammonium hexafluorophosphate (Bu_4NPF_6) electrolyte.[4] The electrolyte is photopolymerized with an ELC-500 light exposure system to properly seal and mate the top and bottom slides. The aluminum (Al) electrodes used on the nonconformal toy car device were deposited via a Denton DV-502a thermal evaporator after templating and masking the car with polyimide tape. All other fabrication steps were the same for the toy car device as for the ITO-based devices unless otherwise stated.

2.5. Device Characterization. Electrical characterization of the devices was done using a Keithley 236 source measurement unit (SMU) to apply any required voltage-pulse scheme to the top synaptic electrode (V_{pre}), and a Keithley 2440 5a sourcemeter was used to supply a constant voltage to the bottom bifurcated synaptic electrode (V_{post}) while constantly monitoring the current. The Keithley 236 SMU was programmed using HTBasic by TransEra, and the Keithley 2440 was programmed in LabVIEW. All testing is done in an ambient environment at room temperature (ca. 21 °C).

3. RESULTS AND DISCUSSION

3.1. Film Characterization. Figure 1a represents the current embodiment of the PPy-based synaptic memristive device and the electronic circuit to implement it. This 3-terminal device contains two active layers, both deposited via a VPP technique for Py. The top presynaptic electrode is separated from the bottom bifurcated postsynaptic electrode via a polymeric gel electrolyte. The electrolyte used is tetrabutylammonium hexafluorophosphate (Bu_4NPF_6) encapsulated in a PEG-based gel network. The electrolyte layer acts as an energy barrier to decouple electron/hole migration and recombination from the top presynaptic input and the bottom postsynaptic terminal. With regard to biological synapses, each conducting layer can be considered a synapse (pre- and postsynaptic terminals) where the gel electrolyte is the synaptic cleft.[3] By modulating the potential redox states of the postsynaptic terminal, a linear, nonvolatile memristive device can be achieved. PPy films are synthesized using a VPP technique where the substrate is first coated with an oxidant material, specifically FeToS spun cast in a methanol (MeOH) solution and soft-baked to remove some residual solvent. The coated films are almost immediately loaded into a vacuum oven such that the films face down with a supply of Py monomer below them. Once the proper vacuum and temperature are reached, Py vaporizes and deposits over the FeToS film, where the polymerization reaction occurs to form PPy as a green-purple film. The residual oxidant is rinsed off with pure methanol postpolymerization prior to any testing or use. Figure 1b presents the fully oxidized and fully reduced chemical structure of PPy, where Figure 1c displays the optical properties of these respective thin films. For the oxidized PPy film, there is a maximum absorption at 453 nm, which is characteristic of the PPy polymer.[45] The broadband absorption tail past ca. 600 nm is an attribute of a highly oxidized species.[46] By exposing a PPy film to PEI vapor, a commonly used reductant,[47] the film is chemically dedoped, and the broadband absorption past ca. 600 nm is drastically diminished. The shallow absorption past ca. 600 nm is a characteristic of a reduced conjugated material.[46]

With regard to polymerization over nonconformal shapes and substrates, Figure 1d demonstrates the use of this polymerization technique on a toy car turned into a memristive synaptic-capable device. While the density of chips on print circuit boards (PCBs) has drastically increased over the past

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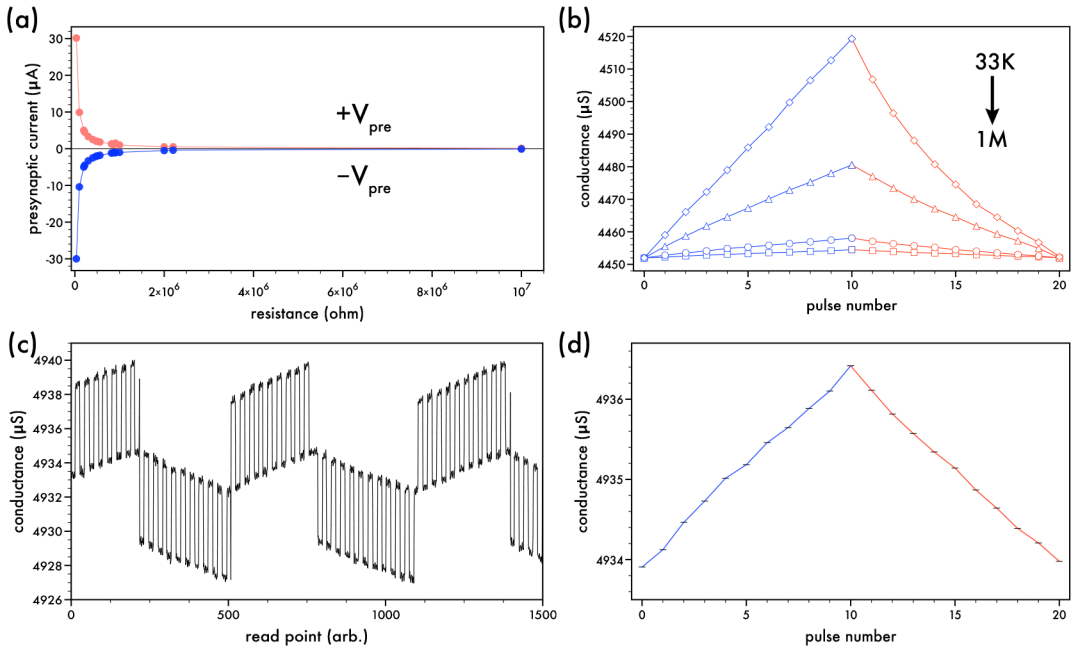

Figure 2. (a) Presynaptic current with regard to varying the input current limiting resistor (R_{CL}). Red implies positive voltage, $+V_{pre}$, and blue implies negative voltage, $-V_{pre}$. R_{CL} values vary from 33 kΩ up to 10 MΩ. (b) Postsynaptic conductance response with regard to varying the input resistance, R_{CL}. R_{CL} values tested are 33 kΩ (◇), 100 kΩ (△), 470 kΩ (○), and 1 MΩ (□). (c) Device output characteristics after applying cycles of 10 pulses/bias. (d) Postsynaptic conductance response with an R_{CL} of 1 MΩ. Tick lines represent standard deviation of distinct programmed states from 10 repeated cycle operations.

few decades with the use of surface-mounted devices (SMDs) and well-established fabrication methods,[48] PCBs suffer from their rigid substrate and planar design. The demand for the design of nonuniform and nonconformal devices affords a path forward to implement smart technology into commonplace objects in the world around us. The toy car was templated with polyimide tape, and aluminum (Al) electrodes were deposited via a high-vacuum thermal evaporator. Following Al electrode deposition, PPy was vapor phase polymerized after dipping the car's roof in a FeToS/MeOH solution and dried under vacuum for 5 min prior to VPP. Following all film depositions, the polyimide tape is removed and the PEG-based gel electrolyte is placed on top such that the gel physically connects the top pre- and bottom postsynaptic electrodes. As a demonstration tool, the toy car was capable of simple potentiation and depression mechanics by applying a constant potential to the postsynaptic terminals (−0.1 V) while programming voltage pulses the top presynaptic terminal (±1 V, 1 s on and 1 s off). This effect is analogous to short-term memory in biological systems.[49]

3.2. Device Performance. For device operation, a voltage pulse (V_{pre}) drives electrons/holes across the top presynaptic electrode, through the gel electrolyte, and into the bottom postsynaptic electrodes. A small voltage (V_{post}) simultaneously biases the bifurcated bottom postsynaptic electrode and continuously reads the current state of the device (i_{post}) every ca. 60 ms. For this circuit, a resistor is used in series prior to the top presynaptic electrode in order to ensure proper current loading to the device. Monitoring the current load distributed across the device (i_{pre}) (cf. Figure 2a), a drastic decrease of current can be observed by increasing the resistor's value. While this strictly follows Ohm's law, there is an asymmetric deviation to the amount of current loaded to the device at lower resistor values (R_{CL} < 50 kΩ). Over a certain threshold (R_{CL} > 100k), the current value is symmetric over repeated pulsing and equally weighted for varying bias polarity, whereas lower resistor values provide variability of current, leading to an asymmetric output. The current load at lower resistor values ensues with improper decoupling of the pre- and postsynaptic terminals, where electrochromic behavior begins to be observed and memristive attributes are diminished. For the case of R_{CL} = 33 kΩ, during the application of 10 + V_{pre} pulses (V_{pre} = +1 V, t_{pulse} = 1 s, t_{off} = 1 s), i_{pre} is observed where the first pulse drives the device at a load of 31.7 μA. At the tenth pulse, the current drops down and drives the presynaptic electrode with 28.6 μA. In the reverse bias, the first $-V_{pre}$ pulse (V_{pre} = −1 V) drives the current at a value of −31.6 μA, and the tenth pulse drops down to −28.6 μA. For the case of R_{CL} = 500 kΩ, V_{pre}'s application drives i_{pre} at a consistent ±2 μA based on the polarity of the bias.

By applying 10 − V_{pre} square wave pulses followed by 10 + V_{pre} square waves, the current response of the device is recorded and presented as i_{post}. Figure 2b represents this voltage paradigm while varying resistor values at the input from 33 kΩ to 1 MΩ. It is important to note that a $+V_{pre}$ will increase current but decrease conductance, whereas a $-V_{pre}$ will decrease current but increase conductance. This is visually represented where blue implies $-V_{pre}$ pulsing and red implies $+V_{pre}$. With an input resistor of 33 kΩ, the response in the $-V_{pre}$ domain linearly increases conductance. When the bias is reversed to + V_{pre} pulsing, an asymmetric decrease in the conductance is observed. As seen in Figure 2d with a resistor value of 1 MΩ, the input current is limited and drives the device at a constant and consistent ±1 μA. Each voltage pulse (V_{pre}) steps up or down the conductance state in increments of ca. 0.245 μS. After 10 − V_{pre} pulses, the device conductance steps up from 4933.91 μS to 4936.42 μS, for a ΔG of 2.51 μS or a percent change of 0.051%. The device demonstrates its symmetric nature after the application of 10 + V_{pre} pulses, which returns to a conductance of 4933.97 μS for a ΔG of ca. 0.06 μS or a percent change of 0.0014% from its initial state.

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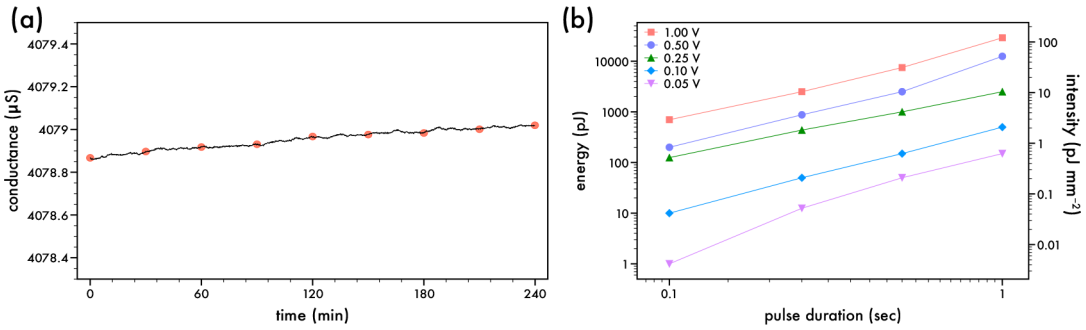

Figure 3. (a) Retention properties of the device after a single cycle of 10 pulses/bias monitored for 4 h with a constant bias to V_{post}. (b) Power consumption characteristics of the device.

Figure 2c is a demonstration of the normal output conductance presented over multiple cycle operations and displays the reliability and reproducibility of the observed programmed states. With regard to mathematical functions, the procedure of applying $+V_{pre}$ and $-V_{pre}$ pulses is synonymous with addition and subtraction, respectively. Further elementary algebra operations (multiplication and division) can also be achieved and have been recently reported for a similar device.[4]

The device's retention and state stability are demonstrated in Figure 3a. These pulse data portray the characteristic signal response exhibited prior to extrapolating each current or conductance state. Retention is measured after a cycle of 10 + V_{pre} followed by 10 − V_{pre} pulses with a continuous V_{post} application of −0.1 V. Within the first 10 s after pulsing, there is a 0.0025% drift, and 4 h after pulsing, there is a 0.0037% drift. To prove the efficiency of the device, energy (pJ) can be calculated as $P = i \times V \times t$. The device's active area is 240 mm^2 and can be used to convert energy to intensity (pJ mm^{-2}) where $E = P$/Active Area. Applying a V_{pre} amplitude of ±1 V and a width of 1 s for the input, the energy consumption for the device is $E = (0.029\ \mu A \times 1\ V \times 1\ s)/240\ mm^2 = 120.83$ pJ mm^{-2} (29 000 pJ of energy) (cf. Figure 3b). When analyzing a more optimized input regime (amplitude of 50 mV and 100 ms duration), the energy consumption is reduced to 1 pJ (intensity of 4.16 fJ mm^{-2}), at an almost 100% decrease in energy consumed per programming pulse.

To understand the tunability of the organic synaptic memristor, the bottom postsynaptic electrode can demonstrate near-linear response when varying the pulse duration and/or the pulse amplitude. This is due to the artifact, where the oxidation state of the PPy-conjugated polymer is a function of the total charge programmed in or out of this layer. Remembering that $+V_{pre}$ will increase current but decrease conductance, and *vice versa*, Figure 4a,b present the change in conductance (ΔG) of the bottom synaptic electrode with varying the input V_{pre} pulses' amplitude or duration, respectively. A near-linear trend in the increase of ΔG for $-V_{pre}$ pulses is evident, with the same trend for the decrease of ΔG occurring for $+V_{pre}$ pulses. This predictable change in conductance is addressed by the departure of cations from the presynaptic top electrode flowing into the bottom postsynaptic electrode for the case of $+V_{pre}$ pulses. The near-linear tunability of this device affords a simple design in devising Boolean and elementary algebra operations by modulating the input voltage parameters, and these will be presented subsequently.

3.3. Neuromorphic Trends. The mechanism for this 3-terminal device to read, write, and forget is similar to a biological nervous system.[4] With the top and bottom synaptic

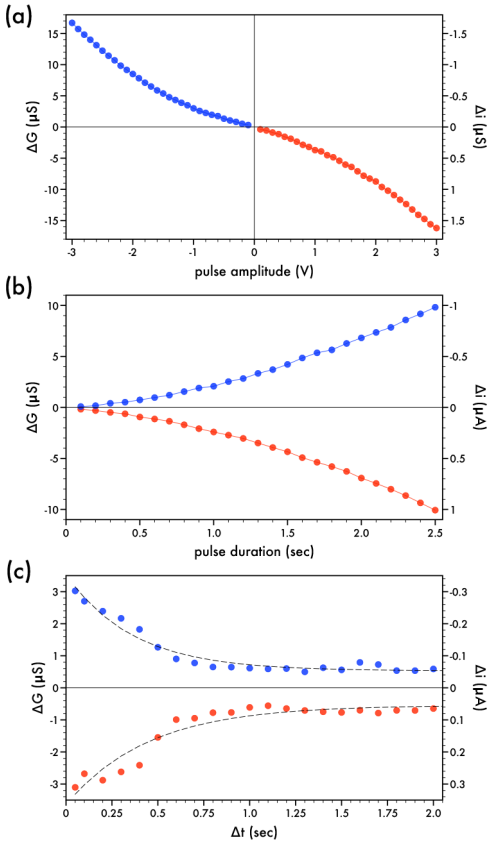

Figure 4. (a) Device response to voltage pulsing at a constant amplitude, $V_{pre} = \pm 1$ V, while varying the pulse duration. (b) Device response to voltage pulsing at a constant duration, $t_{pre} = 1$ s, while varying the pulse amplitude. (c) Paired-pulse facilitation (PPF) (red) and depression (PPD) (blue). Dashed lines represent fitted curves based on data.

electrodes imitating that of a pre- and postsynapse, the device's response (i_{post}) is modulated based on the current flow through the conjugated polymer covering the bottom synaptic electrode, analogous to modulating synaptic weight. Paired-pulse facilitation (PPF) and paired-pulse depression (PPD) are both short-term memory mechanics that measure the response characteristic based on two stimuli inputs (V_{pre}) and the time scale that separates them (Δt). Remembering that a $-V_{pre}$ will decrease current but increase conductance and *vice versa* for $+V_{pre}$, PPF is achieved with $-V_{pre}$ pulsing, while PPD is pulsed with $+V_{pre}$. The PPF response was modeled to a dual exponential of the form

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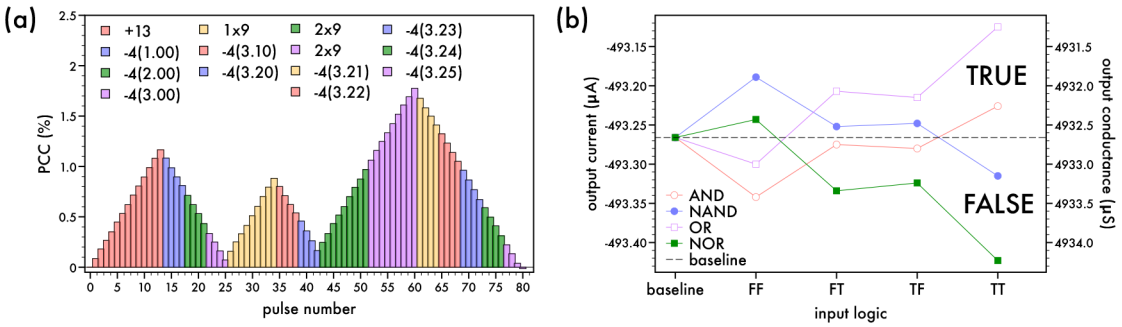

Figure 5. (a) Division operation based on a subtraction-replace-subtraction method for 13 ÷ 4 = 3.25. (b) Basic logical operation output for the cases of AND (red), NAND (blue), OR (lavender), and NOR (green). The dashed line represents the baseline current and conductance state of the device prior to any pulse stimuli and is used to determine logical output.

$$\text{PPF/PPD} = C_1 \exp(t/\tau_1) + C_2 \exp(t/\tau_2)$$

and is observed as a dashed line in Figure 4c. In the equation, τ represents the relaxation time constant and C represents a unitless amplitude. A pair of square-waves with an amplitude of ±1 V and duration of 1 s are applied to the device while monitoring the bottom synaptic electrodes' conductance (synaptic weight) at a constant V_{post} (−0.1 V). The time scales between the two stimuli (Δt) are separated in increments from 50 ms up to 2 s. The difference in conductance states is observed for a set pair of pulses and is calculated by $\Delta G = G_2 - G_1$ where G_1 and G_2 are the conductances of the state immediately after each voltage pulse stimulus. Following PPF ($-V_{pre}$), values for τ_1 and τ_2 are 0.0004 and 275.923 ms, respectively, with $C_1 = 0.529$ and $C_2 = 3.01$. For PPD ($+V_{pre}$), values for τ_1 and τ_2 are 0.0116 and 223.885 ms, respectively, with $C_1 = 3.11$ and $C_2 = 0.542$. This suggests there is a rapid phase relaxation for τ_1 of 0.0004 and 0.0116 ms, respectively, for PPF and PPD and a slow phase relaxation for τ_2 of 275.923 and 223.885 ms.

3.4. Hardware Implementation. Elementary algebra or simple mathematical operations are an essential capability requirement for future neuromorphic computers. To that end, the operation of division can be achieved through loops of repeated subtractions to quantify a quotient, C, for the equation $A \div B = C$ presented for the case of $A = 13$ and $B = 4$ knowing $13 \div 4 = 3.25$ (cf. Figure 5a). The value of the integer quotient n_1 is found that results in the remainder (r_1) such that $0 < r_1 < B$ for $r_1 = A - n_1 \times B$. In this context, $n_1 = 3$ satisfies this requirement with $r_1 = 13 - (3 \times 4) = 1$. The number 13 is initially programmed to the device via 13 sequential +1 V, 1 s square-wave pulses that is then represented by a percent conductance change (PCC) value of 1.166%. The PCC is calculated as the difference in conductance between the initial baseline state (G_0) and the respective programmed voltage-pulsed state (G_n), represented as $\text{PCC} = (G_n - G_0) \times (100/G_0)$. It is important to note that for elementary algebra multiplication can be thought of as addition/subtraction with equal groups. Simply put, the case of $D \times E = F$ implies D groups of E inputs lead to the value F. The first section of the repeated subtraction method then begins with a multiplication step where 3 groups of 4 negative pulses (−1 V, 1 s) are applied to the top synaptic electrode. This lowers the PCC value to 0.072%, the equivalent numerical value of 1. To find the remainder in the decimals format, the remainder (r_1) is then replaced by $r_2 = r_1 + r_1 \times 9$, where $r_2 = 1 + (1 \times 9) = 10$. To program this, 1 group of 9 positive pulses (+1 V, 1 s) is applied to the top synaptic electrode to raise the PCC to 0.883%, or the equivalent value of 10. The consecutive subtractions with the first decimal quotient (n_2) are performed for $r_3 = r_2 - n_2 \times B$ until the criteria $r_n = 0$ is satisfied. For the present case, $r_3 \neq 0$ as $r_3 = 10 - (2 \times 4) = 2$; therefore another sequence of subtraction-replace-subtraction will take place such that $r_4 = r_3 + (r_3 \times 9) = 2 + (2 \times 9) = 20$ followed by $r_5 = r_4 - (n_3 \times B) = 20 - (5 \times 4) = 0$. To achieve this, 2 groups of 4 negative pulses (−1 V, 1 s) are applied to the top synaptic electrode to lower the PCC to 0.165%, or the equivalent value of 2. This is followed by the second series of decimal replaced-subtraction by 2 groups of 9 positive pulses (+1 V, 1 s) to raise the PCC to 1.775%, or the equivalent value of 20. This further proves the linearity and tunability of the device where the PCC for the numerical value of 20 is almost exactly double that for the PCC of the value 10. The division is completed by subtracting 5 groups of 4 negative pulses (−1 V, 1 s) to lower the PCC to −0.014%, or the equivalent value of 0, within the standard deviation of the device. The final quotient (Q) is the sum of the counted integer quotients in the form of $Q = n_1 + 0.n_2 + 0.0n_3 = 3.25$.

The demand for future neuromorphic computational devices requires the ability to process and store information simultaneously within a single device. Boolean logic operations demonstrate the capability of data processing and storage in-memory of a single device, where the physical states of the semiconducting polymer films making up the electronic device represent logic states and operations.[50,51] Boolean logic employs the logical values often represented as TRUE (T) or FALSE (F). Table 1 presents the operational truth tables for the logic gates of AND, NAND, OR, and NOR. For the PPy-

Table 1. Logic-Based Truth Table for Various Single Gate Logic

			truth table			
AND	input	A	F	F	T	T
		B	F	T	F	T
	output		F	F	F	T
NAND	input	A	F	F	T	T
		B	F	T	F	T
	output		T	T	T	F
OR	input	A	F	F	T	T
		B	F	T	F	T
	output		F	T	T	T
NOR	input	A	F	F	T	T
		B	F	T	F	T
	output		T	F	F	F

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based synaptic memristor, tuning the specific amplitudes or durations of the square-wave input pulse represents a TRUE or FALSE value that can lead to the desired output case (cf., Table 2). For the case of the OR gate, a TRUE value is

Table 2. Voltage Pulse Parameters for Each Logical *FALSE* and *TRUE* Inputs

		parameters	
gate	logic	amplitude (V)	duration (s)
AND	F	−1.0	1.0
	T	+0.5	1.0
NAND	F	+1.0	1.0
	T	−0.5	1.0
OR	F	−0.5	1.0
	T	+2.0	1.0
NOR	F	+0.5	1.0
	T	−2.0	1.0

programmed to the device with a square-wave pulse amplitude of +2 V and 1 s duration, while a FALSE value is programmed as a pulse amplitude of −0.5 V with the same duration. Figure 5b presents the output current of the device based on the truth table generated for all logical gate cases. The initial current state of the bottom synaptic electrode is measured as the baseline, which is employed in defining the output logic of the device. Here, a baseline current of $i_{post,O}$ = −493.26 μA is shown as the dashed line in Figure 5b. The definition of the output logic is configured such that $i_{post,O}$ > −493.26 μA results in a TRUE output; otherwise for $i_{post,O}$ < −493.26 μA the output is FALSE. For this device, the bottom synaptic electrode's current is monitored by a −0.1 V constant potential; therefore, a positive voltage pulse to the top synaptic electrode results in an increase in the electrode current and a decrease in the conductance. Following each logical input sequence (FF, FT, TF, TT), a reset sequence is programmed where the previous input program is driven at a negative bias polarity in order to return the device to its initial baseline state preceding the following logical inputs. The math rule of the associative property is evident based on the similarity of the output current states where the input application follows either FALSE then TRUE (FT) or TRUE then FALSE (TF) programs. Similarly, this can be achieved for all simple logic gates AND, NAND, OR, and NOR. It is also important to note that NAND and NOR are the negative operations of AND and OR, respectively.

4. CONCLUSION

In summary, a simple vapor phase polymerization of pyrrole is implemented to fabricate an organic electrochemically based synaptic memristor. The device demonstrates high conductance tunability and linearity over a range of distinct states based on input potentiation or depression parameters. The device, at a more optimized voltage scheme, has an ultralow energy consumption of 4.16 fJ mm^{-2}, mimicking that of actual synaptic and neuronal responses. Implementing current state-of-the-art depositing and printing techniques, such as roll-to-roll and lithography, such devices can be easily mass-produced as well as scaled down in size to further decrease energy consumption. This is a major step toward future neuromorphic computers that exhibit high-end information storage and processing for artificial neural networks.

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Author Contributions

B.G. started the project under the supervision and guidance of S.H.F.; B.G. and T.W. contributed equally with fabrication and electrical testing; Y.B. aided with chemical synthesis; J.C. and L.B. wrote code for the Keithley equipment to preform device measurements; B.G. and S.H.F. discussed results and prepared the manuscript. All authors gave approval of the final version of the manuscript before submission.

Notes

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ABBREVIATIONS

FET	field-effect transistor
OECT	organic electrochemical transistor
CP	conjugated polymer
FeToS	iron(III) *p*-toluenesulfonate hexahydrate
cPECM	conjugated polymeric electrochemical memristor
DI-H_2O	deionized water
VPP	vapor phase polymerization
Py	pyrrole
MeOH	methanol

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PPy	polypyrrole
N_2	nitrogen
ITO	indium tin oxide
SMU	source measurement unit
V_{pre}, V_{post}	voltage
Bu_4NPF_6	tetrabutylammonium hexafluorophosphate
PEI	polyethylenimine
PCB	printed circuit board
SMDs	surface mounted devices
Al	aluminum
i_{pre}, i_{post}	current
R_{CL}	current limiting resistor
t_{pulse}, t_{off}, Δt	time
G, G_o, G_n	conductance
PPF, PPD	paired-pulse facilitation/depression
τ_1, τ_2	time scale
C_1, C_2	magnitude
r_1, r_2, r_3, r_4, r_5	remainder values
n_1, n_2, n_3	counting values
Q	quotient.

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