Editors' Suggestion

Direct growth of MoS_2 on electrolytic substrate and realization of high-mobility transistors

Md Hasibul Alam,[1,*] Sayema Chowdhury,[1,*] Anupam Roy,[1] Maria Helena Braga,[2] Sanjay K. Banerjee,[1] and Deji Akinwande[1,†]

[1]*Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas, Austin, Texas 78758, USA*

[2]*LAETA-INEGI, University of Porto, Engineering Faculty, Department of Engineering Physics, R. Dr. Roberto Frias s/n, 4200-465 Porto, Portugal*

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Although electrostatic gating with liquid electrolytes has been thoroughly investigated to enhance electrical transport in two-dimensional (2D) materials, solid electrolyte alternatives are now actively being researched to overcome the limitations of liquid dielectrics. Here, we report direct growth of few-layer ($3-4L$) molybdenum disulfide (MoS_2), a prototypical 2D transition metal dichalcogenide (TMD), on lithium-ion solid electrolyte substrate by chemical vapor deposition (CVD), and demonstrate a transfer-free device fabrication method. The growth resulted in 5–10 μm sized triangular MoS_2 single crystals as confirmed by Raman spectroscopy, x-ray photoelectron spectroscopy, and scanning electron microscopy. Field-effect transistors (FETs) fabricated on the as-grown few-layer crystals show near-ideal gating performance with room temperature subthreshold swings around 65 mV/decade while maintaining an ON/OFF ratio around 10^5. Field-effect mobility in the range of 42–49 $cm^2\,V^{-1}\,s^{-1}$ and current densities as high as 120 $\mu A/\mu m$ with 0.5 μm channel length has been achieved, back-gated by the solid electrolyte. This is the highest reported mobility among comparable FETs on as-grown single/few-layer CVD MoS_2. This growth and transfer-free device fabrication method on solid electrolyte substrates can be applied to other 2D TMDs for studying advanced thin-film transistors and interesting physics, and is amenable to diverse surface science experiments, otherwise difficult to realize with liquid electrolytes.

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I. INTRODUCTION

Recently, two-dimensional (2D) layered transition metal dichalcogenides (TMDs) have attracted significant research interest due to the unique physical, electronic, and optoelectronic properties suitable for emerging device applications [1–3]. Specifically, molybdenum disulfide (MoS_2), an important 2D TMD, has emerged as a potential candidate for future electronics due to its sizable band gap, heavier electron effective mass than silicon, and outstanding electrostatic integrity due to its 2D structure [4]. High-performance devices have been reported on materials generally obtained from the top-down micromechanical exfoliation method, which is not suitable for practical large-area applications [5,6]. On the other hand, the development of a bottom-up synthesis method like chemical vapor deposition (CVD) has been progressing with recent reports of high-quality crystalline materials on various growth substrates, including both dielectric [7,8] and insulating [9–11] substrates. However, the as-grown material on conventional dielectric substrates suffers from low field-effect mobility (0.1–10 $cm^2\,V^{-1}\,s^{-1}$) [12,13], in a back-gated architecture, attributed in part to the charged impurity scattering due to the trapped charges at the interface [14]. Recent reports have shown the mitigation of charged impurity scattering by using a high-κ dielectric on top of the as-grown material, resulting in higher charge carrier mobility with top-gated device structures [12,15,16]. The preferred deposition technique for the high-κ dielectric film is atomic layer deposition (ALD), which can produce highly uniform and conformal thin films. However, it is not easy to grow high-quality ALD dielectric on pristine TMDs due to the inertness of the 2D surface [17]. Moreover, the deposited high-κ film is reported to dope the underlying TMD channel under certain conditions [18], which can degrade the gating efficiency and device performance. Recently, solid electrolyte substrates, the solid-state cousin of the well-known ionic liquids, have been gaining increased attention due to several inherent limitations of liquid electrolytes such as (i) the strong dependence on the humidity, (ii) the liquid state that prevents various practical applications, and (iii) film stress and freezing at cold temperatures [19–21]. In addition to providing a growth platform, solid electrolyte substrates can also be used as a back-gate dielectric where the charge carrier in the semiconductor channel can be modulated with the formation of electric double layers (EDLs) at the semiconductor channel/electrolyte interface as a result of a back-gate bias. EDLs formed at the channel/electrolyte interface enhanced by ionic conduction act as a nanogap parallel plate capacitor, contributing to a very high dielectric capacitance (1–10 $\mu F\,cm^{-2}$), enabling low voltage operation and high drive current [22]. High-performance TMD transistors with near-ideal gating and improved field-effect mobility have been realized on lithium ion-based solid electrolyte substrate with transferred material, as reported in our previous work [21]. Several other works on 2D FETs based on solid

*These authors contributed equally to this work.
†deji@ece.utexas.edu

electrolyte substrates have also been reported, mainly with exfoliated or transferred CVD material [23–26]. However, the full potential of the transistors cannot be realized with a material transfer, as the device performance is limited by the added polymer residues/contaminants, low yield, material damage, and deformation during the transfer from the growth substrate to the target substrate. As such, a transfer-free method for device fabrication, or in other words, direct growth of TMD on solid electrolyte substrates, is a welcome advancement. However, there is no report of direct growth of any 2D material on solid electrolyte substrates to date.

Here, we report the direct growth of a few-layer ($3-4L$) single-crystal MoS_2 on lithium-ion (Li-ion) solid electrolyte substrate by CVD. High-quality triangular-shaped uniform single crystals were obtained, as confirmed by Raman spectroscopy, x-ray photoelectron spectroscopy (XPS), and scanning electron microscopy (SEM). Next, we demonstrate back-gated transistors on the as-grown crystals and observe near-ideal gating efficiency with room temperature subthreshold swing (SS) around 65 mV/decade and ON/OFF ratio around 10^5. Electrical transport measurement reveals unipolar electron conduction, which translates to a desirable enhancement mode (*e*-mode, usually OFF) operation with a small positive threshold voltage (∼0.40 V), and low voltage operation (<1V). The output characteristics for 0.5 μm channel length show current densities reaching as high as 120 μA/μm with Ohmic-like contacts and current saturation at higher drain voltages. Remarkably, with this back-gated configuration, a field-effect mobility of 42–49 $cm^2\ V^{-1}\ s^{-1}$ has been achieved, the highest reported values among comparable MoS_2 transistors.

II. EXPERIMENTAL METHOD

Growth. We used a single zone furnace for the CVD growth of MoS_2. A schematic of our CVD setup is shown in Fig. 1(a). The substrate from the Ohara corporation (150 μm thick AG-01 LICGC^{TM}) was cut into a rectangle with dimensions 1.7 cm by 2.54 cm and placed face down on an alumina boat containing molybdenum oxide (MoO_3) powder (9.2 mg, 99.5%, Alfa Aesar) in the center of the furnace. Sulfur (S) powder (99.5%, Sigma-Aldrich) was placed in a separate boat upstream, and a separate coil heater was used to heat the sulfur boat. The 1-in. quartz reaction tube was first flushed with 200 sccm of N_2 for 5 min and then purged three times to remove any impurities. After the purging steps, the system was opened to the atmosphere, and the rest of the growth was done under ambient pressure with 6 sccm of Ar/H_2 as carrier gas. The furnace was turned on, and at 550 °C, the sulfur heater was plugged in. The growth occurred at 825 °C furnace temperature and 150 °C sulfur heater temperature for 5 min. After 5 min, the furnace was turned off, and the lid was opened to allow the substrate to cool down. The sulfur heater was turned off when the furnace reached a temperature of 550 °C again. When the temperature went below 100 °C, the substrate was unloaded.

Characterization. Optical characterization was done using an Olympus microscope (BX53M) coupled with their proprietary software *Stream Essential*. Dark-field optical microscopy mode was used as the contrast of the single crystals

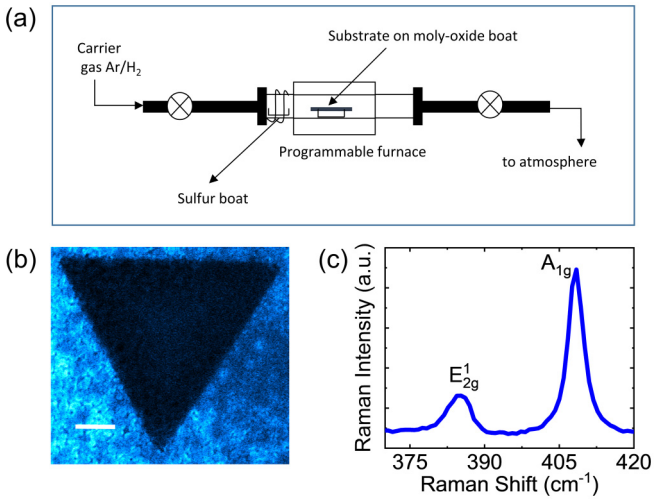

FIG. 1. Experimental setup and material characterization of few-layer CVD MoS_2 directly grown on Li-ion glass. (a) Schematic illustration of the experimental setup used for APCVD growth. (b) False-color SEM image of a typical MoS_2 single-crystal triangle. The scale bar is 1 μm. (c) Raman spectrum of as-grown CVD MoS_2 on Li-ion glass. E^1_{2g} and A_{1g} peaks are located at 384.8 and 408.3 cm^{-1}, respectively. Peak separation ∼23.5 cm^{-1} suggests a $3L$ thick MoS_2.

was not clearly visible in bright field mode. SEM (ZEISS Neon 40) was used to take high-resolution images of the single-crystal MoS_2. Raman spectroscopy was performed in a Renishaw inVia micro-Raman system. An excitation wavelength of 532 nm with beam power ∼1 mW and exposure time ∼10 s was used. A 3000 l/mm grating is used for <5 cm^{-1} resolution. XPS spectra (Omicron Multiprobe system with base pressure below 3×10^{-10} mbar) were acquired using monochromatic Al-$K\alpha$ ($h\upsilon = 1486.7$ eV) operated at 15 kV at room temperature. During the XPS measurement, a charge neutralizer (CN10 electron source for charge neutralization, Omicron, Germany) was used for the charge compensation of insulating/semiconducting materials.

Device fabrication and electrical characterization. Electron beam lithography (EBL) was used to pattern drain/source contact, followed by *e*-beam deposition (10^{-6} Torr) of contact metals (Ni/Au 20 nm/30 nm) and subsequent lift-off. All electrical DC measurements were performed at room temperature in ambient at a sweep rate of 9 mV/sec by using the Cascade Microtech Summit 11000B-AP probe station coupled with an Agilent 4156C parameter analyzer. A LCR meter (HIOKI IM 3536) was used for frequency-dependent capacitance measurement. Quasistatic capacitance-voltage characteristics was measured using Keysight B1500 parameter analyzer.

III. RESULTS AND DISCUSSIONS

Figure 1(a) shows a schematic diagram of the experimental setup used for growing MoS_2 by atmospheric pressure CVD (APCVD). The substrate used for growth is a double side polished Li-ion solid electrolyte glass (or simply Li-ion glass), which is air stable, nonflammable, and thermally stable with an ultraflat surface [27]. The substrate was placed face down on an alumina combustion boat containing roughly 9.2 mg of

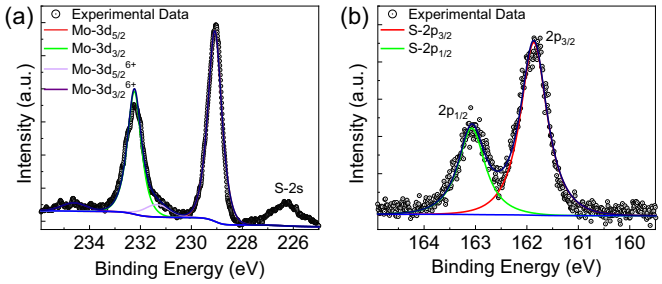

FIG. 2. High-resolution XPS spectra of MoS_2 thin films: (a) Mo-3*d* and (b) S-2*p* core-level peaks of MoS_2, respectively. A Mo/S ratio of 1:1.97 is extracted from the area fit (solid lines) to the experimental data (○). A close-to-the-ideal ratio of 1:1.97 indicates a fairly stoichiometric MoS_2.

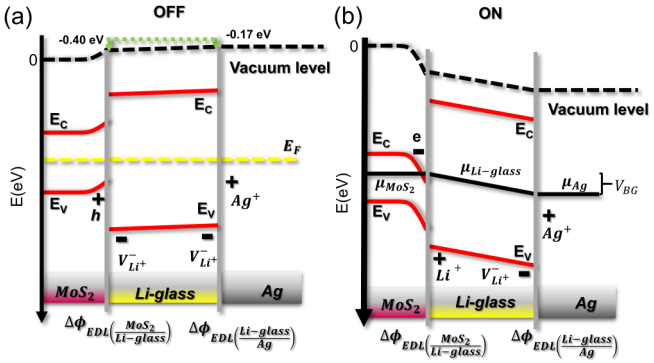

FIG. 3. Schematics showing the energy band diagram of a back-gated CVD MoS_2 FET. The band diagrams were obtained by considering the chemical potential of Ag [37] and channel formation at the MoS_2/Li-ion glass interface. The dashed and solid black lines represent the vacuum levels and chemical potential, respectively. (a) In the OFF state, the alignment of the Fermi levels (dashed yellow line) is made spontaneously by the movement of the Li ions in the electrolyte; the Li ions diffuse to the center of the Li-ion glass substrate, leaving negatively charged vacancies behind and thereby constituting EDLs at both interfaces to allow alignment of the Fermi levels. The adjustment in vacuum level in the solid electrolyte is shown with the green dashed line. (b) MoS_2 FET is in the ON state. The channel is formed when the MoS_2 aligns its chemical potential with that of the Li-ion glass (no EDL forms at the MoS_2/Li-glass interface immediately before channel formation).

molybdenum oxide (MoO_3) powder and loaded inside a 1-in. quartz tube positioned at the central region of a single-zone Lindberg/Blue M furnace. Another crucible containing sulfur powder was loaded into the tube's upstream position and heated separately by a coil heater. The growth was conducted under atmospheric pressure at 825 °C for 5 min. The growth yielded a central region of very thick deposits of a mixture of bulk MoS_2, and unreacted or partially reacted MoO_3, with isolated triangular crystals spread across the periphery of the thick central region as is the case with several other APCVD growths [1,28]. Figure 1(b) shows the SEM image of a typical MoS_2 crystal grown via APCVD on Li-ion glass. Single crystals ranging from 5 to 10 μm in size mostly populate the downstream region of the sample. Raman spectroscopic analyses on the single crystal show a clear presence of MoS_2 from the characteristic in-plane (E^1_{2g}) and out-of-plane (A_{1g}) peaks at 384.8 and 408.3 cm^{-1}, respectively, as seen in Fig. 1(c). The peak separation of $\sim$23.5 cm^{-1} corresponds to 3*L* MoS_2 [29]. The full width at half maximum (FWHM) for E^1_{2g} and A_{1g} peaks are $<$6 cm^{-1} and $<$4 cm^{-1}, respectively, which indicates the high crystalline quality of the as-grown material [28]. To confirm uniformity across the entire crystal, Raman mapping is done on it in a grid configuration with a spatial resolution of 400 nm, by using a 532 nm laser. Raman intensity mapping of E^1_{2g} and A_{1g}, plotted without baseline correction, shows homogeneous color contrast except for few local variations, suggesting the overall uniformity of the as-grown material within the mapping resolution (Supplemental Material Fig. S1 [30]). The local variation can be attributed to the presence of small secondary domains on the primary crystal as well as the surface roughness variation of the underlying substrate [31].

To investigate the chemical composition of the grown material, XPS measurements were carried out, as seen in Fig. 2. The high-resolution XPS spectra of Mo-3*d* and S-2*p* are demonstrated in Figs. 2(a) and 2(b), respectively. The two characteristic emission peaks at binding energies 229 eV (Mo-$3d_{5/2}$) and 232 eV (Mo-$3d_{3/2}$) correspond to the +4 oxidation state of Mo in MoS_2, as shown in Fig. 2(a). An additional peak at 226.2 eV is attributed to S-2*s* peak [32]. Similarly, S-$2p_{3/2}$ (161.8 eV) and S-$2p_{1/2}$ (163 eV) in Fig. 2(b) correspond to the −2 oxidation state of S in MoS_2. These values of Mo and S peak positions closely match with those reported in the literature [33]. Besides the main MoS_2 component, a limited contribution attributed to the presence of MoO_3 is observed at binding energies of 231.3 and 234.8 eV [34,35], which may result from exposure to ambient and/or physically adsorbed oxygen [36]. The integrated peak area of Mo-3*d* and S-2*p* are calculated, and an S-to-Mo ratio of 1.97 is obtained, which suggests that the grown MoS_2 is reasonably stoichiometric. The slight deviation from the ideal stoichiometry of MoS_2 can be attributed to the presence of sulfur vacancies, often associated with CVD growth [28].

To understand the semiconductor channel formation and carrier dynamics in solid electrolyte gated FETs, the electrostatics of EDL formation is of utmost importance. The band diagrams showing the Fermi levels in the Li-ion glass and layers in contact with it (Ag and MoS_2) are shown in Fig. 3. In the OFF state [Fig. 3(a)], the spontaneous alignment of the Fermi levels (electrochemical potential) is achieved by the diffusion of Li ions in the Li-ion glass, leaving negatively charged vacancies behind (anions), therefore the electrolyte may align its Fermi level to the Fermi levels of both materials in electrical contact with its surfaces by locally changing its composition and by the formation of EDLs to achieve

$$\bar{\mu}_{Ag} - \bar{\mu}_{MoS_2} = 0 = \mu_{Ag} - \mu_{MoS_2} + e\left(\Delta\phi_{EDL(\frac{MoS_2}{Li-glass})} + \Delta\phi_{EDL(\frac{Li-glass}{Ag})}\right), \quad (1)$$

where $\bar{\mu}_{Ag}$, $\bar{\mu}_{MoS_2}$ are electrochemical potentials or Fermi levels, μ_{Ag}, μ_{MoS_2} are the chemical potentials, and $e(\Delta\phi_{EDL(\frac{MoS_2}{Li-glass})} + \Delta\phi_{EDL(\frac{Li-glass}{Ag})})$ is the V_{BG} in eV. The semiconductor (MoS_2) and silver (Ag) cannot change their

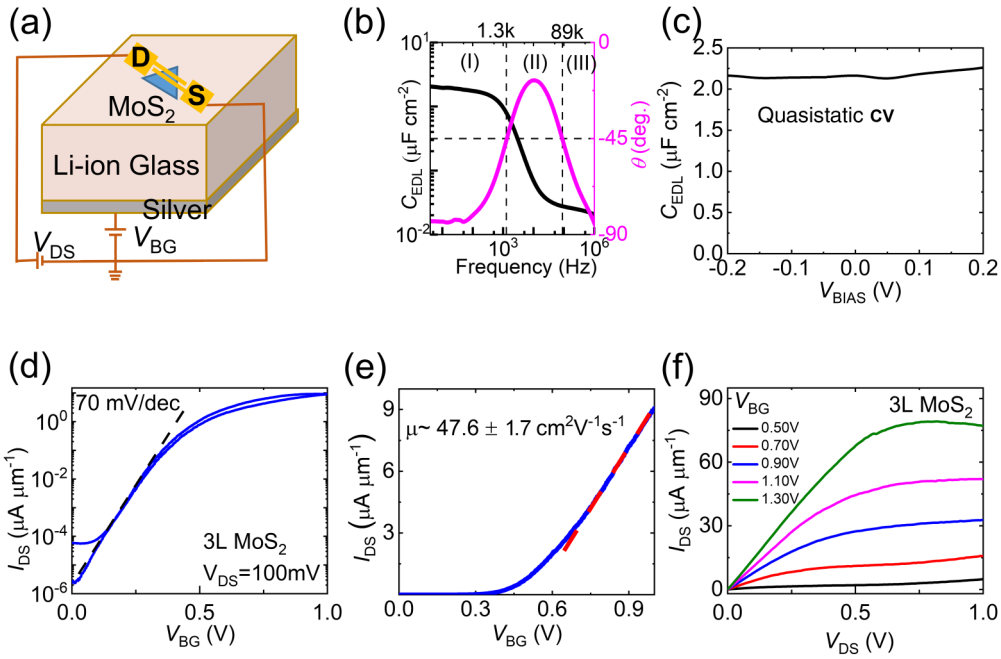

FIG. 4. Electrical characteristics of as-grown 3*L* CVD MoS_2 on Li-ion glass. (a) Schematic diagram of MoS_2 FET on Li-ion glass. Electrical connections are shown with orange lines. (b) Capacitance (phase angle) vs frequency characteristics of a Li-ion glass substrate with top and bottom Ni (20 nm) electrode. The frequency spectrum can be divided into three distinct regions: (I) where EDL is formed, (II) where ion migration dominates, and (III) where the bulk substrate works as dielectric. We note that $C_{EDL} \approx 2.0\,\mu F\,cm^{-2}$ at low frequency ($f = 4$ Hz). (c) Quasistatic capacitance-voltage characteristics of the same structure of (b). We note an average value of $C_{EDL} \approx 2.15\,\mu F\,cm^{-2}$ from the quasistatic measurement. Transfer characteristics of a 3*L* MoS_2 FET in (d) log scale, with V_{TH} approximately 0.40 V and hysteresis voltage <60 mV, and (e) linear scale, where the field-effect mobility of $\sim 47.6 \pm 1.7\,cm^2\,V^{-1}\,s^{-1}$ is extracted from the slope of the linear I_D-V_{BG}. (f) The output characteristics of the same FET. Linear $I_{DS} - V_{DS}$ is observed for small V_{DS} suggesting an Ohmic-like contact. Current saturation is observed for higher drain voltages. A DC sweep rate of 9 mV/sec was used for electrical transport measurement.

chemical potentials without exchanging electrons or holes. Therefore, in the OFF state, the Fermi levels alignment is made by the electrolyte, as shown in Fig. 3(a), and the relationship becomes

$$\Delta\phi_{EDL(\frac{MoS_2}{Li-glass})} + \Delta\phi_{EDL(\frac{Li-glass}{Ag})} = V_{OCV}, \qquad (2)$$

where V_{OCV} is the open-circuit voltage. We note that the local vacuum level of Li-ion glass (green dashed line) shifts downward by an amount of approximately 0.17 eV at the electrolyte/Ag interface to accommodate the alignment of the Fermi levels in the OFF state, as shown in Fig. 3(a) [21]. Once the back-gate voltage is applied to the silver contact, the chemical potential of the silver decreases, whereas that of the MoS_2 increases, and above the chemical potential of the Li-ion glass, the channel is formed. Therefore, electrons are electrostatically induced at the MoS_2/Li-ion glass interface, and the FET is now in the ON state [Fig. 3(b)]. The V_{BG} to form the channel (0.40 V) is indirectly obtained from the I_D-V_{BG} measurements in Fig. 4(d).

Next, few-layer crystals were selected to fabricate transistor devices. Back-gated FET ($L = 0.5\,\mu m$) is fabricated on one of the as-grown 3*L* crystals by patterning drain/source contacts using *e*-beam lithography (EBL), followed by contact metal (Ni/Au 20 nm/30 nm) deposition with *e*-beam evaporation and metal lift-off. All electrical measurements were performed at room temperature under ambient conditions at a DC sweep rate of 9 mV/sec unless otherwise mentioned. The device schematic is shown in Fig. 4(a), with electrical bias conditions. A near-ideal SS of 70 mV/decade was observed from DC electrical measurement on the fabricated back-gate transistor while maintaining the ON/OFF ratio around 10^5 [Fig. 4(d)]. Also, negligible hysteresis (<60 mV) on the order of thermal voltage was observed, as evident from the close agreement between the forward and reverse sweeps. This negligible hysteresis can be attributed to the faster ion movement in the solid electrolyte, consistent with a previous report [21]. Enhancement mode operation with a small positive threshold voltage of approximately 0.40 V was achieved, a desirable feature for low-power electronics. Using an LCR meter (HIOKI IM 3536), capacitance vs frequency of Ni/Li-ion glass/Ni structure was characterized in the frequency range of 4 Hz–1 MHz with an AC signal of 100 mV [Fig. 4(b)]. At $f = 4$ Hz, $C_{EDL} \approx 2.0\,\mu F\,cm^{-2}$ with a phase angle reaching close to $-83\,°$. Quasistatic capacitance (Keysight B1500) was also measured on the same structure, leading to a value of $C_{EDL} \approx 2.15\,\mu F\,cm^{-2}$ [Fig. 4(c)]. As the quantum capacitance of MoS_2 ($C_Q = \frac{q^2 m^*}{\pi\hbar^2}$, therefore $C_{Q,MoS2} \sim 38\,\mu F\,cm^{-2}$) is at least one order of magnitude higher than the C_{EDL} [38,39], we can neglect the effect of C_Q. Hence, we will use $C_{EDL} = 2.075 \pm 0.075\,\mu F\,cm^{-2}$ (average of AC and quasistatic measurements) to extract field-effect mobility. A field-effect mobility value of $47.65 \pm 1.7\,cm^2\,V^{-1}\,s^{-1}$ was obtained based on the linear slope of I_{DS}-V_{BG} [Fig. 4(e)]. Moreover, unipolar conduction is observed, as is evident from the absence of

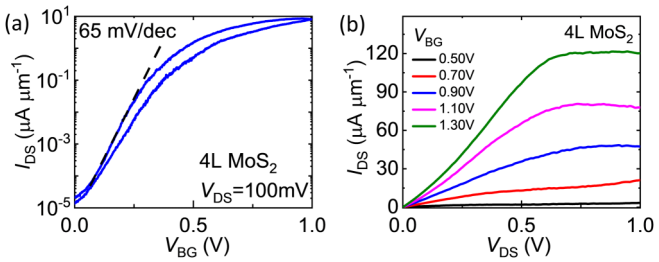

FIG. 5. Electrical characteristics of as-grown 4*L* CVD MoS_2 on Li-ion glass. (a) Transfer characteristics of a 4*L* MoS_2 FET on a log scale. V_{TH} is approximately 0.40 V. Hysteresis voltage is less than 150 mV, and the ON/OFF ratio is around 10^5. (b) Output characteristics of the same FET. Linear I_{DS}-V_{DS} is observed for small V_{DS} suggesting an Ohmic-like contact. Current saturation is observed for higher drain voltages. A DC sweep rate of 9 mV/sec was used for electrical transport measurement.

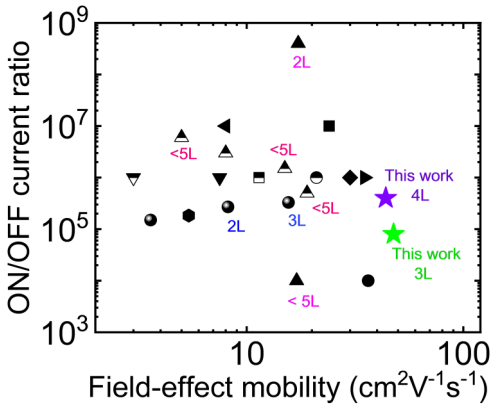

FIG. 6. A plot of the ON/OFF ratio vs field-effect mobility for single/few-layer as-grown CVD MoS_2 FETs. Data from this work (violet and green star) are compared with reported data [7,8,11,45–54] for as-grown single (not labeled) and few-layer (labeled) CVD MoS_2 FETs. Here we considered materials with thicknesses from a single layer up to 5*L* for comparison. The mean value of the mobility data from this work is plotted (without the error bar).

the hole conducting branch in the transfer characteristics, a welcome feature beneficial for complementary metal-oxide-semiconductor (CMOS) amplifiers. The output characteristics of the device are shown in Fig. 4(f), where a linear I_{DS}-V_{DS} is observed for small V_{DS}, suggesting an Ohmic-like contact. Current saturation is seen for V_{DS} greater than the overdrive voltage ($V_{OV} = V_{BG} - V_{TH}$), typical for a well-behaved long channel transistor experiencing channel pinch-off [40]. Output current densities reaching $\sim 80\,\mu A/\mu m$ were achieved with the same 3*L* device.

Another transistor fabricated on a 4*L* MoS_2 demonstrates a similar trend in transfer characteristics such as unipolar electron conduction, enhancement-mode operation ($V_{TH} \sim 0.40$V), and small hysteresis (<150 mV), as shown in Fig. 5(a). The near-ideal gating is also maintained with SS values around 65 mV/decade and an ON/OFF ratio around 10^5, which can be attributed to the collective effect of a clean interface, very high electrolytic capacitance, and low gate leakage current (Supplemental Material Fig. S2 [30]). A high field-effect mobility of $43.86 \pm 1.58\,cm^2\,V^{-1}\,s^{-1}$ was achieved, consistent with the high current densities ($\sim 120\,\mu A/\mu m$) observed in the output characteristics [Fig. 5(b)]. Also, a linear I_D-V_D is observed for small V_{DS} (Supplemental Material Fig. S2 [30]), and current saturation is observed for $V_{DS} > V_{BG} - V_{TH}$, as expected for electrostatically well-behaved transistors showing channel pinch-off [40].

We compared the data against as-grown single and few-layer CVD MoS_2 FETs reported in the literature to put our device data into perspective. Specifically, the ON/OFF ratio vs field-effect mobility was compared for similar FETs (Fig. 6 and Supplemental Material Table 1 [30]). We considered materials up to five layers thick and labeled the legends with layer numbers except for monolayer FETs. The same legends are from the same work, with layer number labeled if it is more than one layer thick. We note that the field-effect mobility obtained in this work is the highest among comparable FETs while maintaining a decent ON/OFF ratio ($\sim 10^5$). The ON/OFF ratio is mainly limited by the OFF-state current, dominated by the gate leakage current through the electrolyte substrate, as shown in Supplemental Material Fig. S2 [30]. The enhancement in the field-effect mobility can be attributed to a clean and smooth interface between the as-grown semiconductor and the underlying channel free from any residue or contaminants usually introduced during the material transfer process. Moreover, a significant reduction of charge carrier scattering in this high-κ dielectric environment offered by Li-ion glass (Li-ion glass $\kappa = 35$) [41] may also contribute to the improvement [42–44].

IV. SUMMARY AND CONCLUSION

In summary, we have demonstrated the direct growth of a few-layer (3−4*L*) MoS_2 on lithium-ion solid electrolyte substrate by CVD synthesis. A uniform, high-quality single-crystal MoS_2 with 5–10 μm average size was obtained. This direct growth enabled transfer-free device fabrication, a critically important step to realize a contaminant-free, clean, smooth, and intimate interface between the semiconductor channel and the underlying substrate. FETs fabricated on the as-grown single-crystals showed near-ideal gating with room temperature subthreshold swing around 65 mV/decade and ON/OFF ratio around 10^5. Desirable enhancement-mode device operation with a small positive threshold voltage ($\sim$0.40 V) was obtained with the device operation under a low voltage supply ($<$1V). Unlike liquid electrolytes, where ambipolar transport is usually observed, unipolar electron transport was realized, suggesting suitability in CMOS circuits. Field-effect mobility in the range of 42–49 $cm^2\,V^{-1}\,s^{-1}$ with ON currents reaching 120 $\mu A/\mu m$ has been demonstrated. The high mobility can be ascribed to the smooth and clean interface of the semiconductor and the underlying solid electrolyte substrate, along with the suppression of Coulomb scattering from the high-κ environment. This demonstrates a route to grow 2D MoS_2 and fabricate transfer-free devices on solid electrolyte substrate, which can be extended to other TMDs to study advanced transistors and enable diverse surface science experiments, otherwise difficult to achieve in a liquid electrolyte platform.

V. OUTLOOK

EDL gating in 2D crystals mainly realized with ionic liquids has shown significant progress in unraveling fundamental transport physics, demonstrating superconductor-insulator transition, mimicking biological synaptic functions, studying spin- and valleytronics, and investigating structural phase transitions [26,55–57]. However, the intrinsic liquid nature of ionic liquids prevents them from forming an ideal platform. Recently, solid electrolyte substrates with high ionic conductivity have been developed, thanks to the extensive progress in battery research. These solid electrolytes can offer similar advantages as ionic liquids with the added benefit of solid-state compatibility. Here we present a solid lithium-ion electrolyte substrate as a platform for the direct growth and realization of high-performance MoS_2 devices. Field-effect mobility extracted from the as-grown crystals shows higher values than the reported numbers in literature for comparable FETs, which can be ascribed to the clean and smooth interface between the semiconductor and the underlying electrolyte substrate. This route of direct growth and device fabrication of 2D MoS_2 can be extended for other TMDs to engineer and study advanced transistors, explore exciting physics, and enable diverse surface science experiments, otherwise difficult to achieve in liquid electrolyte platforms.

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