Progress and application perspectives of voltage-controlled magnetic tunnel junctions

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This article discusses the current state of development, open research opportunities, and application perspectives of electric-field-controlled magnetic tunnel junctions that use the voltage-controlled magnetic anisotropy effect to control their magnetization. The integration of embedded magnetic random-access memory (MRAM) into mainstream semiconductor foundry manufacturing opens new possibilities for the development of energy-efficient, high-performance and intelligent computing systems. The current generation of MRAM, which uses the current-controlled spin-transfer torque (STT) effect to write information, has gained traction due to its nonvolatile data retention and lower integration cost compared to embedded Flash. However, scaling MRAM to high bit densities will likely require a transition from current-controlled to voltage-controlled operation. In this perspective, we provide an overview of voltage-controlled magnetic anisotropy (VCMA) as a promising beyond-STT write mechanism for MRAM devices, and highlight recent advancements in developing VCMA-MRAM devices with perpendicular magnetization. Starting from the fundamental mechanisms, we discuss the key remaining challenges of VCMA-MRAM, such as increasing the VCMA coefficient, controlling the write error rate, and achieving field-free VCMA switching. We then discuss potential solutions and highlight open research questions. Lastly, we explore prospective applications of voltage-controlled magnetic tunnel junctions (VC-MTJs) in security applications, extending beyond their traditional role as memory devices.

1. Introduction

Over the past decade, the semiconductor industry has shown very significant interest in emerging nonvolatile memory technologies. This trend has been driven by the growing demand for computing applications that require large amounts of memory with high bandwidth, low energy dissipation, and low latency[1-8], as well as the increasing difficulty of scaling incumbent memory technologies – notably, embedded static random-access memory (SRAM) and embedded Flash (eFlash) – at advanced semiconductor logic manufacturing nodes.

In addition to potential standby energy savings due to their nonvolatile data retention, the value proposition of emerging technology candidates for embedded memory principally takes one of two forms: (1) A nonvolatile memory technology that can be integrated into existing advanced complementary metal-oxide-silicon (CMOS) logic manufacturing processes with few added masks, and therefore small added costs. This is the case for eFlash alternatives based on magnetic random-access memory (MRAM) below the 28 nm node[9-12]; (2) A random-access memory technology that decreases the portion of the area occupied by SRAM in existing microprocessors, accelerators for graphics and artificial intelligence, and other application-specific integrated circuits[13-16]. Such a higher-density version of SRAM can, in principle, be used to reduce the overall chip area for the same amount of embedded memory, or conversely, achieve larger on-chip memory capacity (and therefore higher bandwidth) for the same constant chip area. The development of embedded MRAM based on the spin-transfer torque (STT) effect to date has been focused on both of these potential applications.

In addition, the large-scale integration of MRAM with high densities in relatively mature CMOS nodes (at the time of this writing, roughly encompassing the 14 to 28 nm nodes) also presents an unprecedented opportunity to rethink the fundamental fabric of computing, beyond only using MRAM as an eSRAM or eFlash replacement. Specifically, emerging memory technologies offer unique physics that can be leveraged to perform computing tasks that are typically challenging to execute using traditional CMOS technology. Examples include utilizing analog weights encoded in memristors to perform matrix multiplication[17-21], implementing stochastic computing to improve the size and energy efficiency of neural networks[22-28], as well as using various in-memory, reservoir, probabilistic, and other physics-based approaches to computing that capitalize on the unique physics of emerging nanodevices[29-33].

MRAM has emerged as the most promising candidate for many of the above-mentioned embedded applications due to its fast write and read speed, high density (using a one-transistor[12, 13] or zero-transistor cell with a two-terminal select device[34]), high endurance, nonvolatile data

retention, and relative ease of integration with existing semiconductor processes, due to the availability of 300 mm volume processing tools.

The basic storage element of an MRAM is the so-called magnetic tunnel junction (MTJ). An MTJ comprises a sandwiched device structure where an ultrathin insulating layer (typically made of MgO) separates two ferromagnetic layers. One of the ferromagnetic layers is fixed by exchange coupling to another hard magnetic or synthetic antiferromagnetic layer, hence referred to as the "fixed layer," while the other ferromagnet is free to switch, making it the "free layer". When the thickness of the insulating layer is thin enough, electrons from one ferromagnetic layer can tunnel into the other, producing a tunneling current that corresponds to a tunneling resistance. The magnitude of this tunneling resistance depends on the relative orientation of the magnetization of the two ferromagnetic layers. When the magnetization of the two layers is parallel to each other, the resistance is relatively low, noted as the “P” state; while when the magnetization of the two layers is anti-parallel, the resistance is relatively high, noted as the “AP” state. These two states, characterized by different resistance values, can be encoded as "0" and "1", respectively, by using appropriate select devices and readout circuitry that convert the resistance difference into a binary voltage signal. This readout mechanism is referred to as tunneling magnetoresistance (TMR)[35-42].

The conventional switching mechanism of existing embedded MRAM is based on current-induced magnetization reversal using the spin-transfer torque (STT) effect[43-47]. As shown in Fig. 1a, a typical STT-MRAM cell integrates a MTJ in series with a field-effect transistor (FET), resulting in a one transistor – one resistor (1T-1R) structure, similar to that of DRAM. However, writing using STT requires a significant amount of current to be passed through the MTJ, thus limiting the scalability to advanced technology nodes due to the need for the FET to drive this current[48-51]. High-speed (few nanoseconds or less) switching using STT also typically requires a larger current, exacerbating this scaling challenge and creating a tradeoff between write speed and endurance of the device. In order to overcome these limitations of STT-MRAM, a potential solution is to use electric-field-controlled phenomena for switching, which eliminate the need for the large write current. This idea is illustrated in Fig. 1b.

A wide range of magnetoelectric coupling mechanisms have been studied for this purpose, which include voltage-controlled magnetic anisotropy (VCMA)[52-59], strain-mediated magnetoelectric coupling[60, 61], coupling of magnetization and polarization vectors in a single-phase multiferroic material[62, 63], as well as the recently demonstrated voltage-controlled exchange coupling (VCEC) in magnetic tunnel junctions[64]. While each of these approaches

comes with its own advantages and challenges, in this perspective, our focus will be the development status and opportunities related to VCMA devices.

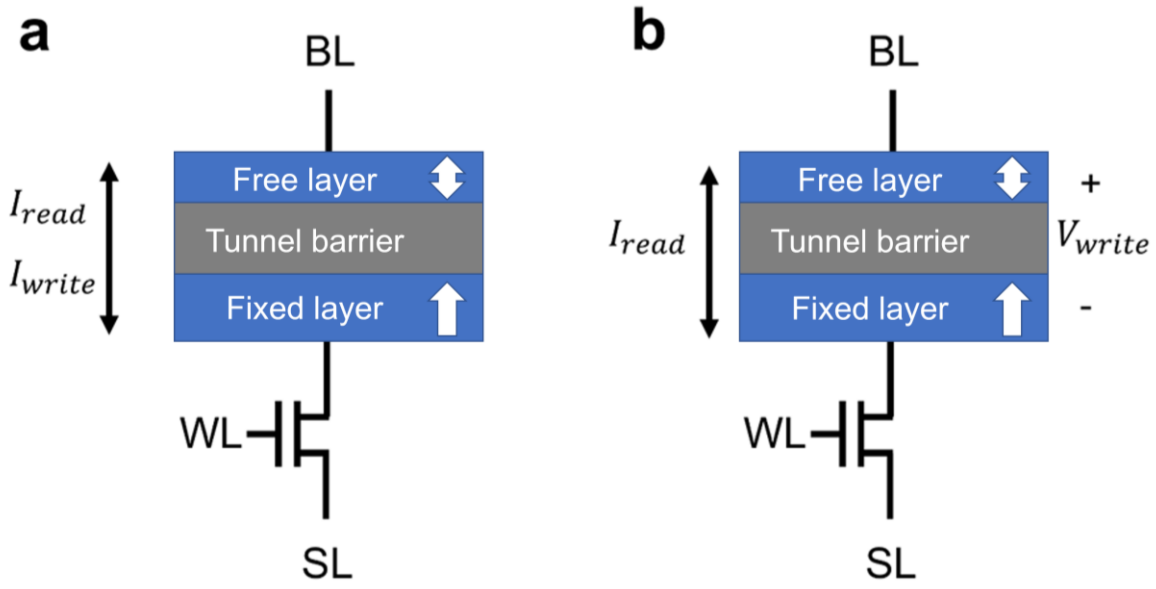

Figure 1. Typical structure of **a** STT- and **b** VCMA-MRAM cells, where the access transistor, bit line (BL), word line (WL), and source line (SL) are also indicated. In STT-MRAM, writing of information is realized via electric current, while in VCMA-MRAM, the write process is realized by an electric field (i.e., voltage), resulting in a smaller access transistor and lower dynamic energy dissipation.

2. Voltage-controlled magnetic anisotropy (VCMA) as a write mechanism for MRAM

As shown in Fig. 1b, the basic idea of VCMA-based MRAM is to use an electric-field-based principle for switching, to enable higher bit density (smaller access transistors) as well as ultra-low power switching due to reduced Ohmic dissipation[53, 65-69].

VCMA was first predicted in theoretical studies that investigated the electric-field-induced spin-dependent screening, which could in turn, modify the surface magnetization and magnetic anisotropy[70, 71]. This was followed by the first experimental demonstration of the VCMA effect in an Fe/MgO structure[53], which is the most widely used material combination in MTJs today (usually, in the form of CoFe/MgO) due to its high TMR. As shown in Fig. 2a, the application of an electric field can change the filling of the hybridized orbitals near the interface, thus adjusting the magnetic anisotropy due to spin-orbit interaction. The manifestation of the VCMA effect at the device level is shown in Fig. 2b. It can be observed that under +1 V, the perpendicular magnetic anisotropy (PMA) of the magnetic tunnel junction free layer is eliminated and the free layer becomes in-plane, while under -1 V, the PMA is enhanced, increasing the coercivity of the free layer[65].

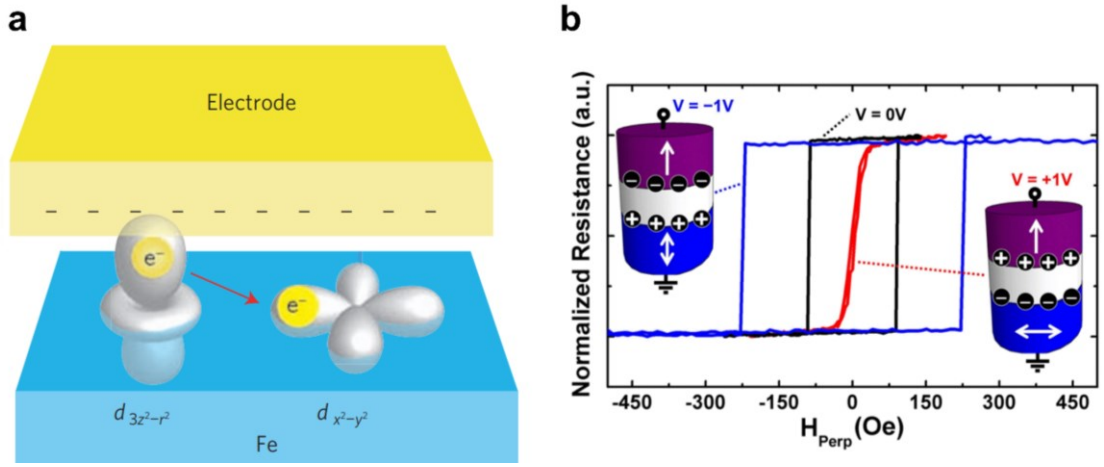

Figure 2. Basic principle and device implication of VCMA. **a** Schematic of the effect of the electric field on the occupancy of 3d orbitals in an Fe layer. Reproduced with permission[53]. Copyright 2009, Springer Nature. **b** Measured magnetoresistance curves of a perpendicular MTJ as a function of perpendicular magnetic field under different bias voltages. Due to the VCMA effect, the coercivity of the free layer increases (decreases) with the application of a negative (positive) voltage. Reproduced with permission[65]. Copyright 2015, IEEE.

By itself, a static VCMA pulse (i.e., having pulse width much larger than the timescale of the magnetization dynamics) cannot result in deterministic switching of the MTJ free layer. However, 180° switching of MTJs via the VCMA effect can be realized dynamically, by applying a voltage pulse across the MTJ, with the pulse duration set to be half of the precession period of the free layer[54, 65, 68, 69, 72-83]. As illustrated in Fig. 3, when a voltage of a certain polarity is applied, the energy barrier E_b between the P and AP states is lowered due to the VCMA effect[53, 67, 70, 84-89]. As the amplitude of the voltage reaches a threshold value, E_b is temporarily eliminated and the magnetization of the free layer starts to precess around an in-plane axis provided by a small in-plane bias magnetic field. By removing the voltage pulse at the halfway of the precession period, the magnetization of the free layer will end up in the opposite direction. Depending on whether the stable free layer states (in the absence of voltage) are in-plane or (more commonly, out-of-plane), the switching voltage must have a polarity that corresponds to the increase or reduction of the PMA due to VCMA, respectively[90].

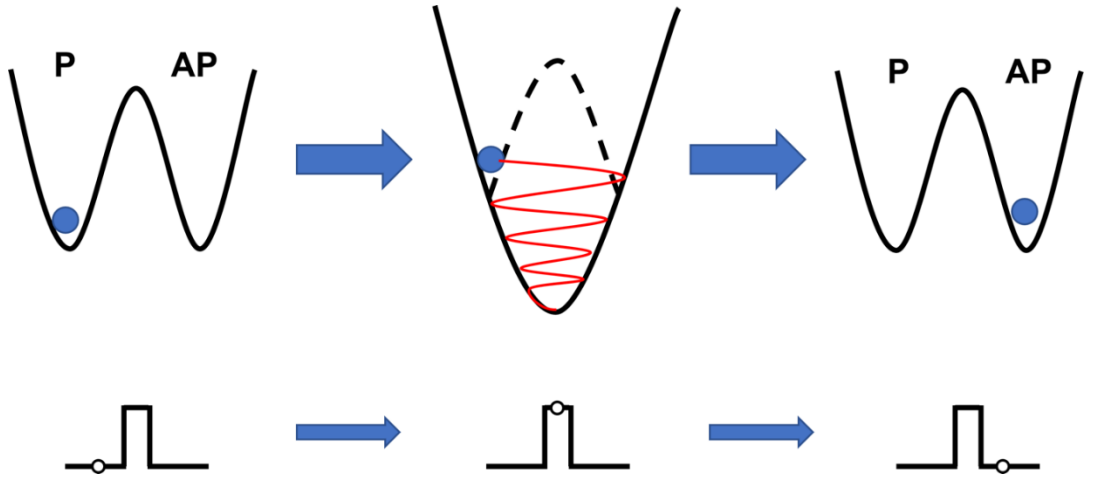

Figure 3. Illustration of VCMA-induced precessional switching. When a voltage is applied, it eliminates the energy barrier between the two free layer states, and the magnetization of the free layer begins to precess around the in-plane bias magnetic field. If the voltage is removed halfway through the precession period, the magnetization will be reversed and ends up pointing in the opposite direction.

There are several advantages of using VCMA as the write mechanism over STT: First, no current is needed for switching, therefore the dynamic power consumption can be much lower (~fJ/bit)[72, 83]. In addition, there is no constraint on the size of the access transistor, as it does not have to provide a large write current to the MTJ. Hence, VCMA-MRAM can in principle be scaled down to more advanced technology nodes while using minimum-sized transistors, thus providing higher bit density. Furthermore, precessional switching via VCMA typically occurs within less than a nanosecond, enabling an ultra-fast write process[72, 83] which is especially important for Cache applications. Moreover, while STT-MRAM suffers from the read disturbance challenge, read disturbance can be completely eliminated for VCMA-MRAM by changing the polarity of the read voltage, taking advantage of the odd dependence of anisotropy on electric field[76, 91]. Finally, VCMA-MRAM usually utilizes MTJs with thicker MgO thickness to eliminate STT contributions to the device dynamics. This increases the TMR ratio, and can also provide better endurance.

3. Challenges and research opportunities for VCMA-MRAM

There are a number of remaining challenges, each presenting exciting research opportunities, when it comes to integrating VCMA-MRAM into practical memory and computing circuits. In this section, we discuss our perspectives on four of these opportunities: (1) Material design to achieve a more efficient VCMA effect; (2) Reliable VCMA switching with low write error rate;

(3) Field-free VCMA-induced precessional switching; and (4) Extension of the VCMA-induced switching concept to materials with antiferromagnetic order.

3.1 Material design to achieve a more efficient VCMA effect

For the practical implementation of VCMA-MRAM, one of the main requirements is to switch the device at low voltages compatible with existing CMOS logic circuits. In precessional VCMA switching, the switching voltage, noted as V_{sw}, is the value at which the energy barrier between the free layer states is eliminated. The switching voltage can be expressed as $V_{\mathrm{sw}} = t_{\mathrm{MgO}} t_{\mathrm{free}} (K_i(V=0)/t_{\mathrm{free}} - 2\pi {M_S}^2)/\xi$[65, 83, 92], where t_{MgO} is the thickness of the MgO tunnel barrier, t_{free} is the thickness of the free layer, K_i is the PMA, M_S is the saturation magnetization, and ξ is the VCMA coefficient that quantifies the magnetic anisotropy's sensitivity to electric fields. As the switching voltage is inversely proportional to ξ, a sufficiently large VCMA coefficient is necessary for low write voltages and to achieve switching of nanoscale MTJs. On the other hand, a large enough energy barrier is needed to maintain sufficient thermal stability. The energy barrier can be written as $E_b = \pi D^2 t_{free} \left(K_i(V=0)/t_{\mathrm{free}} - 2\pi {M_S}^2\right)/4$[65, 83, 92], where D is the diameter of the device. For smaller devices, to have the same thermal stability coefficient $\Delta = E_b / kT$, a higher PMA is needed, imposing an even higher demand for the VCMA coefficient. It can be estimated that for Cache applications with MTJ diameters in the range of ~20 to 30 nm, VCMA coefficients as high as ~300 - 900 fJ/Vm are needed, depending on the required thermal stability coefficient[65, 93, 94].

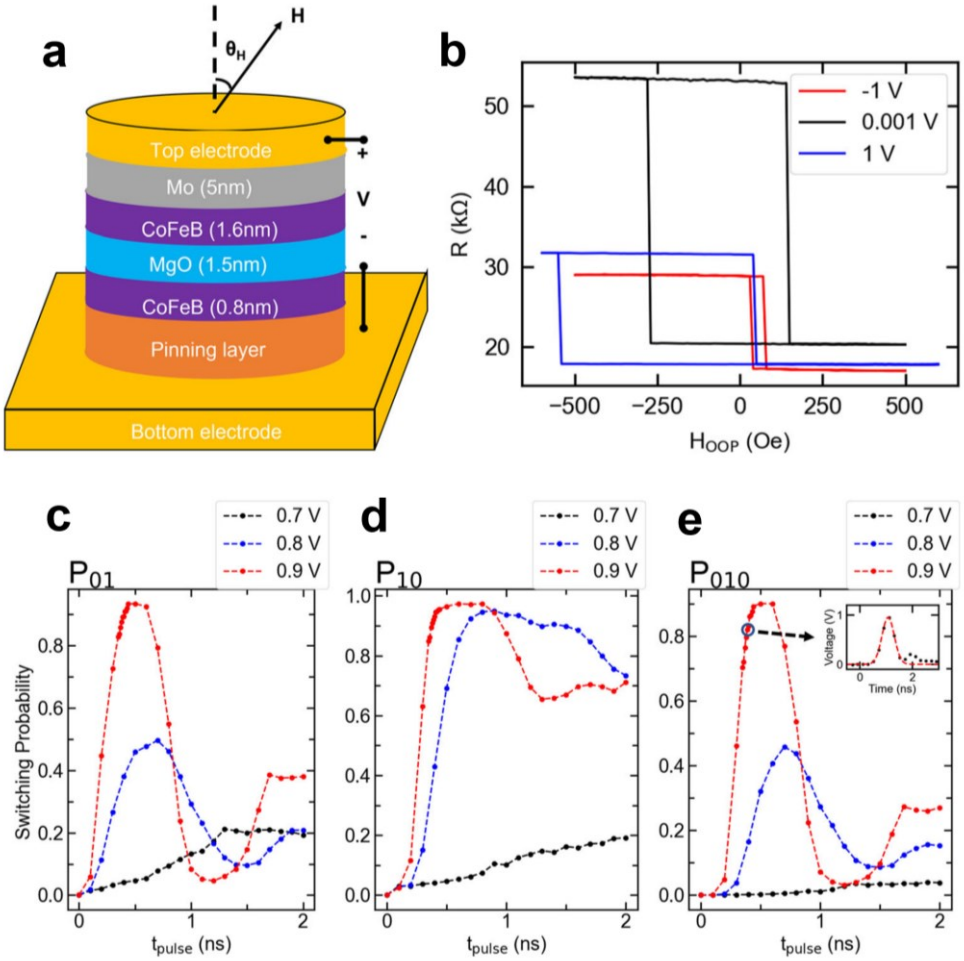

Figure 4. a Schematic of the device structure and **b** measured resistance as a function of magnetic field for perpendicular voltage-controlled magnetic tunnel junctions with high VCMA (130 fJ/Vm), TMR > 150%, and temperature stability after annealing at 400˚C for BEOL integration[94]. **c-e** Measured switching probability under sub-nanosecond pulses for both switching directions (**c** and **d**), and for two successive voltage-induced switching attempts (**e**). Reproduced under the terms of the CC BY 4.0 license[94]. Copyright 2022, Springer Nature.

In the early stages of VCMA-MRAM studies, the VCMA coefficient was limited to relatively low values (~30-50 fJ/Vm), which resulted in relatively high switching voltages (~2 V or higher) and limited the minimum device size that could be switched to 50 nm in diameter or larger[69, 72-82]. Subsequent studies theoretically predicted[95-97] and experimentally demonstrated[98-101] material structures with substantially higher VCMA values, but most of these studies did not advance to performing precessional VCMA switching. This is due to the fact that it is challenging to simultaneously achieve all the required parameters, including high PMA for thermal stability, high TMR for readout, high VCMA for switching and sufficient thermal tolerance (up to 400˚C) to withstand advanced CMOS back-end-of-line (BEOL)

processing temperatures, all within the same MTJ material stack. Additionally, although there have been reports of significant voltage-induced modulation of magnetic properties using magneto-ionic effects[102-114], these effects are not suitable for high-speed precessional switching due to their inability to operate within the sub-nanosecond timescales required for such applications.

Our recent study has shown a significant improvement of VCMA up to 130 fJ/Vm in the CoFeB/MgO/CoFeB system with Mo capping and optimized CoFeB composition, after annealing at 400˚C, while simultaneously achieving TMR larger than 150%[83]. Owing to the high VCMA coefficient, precessional switching was realized at a voltage of ~1 V for 50 nm and 70 nm MTJs and at a voltage of ~2 V for 30 nm MTJs. These results are summarized in Fig. 4. However, further development is still needed for switching of MTJs with a higher PMA and at an even lower voltage. To further enhance the VCMA effect in functional MTJ structures, several different material systems are currently being studied, some of which are discussed in the next sub-sections.

3.1.1 Insertion of a heavy metal at the oxide - free layer interface

A number of *ab initio* computational studies proposed the insertion of an ultrathin heavy metal layer with large spin-orbit coupling (SOC) at the Fe/MgO interface (e.g., Ir or Os), showing that this can enhance the PMA and VCMA[95-97]. Following the theoretical prediction, several experimental studies investigated the VCMA effect in ferromagnet (FM) - dielectric interfaces with heavy metal insertion[99-101, 115]. Figure 5 shows two examples for the enhancement of VCMA in MTJs with Ir insertion at the Fe/MgO interface. VCMA efficiency up to 300 fJ/Vm was observed. It is worth noting that, in *ab initio* calculations, the heavy metal is typically inserted at the Fe/MgO interface, whereas in the real case, the Ir atoms will diffuse into the ferromagnetic layer during the annealing process. As a result, quantitative agreement between the computational and experimental results is not necessarily expected. In addition to heavy metal doping, it was also shown that the strain induced due to the lattice mismatch between the Ir and CoFe layers can also be used to enhance the VCMA effect[98]. *Ab initio* calculations have also been conducted to study the impact of strain on the VCMA effect. VCMA coefficients of > 10,000 fJ/Vm were reported for both Ir capping[95] and doping[96] cases. However, experimental results on such high VCMA coefficients are still lacking, and further materials engineering is still needed for the improvement of PMA and VCMA properties. In addition, the interfacial metal insertion may negatively affect the TMR, which represents a challenge for the development of fully functional memory devices.

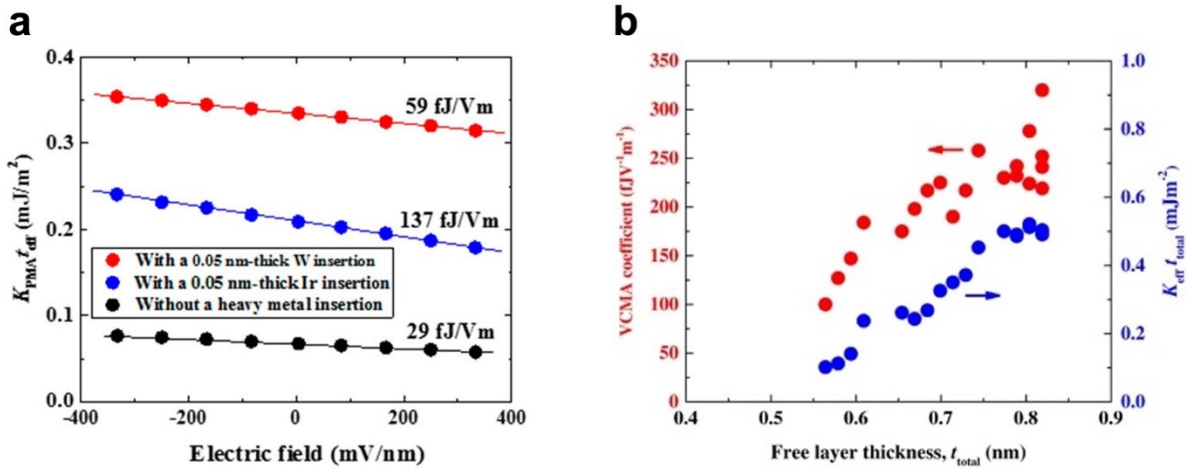

Figure 5. Experimental results on the enhancement of VCMA with heavy metal insertion. **a** Comparison of the electric-field dependences of the PMA energy for MTJs (FeB/Fe/heavy metal/MgO/FeB) with different heavy metal insertions. Reproduced under the terms of the CC BY 4.0 license[101]. Copyright 2017, Springer Nature. **b** Free-layer thickness dependence of the VCMA coefficient (red dots) and PMA energy values (blue dots) for Fe/Ir/MgO/Fe. Reproduced under the terms of the CC BY 4.0 license[99]. Copyright 2018, AIP.

3.1.2 Control of interface oxidation state

As discussed previously, PMA in the CoFeB/MgO system originates from the hybridization between the Fe 3d and O 2p orbitals at the interface. *Ab initio* calculations have suggested that the occupation of the hybridized orbitals can be modified via the charge accumulation/depletion at the CoFeB/MgO interface with application of an electric field[88, 116]. Further theoretical studies have shown that the oxidation level at the Fe/MgO interface can have an impact on the VCMA effect[117, 118]. It was proposed that an ideal abrupt Fe/MgO would give rise to the PMA, while enhancing the VCMA is favored by an over-oxidation state. Li *et al.* confirmed this finding by inserting an Mg layer at the CoFeB/MgO interface[119], and studying the magnetic properties of MTJs with different insertion materials and thicknesses. As shown in Fig. 6, for the Mg insertion case, PMA and M_S both show a peak value around Region III, where an ideal CoFe/MgO interface is expected. The VCMA coefficient shows a peak value of ~100 fJ/Vm at thinner Mg insertion, suggesting that an over-oxidized CoFe/MgO interface will increase the VCMA effect, which is consistent with *ab initio* calculations[117, 118]. A recent study shows a similar result with MgAl insertion[120]. A VCMA coefficient of ~300 fJ/Vm was observed with reasonable PMA values, suggesting the precise control of interface oxidization level can be a useful technique for improving VCMA and PMA properties.

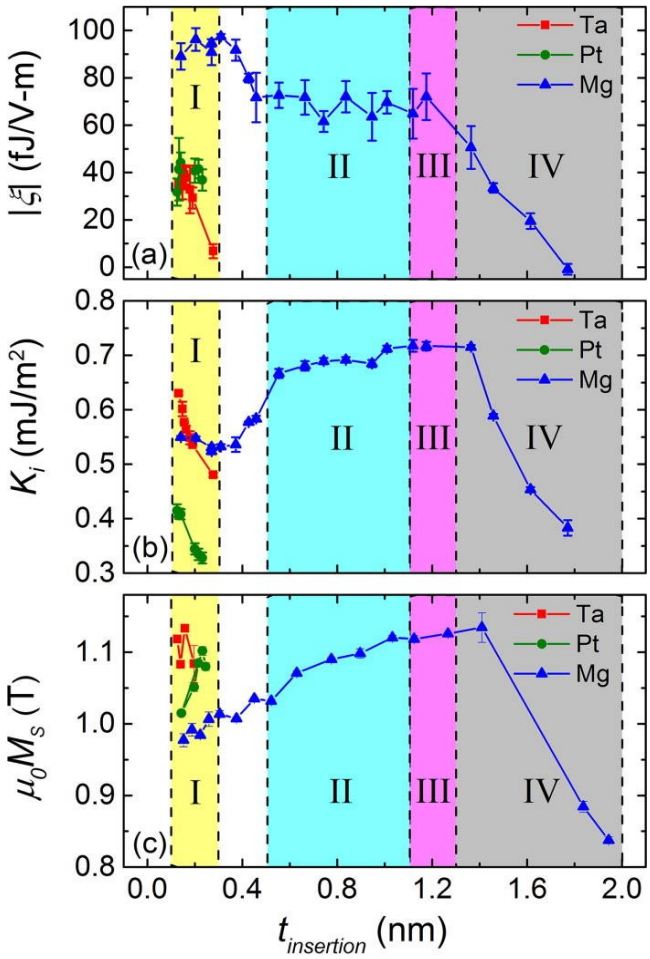

Figure 6. a VCMA coefficient, **b** PMA, and **c** M_S as a function of insertion layer thickness for Ta, Pt, and Mg. Reproduced with permission[119]. Copyright 2017, AIP.

3.1.3 Modification of the dielectric constant

The VCMA effect originates form the charge accumulation at the FM/oxide interface. Thus, the VCMA coefficient ξ is proportional to $\Delta Q/(S\Delta E) = \varepsilon_0\varepsilon_r$[121-123], where ΔQ is the charge accumulation, S is the area, ΔE is the applied electric field, ε_0 is the vacuum permittivity, and ε_r is the relative permittivity (dielectric constant) of the oxide layer. Therefore, exploiting an oxide with higher dielectric constant could potentially increase the VCMA coefficient. There have been a number of studies on the VCMA effect using dielectric layers other than MgO, including HfO_2[123-125] and $SrTiO_3$[122, 126]. However, these approaches did not succeed in realizing functional MTJ structures, due to the low TMR ratio in those systems due to the lack of MgO within the tunnel barrier[127]. Figure 7 shows the VCMA and TMR results on full MTJs with a MgO/PZT/MgO barrier[121]. The VCMA effect is enhanced with the insertion of PZT due to the enhancement of the effective dielectric constant, while maintaining a reasonably high TMR ratio. However, the absolute value for the VCMA coefficient in this case was still low. The key

challenge with this approach is that, in order to realize a high TMR and PMA, the presence of the CoFeB/MgO interface is essential, and as a result, a significant portion of the tunnel barrier thickness will consist of MgO, rather than the high dielectric constant material. Therefore, regardless of the specific high-ε_r material used, the effective dielectric constant enhancement remains relatively small.

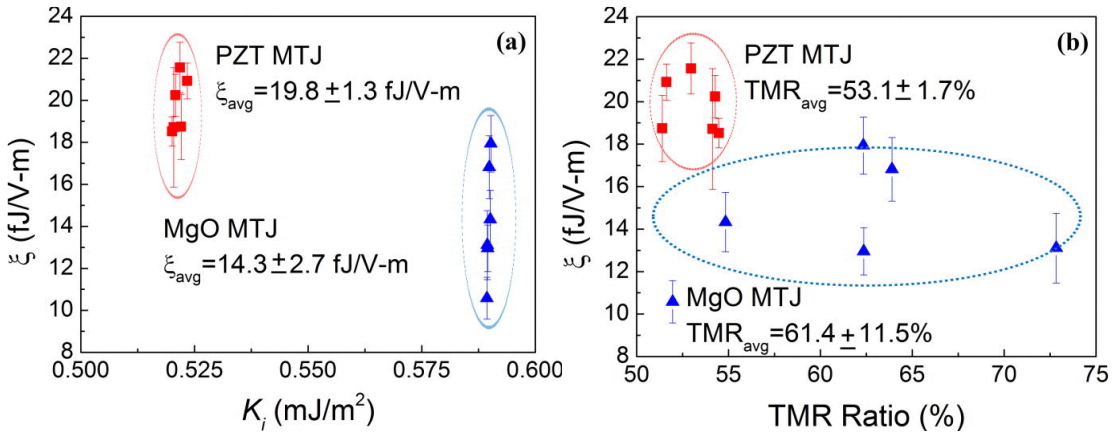

Figure 7. VCMA coefficient ξ, vs. **a** K_i and **b** TMR ratio. The circles are drawn to illustrate the distribution of VCMA coefficients for the MgO and MgO/PZT/MgO MTJs. Reproduced with permission[121]. Copyright 2016, AIP.

3.2 Reliable VCMA switching with low write error rate

For memory applications, a key requirement for any magnetic memory device is to achieve a low write error rate (WER), to reduce the need for error correction and write verification. Due to its resonant mechanism, achieving low WER (as well as good uniformity of WER across large numbers of devices) is a challenge for VCMA-based precessional switching. As discussed in Section 2, the bidirectional switching is realized by a unipolar voltage pulse with certain pulse width. During the application of the pulse, the PMA is eliminated, and the magnetization precesses around the in-plane effective field. Once the pulse is removed, the PMA comes back to its original value, and the magnetization will relax into one of the energy minima. Ideally, the precession trajectory is fixed for a given pulse width, resulting in deterministic 180° switching for an appropriately chosen pulse shape. However, in practice, the precession will be affected by thermal fluctuations, which results in stochastic write errors. In addition, as seen in the inset of Fig. 4e, the real pulse shape in many VCMA switching experiments is not an ideal rectangular shape, which results in additional errors and device-to-device variations. Therefore, an important research need for VCMA-MRAM is to develop methods for reducing WER and the device-to-device variations of resonance characteristics in VCMA-induced precessional switching.

3.2.1 Improvement of thermal stability

Both the WER and read disturbance rate (RDR) of VCMA-MRAM devices are a function of the read/write pulse width and amplitude[76]. While single-pulse WER in VCMA switching can be relatively high, owing to the possibility of fast (sub-nanosecond) write times, it is still possible to achieve very low effective WER using write verification schemes with short overall program time. This was demonstrated in simulations of a 256 Kbit VCMA-MRAM in a 28 nm CMOS process, which showed the capability of the MRAM for delivering WER below 10^{-9} with less than 10 ns total program time, utilizing a write verification process[76]. This highlights the potential of VCMA-MRAM for L3 or last-level (LL) Cache. However, this approach adds circuit overhead and eliminates the possibility of using VCMA devices in applications such as L2 Cache, which require write times of ~5 ns or less. Therefore, further efforts are needed to reduce the WER while maintaining the write speed as well as the energy efficiency.

Using numerical simulations, Shiota *et al.* proposed that the WER can be reduced by increasing the thermal stability (i.e., free layer energy barrier) and reducing the damping of the free layer[75]. As shown in Fig. 8, a larger thermal stability provides lower WER, due to the fact that the thermal fluctuation is reduced before and after the application of the pulse, i.e., the starting position and the relaxation process. Furthermore, a smaller damping is also helpful for lowering WER since the influence of thermal fluctuation during the precession is reduced. Based on this, a WER of 2×10^{-5} was demonstrated without a read verify process by improving the thermal stability[75]. An even lower WER of $< 10^{-6}$ was realized by further optimization of the CoFeB composition[80].

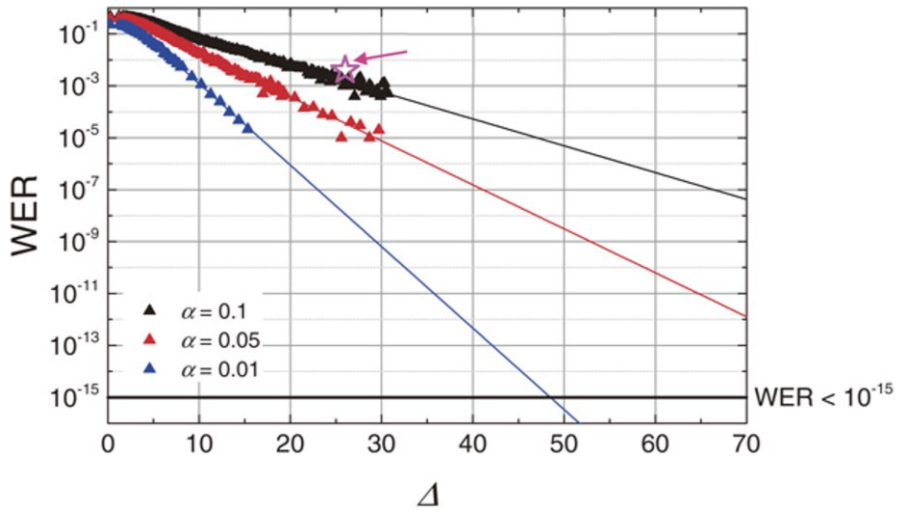

Figure 8. Calculated WER as a function of thermal stability Δ for various damping constants. Arrow indicates typical experimental values of WER obtained in MTJ structures with small VCMA and Δ values. Reproduced with permission[75]. Copyright 2015, IOP.

3.2.2 Use of inverse bias

It is worth noting that, a larger thermal stability requires a higher voltage and/or a larger VCMA coefficient, since the VCMA effect needs to be large enough to eliminate PMA for precessional switching. To address this, a method of using inverse voltage bias was proposed[128], whose effectiveness was later confirmed by numerical simulations[129]. Figure 9a shows the schematic illustration of this idea. During the switching process, a voltage with certain polarity was used to remove the PMA. If reverse voltage pulses with the opposite polarity are applied before and after the write pulse, the PMA at the initial and relaxation states will be enhanced, functioning as an effectively higher thermal stability. Figure 9b shows an experimental demonstration of this method[130]. The reduction of WER was observed experimentally by applying inverse bias. However, the length of the bias voltage pulses applied before and after the write pulse is as large as several nanoseconds, which is not favorable for ultrafast switching applications.

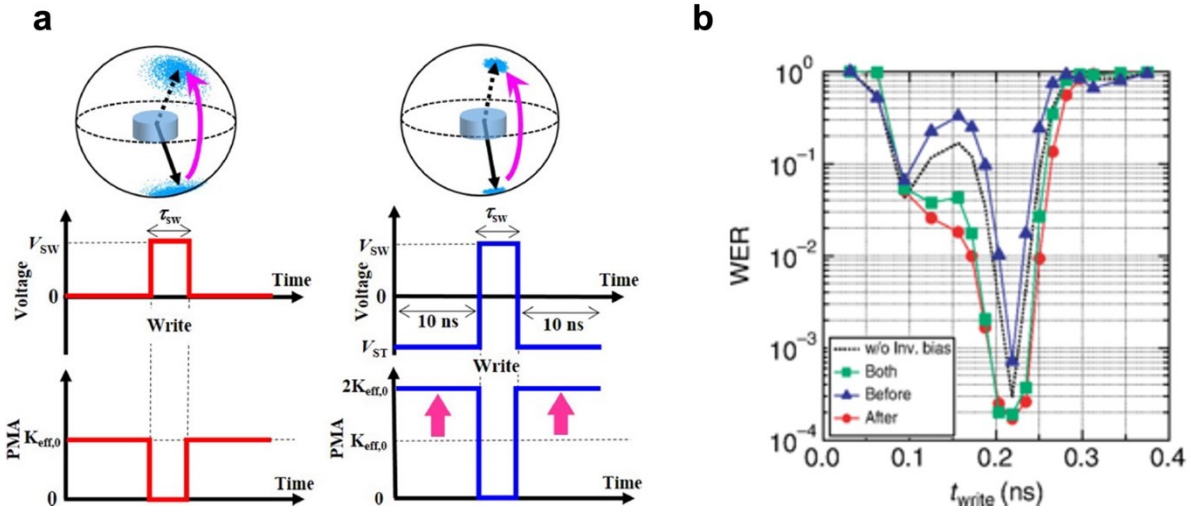

Figure 9. a Schematic illustration of the inverse bias method for reducing WER. The application of the inverse voltage increases the PMA, providing an effectively higher thermal stability. Reproduced with permission[129]. Copyright 2018, IOP. **b** WER experimentally measured using the inverse bias method. Reproduced with permission[130]. Copyright 2020, APS.

3.2.3 Control of pulse shape

Apart from thermal stability, WER may also be influenced by the shape of the voltage pulse, specifically, its rise and fall times. For stable precessional motion, it is necessary for the

effective magnetic field to maintain a constant, in-plane orientation during the pulse application. Lee *et al.* studied the effect of pulse shapes on the precessional switching process using a macro-spin model. They proposed a world-line pulsing method to generate better square-shaped pulses, effectively by using the nonlinearity of the access transistor, when VCMA-MTJs are integrated with CMOS as shown in Fig. 1[131]. As shown in Figure 10a, when a square shaped pulse is applied to the device, the PMA is eliminated abruptly, therefore the effective field becomes in-plane abruptly as well and stays constant during the voltage pulse, which provides a stable axis for the precession of the magnetic moment. However, when a triangular shaped pulse is applied, as shown in Figure 10b, due to the long rise and fall time, the effective field changes gradually from perpendicular to in-plane, resulting in an unstable precession. The free layer magnetization trajectories for both cases are shown in Figures 10c and 10d.

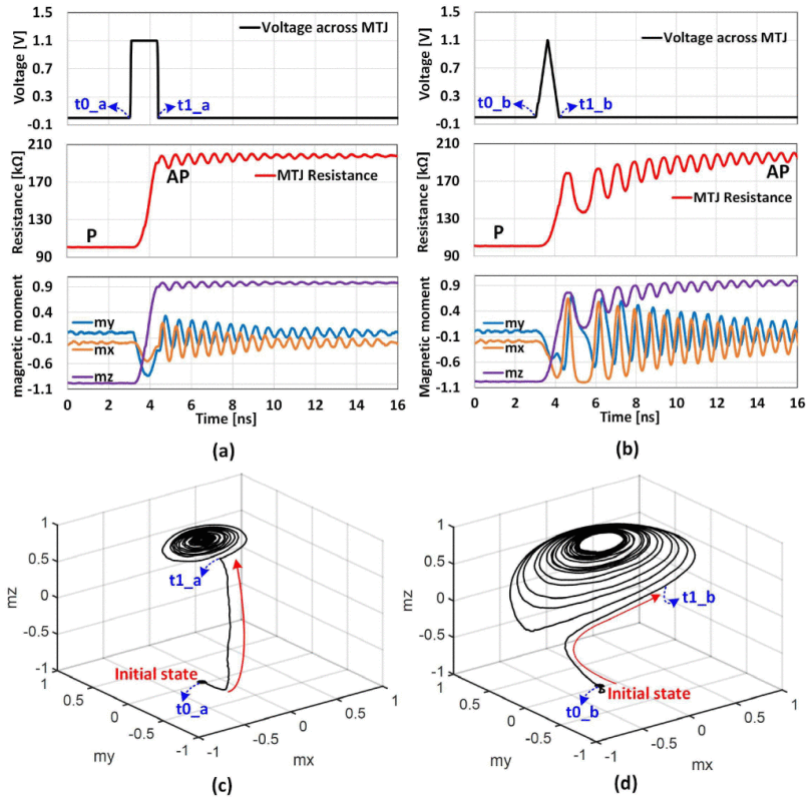

Figure 10. Simulation results for **a** square shaped write pulse and **b** triangular shaped write pulse. **c** VCMA-induced switching with a square pulse shows a more stable trajectory compared to the triangular pulse case shown in **d**. Reproduced with permission[131]. Copyright 2017, IEEE.

A more recent study reported experimental results and a more detailed explanation on the effect of the pulse shape on WER[79]. This work studied the WER for pulses with different rise and fall time, and found that a short and well-defined fall time could reduce the WER. This was attributed to the effect of damping, which reduces the amplitude of the precession. As a result

of damping, for a perfectly square-shaped pulse, the magnetic moment cannot reach the exact opposite point where the other energy minimum is, at the half precession period. On the other hand, when a finite fall time exists, during the fall time there will be an additional effective field term and corresponding torque, which compensate the damping-induced magnetization drift. By precise control of the fall time, this torque can be just enough to pull the magnetic moment to the other energy minimum, thus reducing WER. On the other hand, during the rise time, the extra torque will drag the magnetic moment towards the in-plane direction and will not contribute to improving the WER. Both studies show the potential of reducing WER by controlling the voltage pulse shape. Further studies are still needed for the precise control of pulse shape in real circuits. We expect that the utility of such approaches will exhibit itself particularly well once VCMA-MTJs are directly integrated on CMOS read and write circuity. In this case, the proximity of on-chip transistors will provide more control over the pulse shape than in typical laboratory experiments with probed individual MTJ devices.

3.3 Field-free VCMA switching

As discussed in Section 2, in order to switch the MTJ with voltage pulses, an external in-plane magnetic field is required to define the axis for precession. The application of such an external magnetic field in an integrated chip is impractical. Consequently, field-free VCMA switching is essential for practical applications. Here we briefly discuss some of the methods to address this issue.

One approach to realize field-free switching is to utilize the stray field from a permanent magnet integrated close to the MTJ on the chip. As shown in Fig. 11, Wu *et al.* proposed the integration of a thick Co magnetic hard mask (MHM) on the top of the MTJ cell to provide an in-plane field[81], using which they were able to demonstrate VCMA-induced switching without the application of external magnetic fields. However, there are at least two challenges with this method: (i) The switching time depends on the magnitude of the in-plane field on the MTJ. Therefore, the statistical distribution of the in-plane field can add variability within a chip. (ii) The thickness of the MHM layer is usually relatively large, which may hinder the achievement of small pitch between neighboring MTJs in high-density memory arrays.

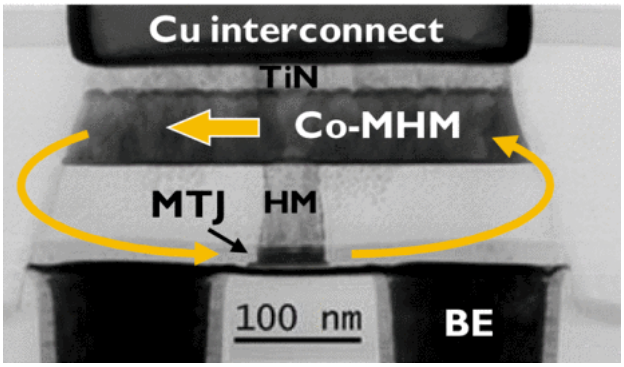

Figure 11. TEM image of the MTJ with a Co-MHM integrated on top of it. Arrows indicate the direction of the magnetization of the Co-MHM as well as the generated stray field. Reproduced with permission[81]. Copyright 2020, IEEE.

Another approach that could potentially realize field-free VCMA switching is to use a conically magnetized free layer (CFL) with an elliptic cylinder shape[132, 133]. When the MTJ is fabricated into an elliptical pillar, due to the shape anisotropy, a shape anisotropy field with an in-plane component will be obtained, which could serve as the bias magnetic field in certain cases. However, since the in-plane shape anisotropy field is proportional to the in-plane component of the magnetization, it cannot help in the case of fully perpendicular free layers. Therefore, the idea of a CFL has been proposed. The conically magnetized state originates from the competition between the first (K_1) and second (K_2) order magnetic anisotropy[134-141]. It has been experimentally studied in various systems including thin Co on Pt or Pd[134], Co/Pt multilayers[135], and Ta/CoFeB/MgO structures[136]. Electric field control of the cone state has also been experimentally demonstrated[137], where an electric field can be used to adjust the cone angle of the free layer. The field-free VCMA switching of CFL MTJs has been demonstrated in macro-spin simulations[132, 133]. While the need for precise control of the second-order anisotropy may make it difficult to realize this concept in practical memory arrays, experimental investigation of the field-free VCMA switching using CFLs remains an exciting research opportunity.

Finally, it may be possible to use exchange bias (EB) to provide a built-in bias field within the device, in a free layer that is interfaced with an adjacent antiferromagnet. This would be similar to an approach that has been applied previously to break the in-plane symmetry of spin-orbit torque (SOT) MRAM devices, in order to achieve deterministic SOT-induced switching[142, 143]. However, the need for simultaneous optimization of EB, PMA, and VCMA within the same material structure presents a significant materials development challenge.

3.4 VCMA-induced switching of antiferromagnetic materials

Materials with antiferromagnetic order are increasingly of interest for MRAM applications, and the study of their SOT-induced switching behavior has been an active and fast-growing research area in recent years[144-147]. This is motivated by their vanishing macroscopic magnetization, which eliminates dipole interactions between adjacent bits (as well as with external fields), making it possible to achieve denser pitch between bits for high-density memory applications. In addition, due to the large built-in exchange field, the dynamics of antiferromagnets occur at much higher frequencies than in ferromagnets, thereby making them potentially good candidates for ultrahigh-speed spintronic devices. However, the same challenges of transistor size and energy dissipation, outlined for current-induced switching of ferromagnets in Section 2, also apply in the case of antiferromagnets. As a result, developing methods for electric-field-induced switching of antiferromagnets is highly desirable. The VCMA effect, which has been predicted to also exist at the interface of various metallic antiferromagnets and commonly used oxides such as MgO[148, 149], could provide a pathway towards this goal[150].

This concept is illustrated in Fig. 12. As in the case of ferromagnetic free layers, the application of a voltage pulse will attempt to reorient the Néel vector $\vec{l} = \overrightarrow{M_1} - \overrightarrow{M_2}$ (i.e., the vector subtraction of the two sublattice magnetizations, the sum of which, $\overrightarrow{M_1} + \overrightarrow{M_2}$, is zero) towards the in-plane orientation. Due to the large exchange field, this occurs via a coupled precession of the two sublattices at a frequency much higher than in the ferromagnetic case (Fig. 12b). If the voltage is terminated while both sublattice magnetizations are near their opposite orientations, as shown in Fig. 12c, the result will be 180˚ switching of the Néel vector. Macro-spin simulations indicate that this switching process can take place in less than ~30 ps for common metallic antiferromagnets[150], which is much faster than ferromagnetic VCMA switching. Interestingly, the threshold electric field required for switching in this case is still only determined by the VCMA coefficient and the PMA of the free layer, and not by the exchange field. Thus, if realized experimentally, this switching concept can provide a pathway towards ultrafast antiferromagnetic dynamics without the need for large currents.

It is worth noting that, there has also been significant progress recently in developing large magnetoresistance effects in heterostructures and tunnel junctions based on noncollinear[151, 152] and collinear spin-split antiferromagnets[153-157], as well as hybrid ferro-antiferromagnetic tunnel junctions[158], which collectively point to a promising future for devices where both writing and reading of information are performed by using the antiferromagnetic order as the state variable[159].

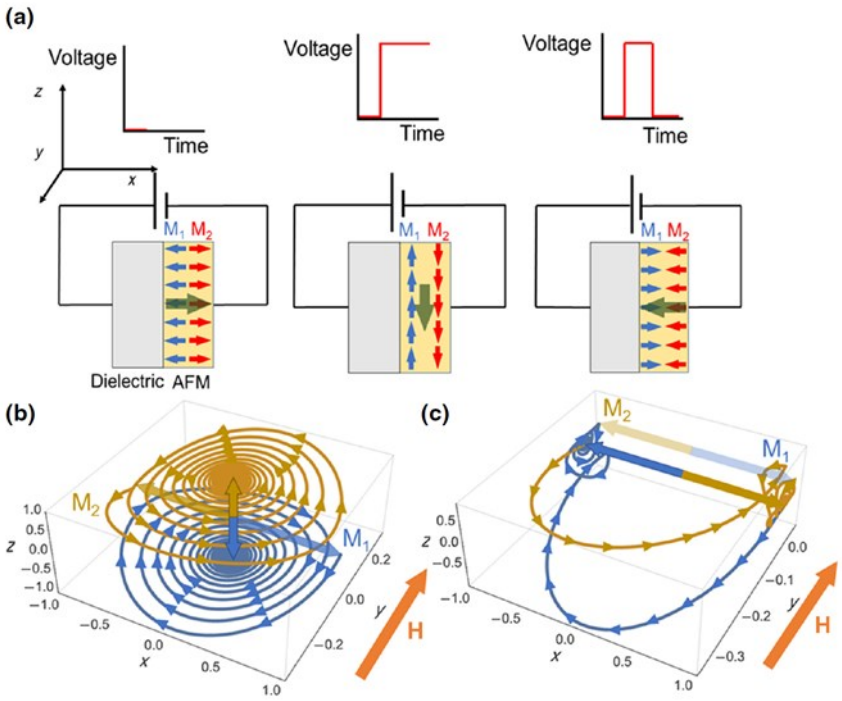

Figure 12. a Illustration of VCMA-induced switching of the antiferromagnetic Néel vector by a short voltage pulse. Bottom panels show macro-spin simulations of **b** 90˚ and **c** 180˚ switching of the Néel vector due to VCMA. Reproduced with permission[150]. Copyright 2019, APS.

4. VCMA-MRAM devices for security applications

In addition to conventional memory applications, VCMA-MRAM has also been studied for security applications due to the growing possibility of integration of MRAM within the semiconductor industry. Here we briefly emphasize two such opportunities that exploit the properties of VCMA-MRAM, namely the use of VCMA for true random number generator (TRNG) and for physically unclonable function (PUF) applications.

4.1 VCMA-MRAM cell for TRNG

In Section 2, we discussed the utilization of VCMA as a switching mechanism for MRAM, wherein a voltage of a specific polarity reduces the PMA in the MTJ. A similar method can also be employed to generate random bits. As discussed in Section 2, upon voltage application across the MTJ, the energy barrier is eliminated, prompting the free layer to initiate a precession around the in-plane axis. The VCMA switching is accomplished by removing the voltage pulse at the half precession period. However, if the voltage pulse is sustained, due to the existence of damping, the magnetic moment will continue to precess with a decreasing amplitude, and will finally relax in the in-plane direction within a few nanoseconds. If we remove the voltage pulse at this point, the easy axis reverts to the perpendicular orientation, causing the magnetic moment

to settle in one of the perpendicular states with equal probability. This phenomenon can be used as a TRNG with a 50% probability[160, 161]. Figure 13 shows the simulation result for random bits generated by MTJ using this VCMA approach. Given its simplicity and compactness, this method could potentially provide a significant power and density improvement compared to conventional pseudo random number generators based on CMOS, which typically consist of thousands of transistors[162, 163].

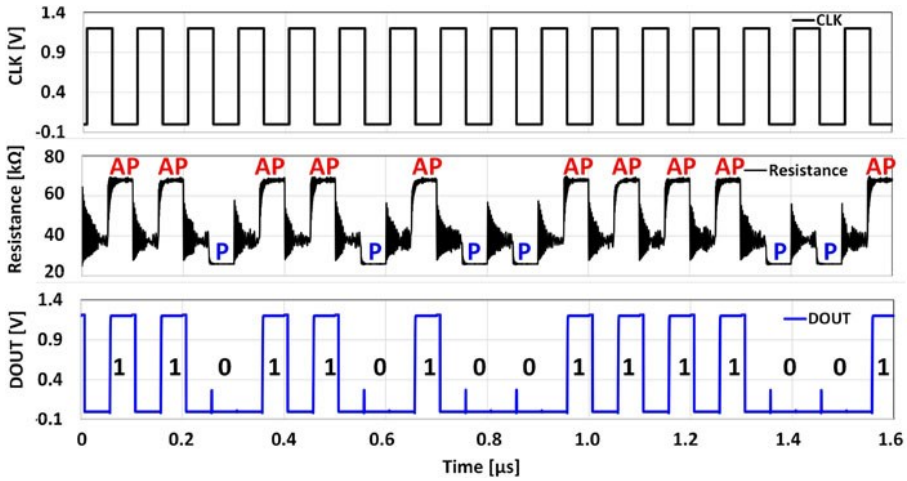

Figure 13. Simulation results of random bits generated by an MTJ using VCMA. The random bit is generated at the falling edge of the CLK signal. The random states of AP and P are converted to digital signals '1' and '0', indicated as DOUT. Reproduced under the terms of the CC BY 4.0 license[160]. Copyright 2017, AIP.

4.2 VCMA-MRAM cell for PUF

Another opportunity for VCMA-MRAM beyond conventional memory are secure hardware building blocks such as PUFs[164, 165]. PUFs are becoming increasingly important in addressing security challenges related to device-level authentication of electronic systems. Figure 14 shows the schematic illustration of a VCMA-based PUF proposed by Tanaka *et al.*[166], where the vertical axis represents the magnetic energy, and the red arrows represent the direction of the magnetization of the free layer. Due to the uncompensated stray field from the fixed layer, there will be a shift of the energy minimum between two free layer directions, resulting in a global minimum and a local minimum, as shown in Figs. 14a and 14d. While this stray field would be zero in an ideal memory device, in practice, it will have a distribution centered around zero for an array of tunnel junctions, with a non-zero shift for each individual device. This shift will be different for each device on a chip, because of manufacturing variations. Initially, the free layer can be in either of its two states. When a voltage with a certain polarity is applied, due to the

VCMA effect, the energy barrier is eliminated and the magnetization will always fall into the global minimum state, and will stay there after the voltage is removed. This represents the PUF state, which can be used to generate a unique fingerprint of a given array of MTJs on a chip.

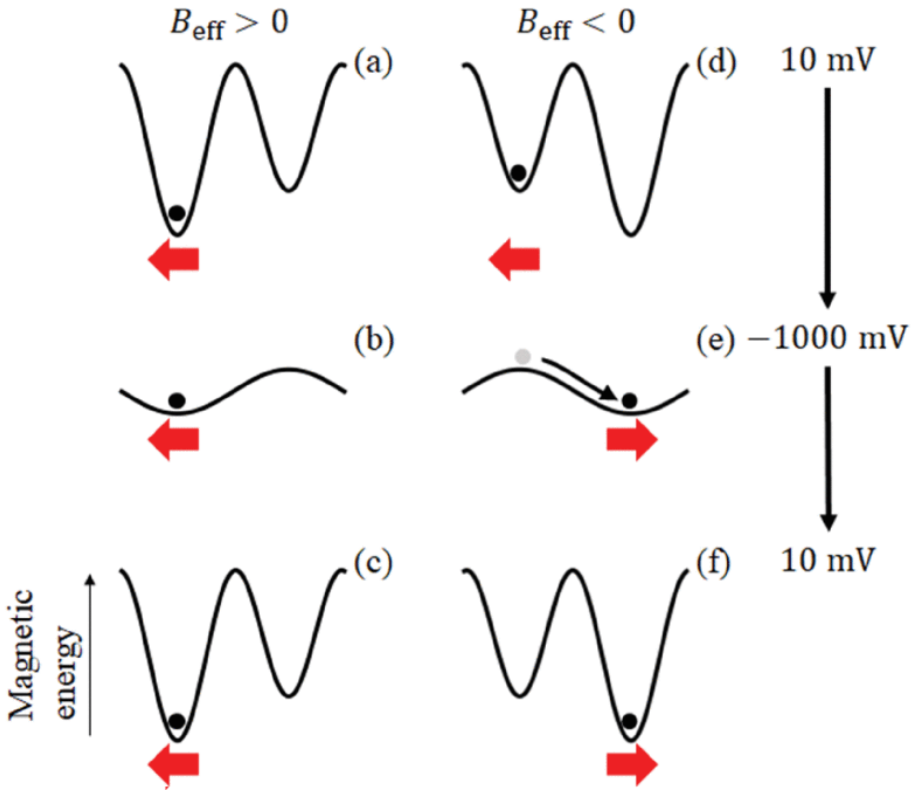

Figure 14. Schematic illustration of a PUF based on VCMA-MTJs. The vertical axis represents the energy of the magnetization and red arrows indicate the magnetization direction of the free layer. Reproduced with permission[166]. Copyright 2020, IEEE.

5. Conclusions

Voltage-controlled magnetic anisotropy offers a promising route towards achieving a combination of performance, density, energy efficiency, and endurance in magnetic random-access memories beyond existing current-controlled MRAMs. The switching can be realized with sub-nanosecond voltages pulses, resulting in fast and ultra-low power write operations, making it a promising candidate for Cache applications. Its unipolar write process also allows for the elimination of read disturb issues by taking advantage of reverse voltage sensing. There are exciting opportunities for further impactful research on VCMA materials and devices. Further materials engineering is required to reduce the write voltage by increasing the VCMA coefficient. Write error rates can be potentially lowered by suppressing thermal fluctuations, precise control of the pulse shape, and by taking advantage of circuit techniques adapted to the

physics of the VCMA devices. The necessity for the external in-plane magnetic field needs to be eliminated, with possible approaches including the integration of magnetic hard masks, utilizing canted free layers with optimized higher-order anisotropies, and even by using built-in exchange bias. In addition to memory applications, the integration of VCMA-MRAM devices with CMOS also unlocks new opportunities for innovation in security and unconventional computing applications. Finally, extension of the VCMA writing mechanism to other types of magnetic order such as antiferromagnets presents an exciting direction for both fundamental and applied research.

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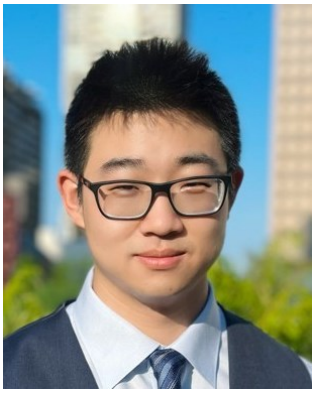

Table of contents entry:

Electric-field-controlled magnetic tunnel junctions that use voltage-controlled magnetic anisotropy (VCMA) for switching provide a path towards magnetic random-access memory (MRAM) with improved density and energy efficiency. Here we discuss the recent progress of VCMA-MRAM and highlight key research opportunities, including increasing the VCMA coefficient, controlling error rates, and field-free switching. We also discuss potential applications of VCMA-MRAM in security applications.

Y. Shao, P. Khalili Amiri*

Progress and application perspectives of voltage-controlled magnetic tunnel junctions