

# Fault Tolerance for Islandable-Microgrid Sensors

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**Abstract**— This paper presents defect tolerance strategies for islandable-microgrid sensors both at the sensor level and at the matrix (or deployment) level. A microgrid is a group of interconnected distributed power/energy sources and loads with well-defined electrical boundaries that act as a single controllable entity with respect to the main grid or other micro-grids, and can connect or disconnect from them to operate in both grid-connected or island modes. Often the control for islanding depends on the monitored voltage and frequency – and sometimes the phase and even the harmonic content, of the units involved. Therefore, accurate estimation of these parameters – especially in transient modes – is critical for successful islanding. We propose Interpolated FFT for this objective, which does not need adaptation and appears to perform well with high accuracy. Also, IpFFT can be implemented on a chip, and is therefore amenable to distributed deployment. Defect tolerance in the sensor system is important for such sensors including fabrication-time yield enhancement, in field self-repair, and system level recovery. The paper discusses a VLSI architecture for the IpFFT algorithm, needed IC cells, with emphasis on defect and fault tolerance from the VLSI chip point of view.

**Keywords:** *Microgrid, islanding, sensors, estimation of key variables (frequency, phase and amplitude), defect and fault tolerance, yield and reliability improvement.*

## I. INTRODUCTION

Electrical grids are becoming increasingly heterogeneous consisting of a mixture of the main grids and microgrids [1]-[3] worldwide and need smart, fault tolerant chips to control them. There is thus an increasing interest in microgrids which can provide multiple benefits including economic, sustainability, and even environmental. They can operate in a permanently islanded mode [4]-[8] or a connected mode: connected to other microgrids or the main grid. When operating in the connected mode it is important to be able to connect or disconnect from them to operate in both connected or island modes for quickly localizing blackouts, or for isolation from the other microgrids or main grid when those are suffering from instability. In Fig. 1 an abstract view of a microgrid is shown, where microgrid MG1 is connected to three other microgrids, MG2, MG3, and MG4, as well as to the main grid G1. Shown also are the power switches which allow connection or disconnection; the latter results in islanding.

Often the control for islanding depends on the monitored voltage and frequency – and sometimes the phase and even the harmonic content, of the various units involved. Therefore, accurate estimation of these parameters – especially in transient

modes – is critical for successful islanding. Although several methods have been proposed in the literature for frequency estimation, including the familiar FFT, they suffer from a couple of disadvantages, which include exclusion of amplitude and phase, need for filter adaptation, and the need for commercial DSP boards. We propose Interpolated FFT (IpFFT) for this objective, which does not need adaptation, and appears to perform well with high accuracy. Also, IpFFT can be implemented on a chip, and is therefore amenable to distributed deployment. However, defect and fault tolerance is important for such sensors which includes fabrication-time yield enhancement, in field self-repair, and system level recovery. The paper discusses a VLSI architecture for the IpFFT algorithm, needed IC cells, with emphasis on defect and fault tolerance from the VLSI chip point of view. (An actual chip has been presented elsewhere [15].)

Finally, just as the VLSI systems have permeated the communications, imaging, and video technologies, there are tremendous opportunities for VLSI systems to contribute to the power and energy domains, both from the research perspective and from the societal perspective.

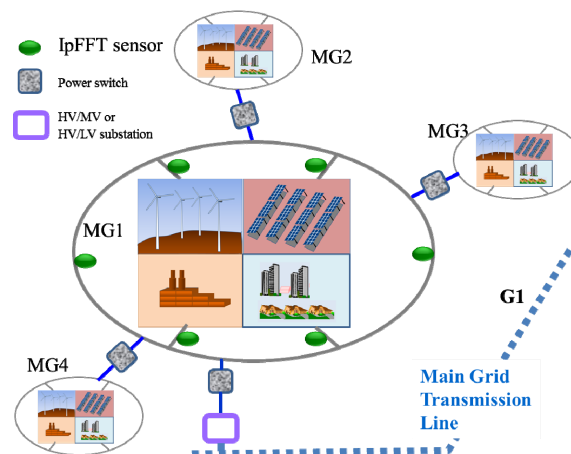


Fig. 1 An abstract view of islandable-microgrid with three neighboring microgrids; not shown are the connections among the sensors and the switches (wired, or wireless)

## II. EMERGING MICROGRID TECHNOLOGY

### A. Why Microgrids

In contrast to the centralized power systems microgrids

may be considered as the key to distributed power and energy systems (DPES). Potential advantages of DPES are redundancy, modularity, fault tolerance and reliability, efficiency, and lower design cost. The following references provide rich information on all these aspects [1]-[8]. So, what is a microgrid? It is a somewhat autonomous electrical subsystem with multiple distributed power and energy resources, with multiple loads, and distribution interconnections. It also allows for variability of renewable power and energy sources. In this section we lay out the control issues for microgrids and what that requires in the VLSI smart sensors of section IV required to solve this problem.

Microgrids comprise distributed power and energy sources with low or medium voltage distribution systems with storage devices and loads, optionally connected to the utility grid in a controlled way. The operation of microgrids offers distinct advantages to customers and utilities such as improved energy efficiency, minimization of overall energy consumption, reduction of environmental impact, and improved reliability of power system. They form a key element within the SmartGrids concept.

### B. Islanding, Control strategies, and Sensor Requirements

The power systems operated by the utilities suffer from an increasing gap between demand and generation, inadequate transmission capacity, and nonuniform location of the load centers and generating stations. Occurrences of faults in such systems, in most cases, end up with the worst consequences (i.e., complete blackout). These can be prevented through segregation of the system into a number of viable islands together with generation and/or load shedding. As stated in Subsection A above, this is inherent in the concept of microgrids.

Islanding can also be used in the utility grid. Such intentional islanding is the purposeful sectionalization of the utility system during widespread disturbances to create "islands". These islands can be designed to maintain an uninterrupted supply of power during disturbances of the main distribution system. The grid sectionalizes itself. The distributed power and energy resources can then supply the load power demand of the islands until reconnection with the main utility system is considered healthy. In such disturbances voltages at the buses suffer from non-diminishing swings, as do the output frequencies. In general, the more the number of islands, the shorter the duration of restoration. The nature and location of any fault that warrants such islanding can be ascertained in real time through monitoring of frequency, voltage amplitude, phase, harmonics, and the active-power flows at both ends of a number of prespecified lines. Given below are some mathematical relationships drawn from [4]-[8].

The control strategies and sensor requirements can be found in references [4]-[8]. Here are two examples where fast and accurate frequency measurement is critical.

$$f = f_0 - k_P \times P \quad (1a)$$

$$V = V_0 - k_Q \times Q_1 \quad (1b)$$

$$f_{01} = f_{grid} + k_P \times P_1 \quad (2a)$$

$$V_{01} = V_{grid} + k_Q \times Q_1 \quad (2a)$$

For explanation of the symbols, see [4]-[7]. A phase measurement based algorithm is described in [8].

## III. INTERPOLATED FFT

### A. FFT

The familiar FFT needs no discussion, except to mention that the accuracy of estimation is good only if the frequency or frequencies of interest coincide with the FFT frequencies. To clarify this briefly, let us introduce the following notation:

$T$  Frame length

$N$  Number of samples

$\Delta$  Sampling interval =  $T / N$

$F_s$  Sampling frequency =  $1 / \Delta$

$\nu$  Frequency resolution =  $1 / T$  (which in the

literature is sometimes denoted by  $df$  or  $\Delta f$ )

Example:  $T = 200$  ms,  $F_s = 800$  Hz,  $N = 160$ ,  $\nu = 5$  Hz,

$$\Delta = 1.25 \text{ ms.}$$

So, in the above example, if the frequency of interest were 57.0 Hz, it is likely to be estimated as 55 Hz, and the amplitude and phase estimates will also be of a poor quality. This is amply remedied in both THA and IHA.

### B. Tomic's Harmonic Analyzer (THA)

The algorithm is rather complex, inasmuch as it requires adaptation, hence it is not used in our sensors. The reader is referred to [9] for details.

### C. Interpolated FFT harmonic analyzer (IHA)

Due to lack of space the reader is referred to [15].

### VLSI Architecture for IpFFT sensor

#### C. Complex FSA

Fabricated in 0.5 micron CMOS technology [10], Fig. 2 shows the VLSI architecture for the complex Fourier analysis [10] for two frequencies with FFT indices  $k$  and  $k+1$ . The sensor coils typically take a large part of the chip area and finer technologies lead to higher resistances; hence 0.5 micron technology suits them well.

#### A. Complex Multiplier

A complex multiplier 0.5 micron CMOS technology was presented in [10]. It is flexible and allows for multiplication of complex numbers and their conjugates or multiplication of a combination of complex and real numbers. As shown in Table 2 of [10], the following expression can be computed in a maximum of 4 clock cycles:

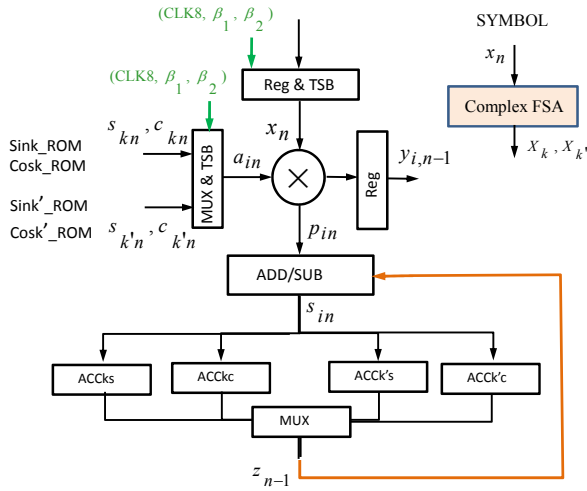


Fig. 2 Complex FSA

$$\begin{aligned} (a + jb)(c + jd) &= (ac - bd) + j(ad + bc) \\ &= X + jY \end{aligned} \quad (9)$$

### B. Computation of Key Parameters

Fig. 3 provides the VLSI architecture for the estimation of the fundamental frequency, phase, and amplitude.

Estimation cell in the VLSI architecture: The estimation cell shown in Fig. 3 requires a linear computation cell (multiply and add/acc), and a nonlinear cell with the following three functionalities: reciprocal, sine, and arctangent. But a square-root functionality is required on the left hand side. So a single nonlinear cell with four functions is required. Fortunately, these are precisely the four functions incorporated in our single-cycle nonlinear cell [12],[13] which has been used in several more recent VLSI architectures. Hereafter, this cell will be called UNL (Universal single-cycle NonLinear) cell.

## V. DEFECT TOLERANCE

To create a fault tolerant system requires a nested set of defect correction strategies:

(a) intra-chip fault tolerance which corrects faults that develop during manufacturing in a complex 3D sensor that involves both sensor layers, complex processing layers and RF communications layers to gain desirable module yields.

(b) chip or sensor level fault tolerance – sensors chips are located in harsh environment (temperature, humidity, weather, high magnetic fields, voltages,) Furthermore the system must also deal with soft/hard errors over time due to cosmic radiation, and

(c) (power) system level fault tolerance: the detection of failures within the power system (faulty/failed transmission lines, transformers etc).

The last one is implicit; therefore we discuss the first two, which relate to fault tolerance within the sensor system. To

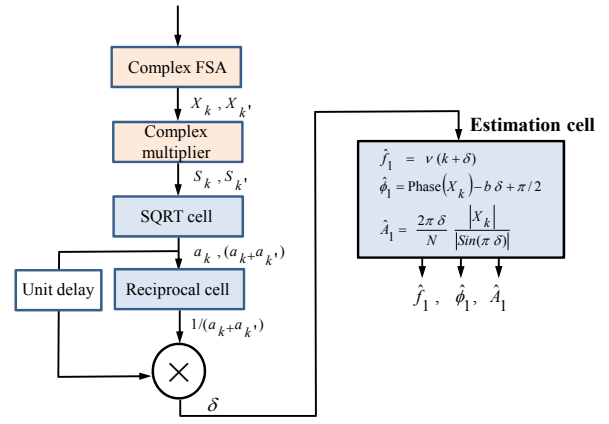


Fig. 3 VLSI architecture for fundamental frequency, phase, and amplitude.

overcome (a), the computing blocks in the chip are provided with redundancy, as discussed below. To achieve (b), sensor level redundancy, or sensor matrix redundancy, is used. That is the devices are distributed, separated by a distance D, uniformly.

For (a) above spares are used. As seen from Fig. 3, four types of cells are needed: the Complex FSA (CFSA), the Complex multiplier (CM), and the underlying cells for the blue-shaded boxes in Fig. 3, which is a single cycle linear cell (MAP) with multiply add/subtract/accumulate capability, and a single UNL cell.

We now discuss the defect tolerance with just one spare of each type of cell.

### Defect Tolerance for IHA Using Spares

As mentioned above, four types of modules are needed. Let  $M_1$  denote the number of CFSA's needed,  $M_2$  denote the number of CM's needed,  $M_3$  the number of MAP's needed, and  $M_4$  the number of UNL's needed to accomplish the configuration of the desired multiplier. Now suppose that  $N_1 \geq M_1$  denote the number of CFSA's provisioned,  $N_2 \geq M_2$  denote the number of CM's provisioned,  $N_3 \geq M_3$  MAP's provisioned, and  $N_4 \geq M_4$  denote the number of UNL's provisioned. Let  $p_1$  denote the probability that a CFSA cell is tested good,  $p_2$  the probability that a CM is tested good,  $p_3$  that an MAP is tested good, and  $p_4$  the probability that a UNL is tested good. Then, with the definition

$$Y_i = \sum_{m=M_i}^{N_i} \binom{N_i}{m} p_i^m (1-p_i)^{(N_i-m)}, \quad i = 1, 2, 3, 4$$

the yield for the IHA is given by  $Y = Y_1 Y_2 Y_3 Y_4 Y_C$ . Here,  $Y_C$  denotes the probability of successful interconnection circumventing the defective cells.

*Example:* Suppose the silicon areas of the three types of cell are  $A_1, A_2, A_3$ , and  $A_4$ , respectively, and that the defect

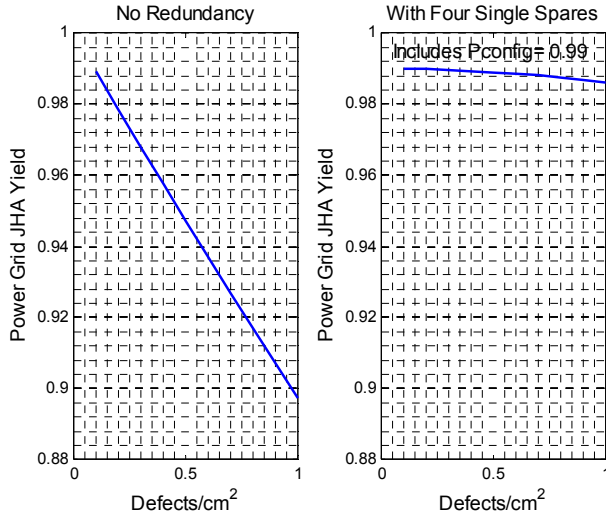


Fig. 4 Predicted yield vs. defect density, without spares and with single spares for all four cells (JHA=IHA)

density is denoted as  $D$  defects/cm<sup>2</sup>. Then using a Poisson defect distribution,

$$p_i = e^{-A_i D}, \quad i = 1, 2$$

and  $A_1=2.502$  mm<sup>2</sup>,  $A_2=2.062$  mm<sup>2</sup>,  $A_3=1.00$  mm<sup>2</sup> and  $A_4=5.263$  mm<sup>2</sup>, the above formulas lead to the predicted yield vs. defect density shown in Fig. 4. The figure on the left shows the yield without any redundancy, and the one on the right for the case with a single spare of each type. Clearly, redundancy is needed since it boosts the yield to a level of 0.986 for otherwise it could be at a level of 0.897 at a defect density of 1 defect/cm<sup>2</sup>. However, at a defect density of 0.1 defect/cm<sup>2</sup>, the decision becomes more difficult: the yield without redundancy is predicted to be 0.989 while with redundancy it is predicted to be 0.999, although it is based on an interconnection success probability of 0.99 – which might be higher.

## VI. MATRIX LEVEL FAULT TOLERANCE

In a future paper we will consider the following scenario. For each faulty sensor, (a) one sensor upstream and another downstream are both healthy [14]. It is depicted in Fig. 5.

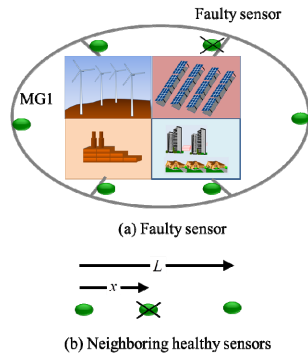


Fig. 5 Faulty and healthy neighboring sensors

## VII. CONCLUSIONS

We have presented defect tolerance strategies for islandable-microgrid-sensors both at the sensor level and at the matrix (or deployment) level. As discussed, the control for islanding depends on the monitored voltage, frequency, phase and sometimes the harmonic content, of the units involved. We have proposed Interpolated FFT for this objective, which does not need adaptation, and appears to perform well with high accuracy. Also, IpFFT can be implemented on a chip, and is therefore amenable to distributed deployment. The paper has discussed a VLSI architecture for it, needed VLSI cells, with emphasis on defect and fault tolerance from the VLSI chip point of view on the one hand and from a system or matrixed deployment point of view on the other.

## ACKNOWLEDGMENT

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