Fault Detection in Three Phase Power Transmission Lines, a TI Microcontroller Implementation, and a VLSI Architecture

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2021 North American Power Symposium (NAPS) | 978-1-6654-2081-5/21/$31.00 ©2021 IEEE | DOI: 10.1109/NAPS52732.2021.9654580

***Abstract*—An important emerging area for VLSI systems is power grids, microgrids, and their transmission lines. Transmission line protection is an important issue in power system engineering because more than 80% of system faults occur in transmission lines. Most of those systems are three phase systems. This paper presents a method for monitoring those three phases on a single output line from a micro-controller/micro-processor-4, which we have named as Γ-line. This innovation is important since a power network has multiple transmission lines emerging from a generator station. The paper also presents the theory for detecting the type of fault and for estimating the distance of the fault from that Γ-line. As a second part of the paper, another micro-controller/micro-processor-3 is used to compute the running DFT/FFT of a signal in real time. A VLSI Architecture for some parts of the algorithm is also presented. The micro-controller/micro-processor-4 is TI TMS320F28379D, and the micro-controller/micro-processor-3 is TI TMS320F28335.**

***Index Terms*—Digital Signal Processing (DSP), digital filters, micro-controller,VLSI**

I. Introduction

While being one of the most beneficial engineering creations, the electrical power transmission line can cover ranges of a few km to hundreds of km making them vulnerable to different kinds of climate catastrophes, large scale fire storms, etc. Therefore, it is imperative to detect the faulty line quickly and to take efficient remedial measures to minimize the damage on the overall system. In the widely used three phase systems these faults may be classified as:

1) Single line-to-ground fault (LG)
2) Line to line fault (LL)
3) Double line to ground fault (LL)
4) Three phase symmetrical fault (LLG)

These are complicated by the unknown location of the fault and the associated fault impedance(s). For example, in the LG case the location could be at a distance $\alpha(D)$ from the source, where $0 < \alpha < 1$, D is the physical length of the line, and the impedance from L to G could be Z_f. Further, in the case of arc faults harmonics play a role [1], [2], [3]. Still further, the load could be a Y-connected load or a Δ-connected load, stated somewhat simplistically. Clearly, sensors play a key role in the beneficial objectives stated in the paragraph above. A useful remark is the following; since the sensing and computations are to be performed on the chip, the VLSI chip may be more appropriately called a Heterogeneous System on a Chip (HSoC) [4], [5], [6], [7], [8], [9], [10].

The overall scope of this problem is immense, so this paper deals with some portions of it, which can lead to further research on a large scale. This paper presents a method for monitoring those three phases on a single output line from a micro-controller/micro-processor-4, which we have named as Γ-line. This innovation is important since a power network has multiple transmission lines emerging from a generator station. This paper will also present the theory for detecting the type of fault and for estimating the distance of the fault from that Γ-line. As a second part of the paper, another micro-controller is used to compute the running DFT/FFT of a signal in real time.A VLSI Architecture for some parts of the algorithm is also presented.

The rest of the paper is organized as follows. Section II describes developed fault studies Simulink model. Section III is about the hardware implementation on TMS320F28379D. Section IV details the sliding DFT with the help of TMS320F28335. Section V details the mathematical derivation of distance estimation of LG fault. Section VI is about the developed VLSI Architecture. Section VII concludes the paper.

II. Fault Studies Simulation Model

Fig. 1 presents a MATLAB/SimPowerSystems model developed to conduct the fault studies. The three-phase source voltage is provided using a controllable voltage source. Transmission line is modeled as a T-circuit, with Section 1 and Section 2 having lengths l_1 and l_2, respectively. It is noted that l_1+l_2 = D. The fault location is at the junction of Section 1 and Section 2 and is labeled as "F." A Y-connected resistive load is also connected to the system. The transmission line model adopted is presented in Fig. 2.

The next step was to create a "Γ- line" to observe the three-phase signals (current and voltage). This was achieved in multiple stages. First, the sampling rate of the three-phase voltages was changed using the "rate transition block." With the help of a "buffer block", the time domain signals were

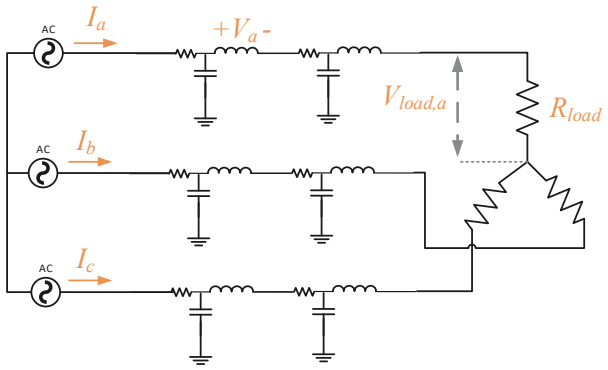


Fig. 1: Block diagram of the model developed in MATLAB/SimPowerSystems for fault studies.

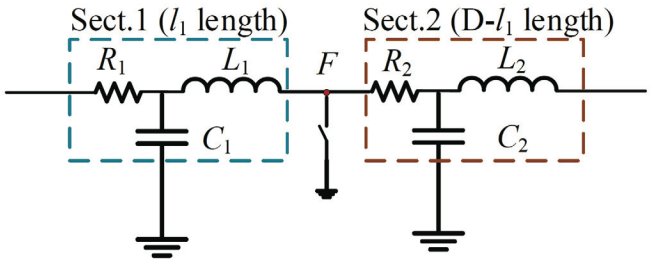


Fig. 2: Transmission line model adopted for fault studies.

converted into frames, with a buffer size of 167 per channel. Then, the "vector concatenate" block is implemented to merge all the channels, equivalent to a 3-to-1 mux operation. Lastly, "unbuffer" is used to combine the frames and form a "Γ- line." Fig. 3 presents the block diagram of the "Γ- line" formation.

A. Case Study 1

The model presented in Fig. 1 is implemented for two cases. Case 1: Without any introduction of a fault. Case 2: A single line to Ground fault at point "F," where l_1 = 20 miles. Load is assumed to be Y-connected. Parameters used in this paper are adopted from are [11] and are listed in Table I .

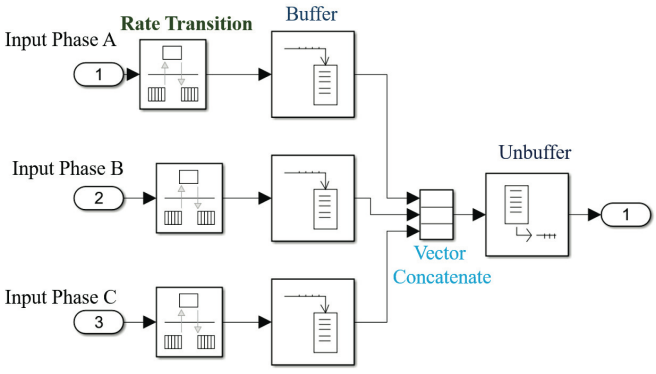


Fig. 3: Block diagram to create the "Γ line" with the help of rate transition, buffer and unbuffer block.

TABLE I: Parameters used for simulations and hardware implementation.

Parameter	Value
R_1, R_2	0.2 Ω /mile, 0.2 Ω/mile
L_1, L_2	1.1 mH/mile, 1.1 mH/mile
C_1, C_2	5.3 nF/mile, 5.3 nF/mile
l_1	20 miles
l_2	30 miles
Load	100 Ω/phase
Sample Rate	20 kHz

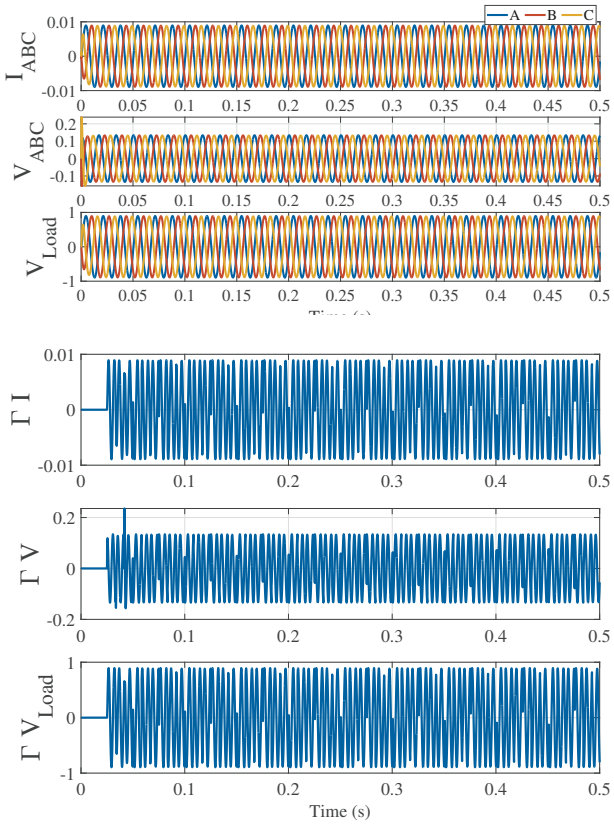


Fig. 4: Simulation results for the three-phase current I_{ABC}, voltage V_{ABC} and the load voltage $V_{Load,ABC}$, and the Γ- lines for the current, and the voltages.

Fig. 4 and Fig. 5 presents the results for the two case studies. The SLG fault is introduced at t=0.2s.

B. Case Study 2

In this section, we discuss the case where the fault location "F" is varied. Here, we change the length l_1, such that l_1 + l_2 = D. As discussed earlier, a similar SLG fault is applied at the fault location, at t = 0.2 s. **Note:** The total length of the transmission line is D = 50 miles. Fig. 6 presents the ΓV_{Load}

TABLE II: Peak value of the load voltage (V) in steady-state, when fault location is varied.

Distance	$V_{Load,A}$	$V_{Load,B}$	$V_{Load,C}$
0.25 D	0.2709	0.8896	0.8841
0.5 D	0.1543	0.8896	0.8842
0.75 D	0.1083	0.8896	0.8842

for the cases when fault location is changed.

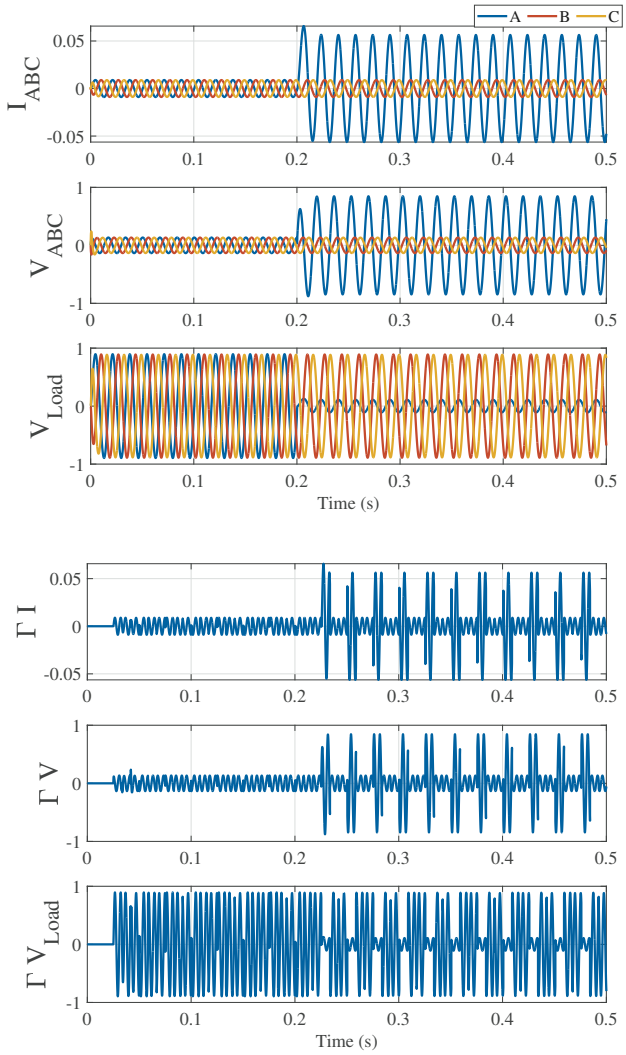


Fig. 5: Simulation results for the three-phase current I_{ABC}, voltage V_{ABC} and the load voltage $V_{Load,ABC}$, and the Γ- lines for the current, and the voltages. The single line to ground fault is introduced in Phase A at t= 0.2s.

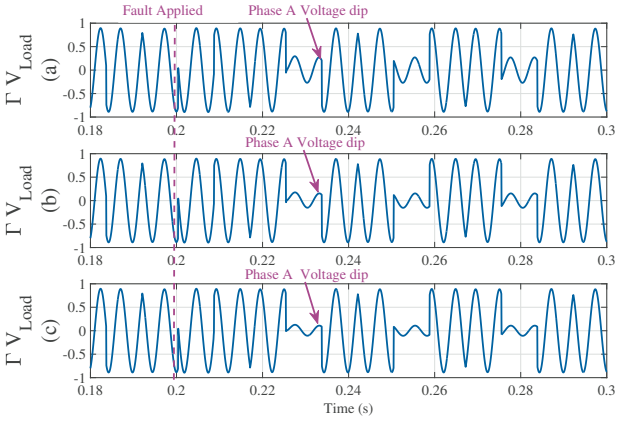


Fig. 6: The plots show the Γ- line for V_{Load}, when the fault location is changed. (a) 0.25D (b) 0.5D (c) 0.75D.

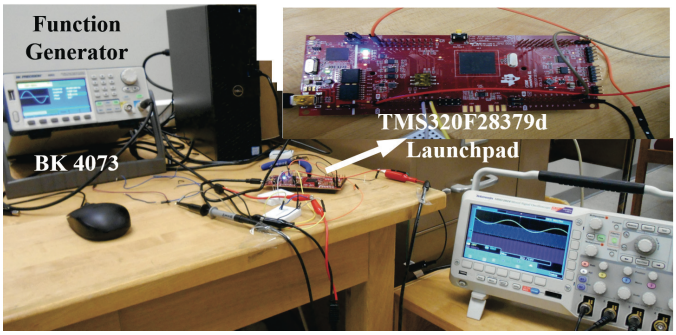


Fig. 7: Hardware setup used for experimentation with TMS320F28379D.

III. HARDWARE IMPLEMENTATION ON TMS320F28379D

The model presented in Fig. 3 is implemented in real-time with the help of Texas Instruments MCU TMS320F28379D Launchpad. The TMS320F2837xD is a powerful 32-bit floating-point microcontroller unit (MCU). To program the TI MCU, MATLAB's Embedded coder along with the Texas Instruments support package was used [12]. The input voltage is provided with an external function generator (BK 4078), to ADC A2 (pin 29). The voltage magnitude is 1 Vpp with a DC offset of 0.5 V. The output is observed using the two DACs on board, DAC-A and DAC-B. The clock frequency of the TI MCU is set as 200 MHz. The hardware setup is presented in Fig. 7.

A single phase to ground was introduced in Phase A, and the results are observed on oscilloscope. Fig. 8 presents the real-time results. The parameters used for the real-time studies are listed in Table. I. The results are similar to the waveform obtained in the simulation studies.

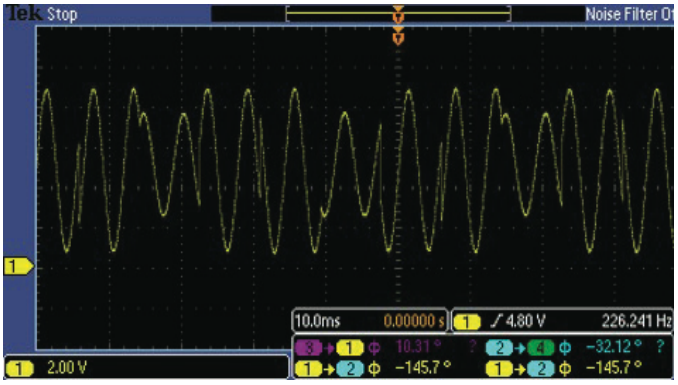
IV. SLIDING DFT IMPLEMENTATION ON TMS320F28335D

Another powerful TI MCU was used to implement Discrete Fourier transform (DFT) algorithm. TM320F28335 is used to implement sliding DFT algorithm. The purpose of doing this work is to study the harmonics of a power signal. For implementation of the segmented DFT, C code was written in Code Composer Studio, and then programmed on the TI MCU. The signal is generated within the MCU of 200 points. The frequency of the signal is 60 Hz. The signal is defined as:

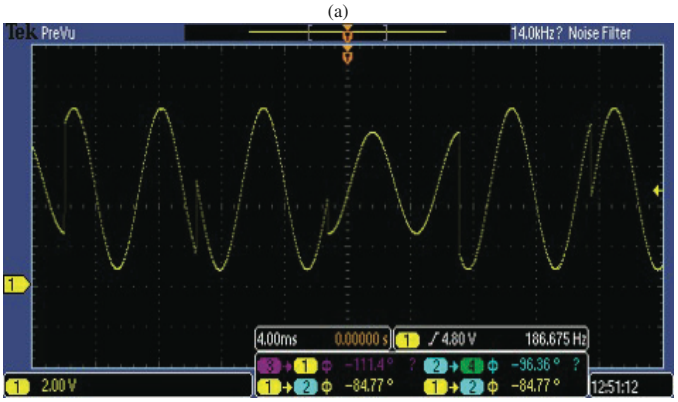
$$y[n] = a_1 \sin(\omega n dt) + a_3 \sin(3\omega n dt) \quad (1)$$

Here, a_1 is amplitude of the fundamental component, a_3 for the third harmonics, ω is the fundamental frequency (377 rad/s), and dt is the sample rate of 1/600 s. The value of a_1 and a_3 are changed accordingly to provide variety of cases, for example for the first 60 points a_1 = 1, and a_3 = 0.

Now, the segmented DFT is performed on the signal $y[n]$. The algorithm considers 4 segments of 50 points each to extract magnitude and phase information. The values for the magnitude of the DFT are stored. The results are presented in



(a)



(b)

Fig. 8: Output voltage across the load voltage observed with single line to ground fault. (b) Is a zoomed in version of (a).

Fig. 9. This work is still in process and in the future works, an external signal will be used to perform the sliding DFT and perform the fault analysis.

V. DISTANCE ESTIMATION FOR LG FAULT

Consider the LG fault model of Fig. 10. For the following analysis, the two voltages shown may be represented by their phasors. We then write the following matrix-vector equation:

$$\begin{bmatrix} \alpha Z + Z_f & -Z_f \\ -Z_f & Z_f + (1-\alpha)Z + Z_L \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ 0 \end{bmatrix} \quad (2)$$

Solving for I_2 yields an expression in the form:

$$I_2 = (\text{Second order polynomial in } \alpha)\, V_1 \quad (3)$$

This can be re-arranged as follows:

$$\alpha^2 - 2bc - c = 0 \quad (4)$$

The solution to (4) is as follows:

$$\alpha = b \pm \sqrt{b^2 + c} \quad (5)$$

In (5), only one of the signs will be valid; which one, that will generally be quite apparent. The location of the fault, or equivalently its distance from the source generator is (αD). A simple example follows. Consider that V_1 = 2, α = 0.5, and that at the test frequency, also Z=1 + j, Z_f=1 and Z_L = 1 − j. Then,

$$I_2 = \frac{V_1}{-(1+j)^2\alpha^2 + 2(1+j)\alpha + 2} \quad (6)$$

For α = 0.2, and V_1 = 2:

$$I_2 = \frac{2}{0.5j + 3} \quad (7)$$

In reality this will be measured or observed value but now we will use the RHS of (7) in the estimation step below. Now, (8) is re-written as:

$$I_2 = \frac{2}{\alpha'^2 + 2\alpha' + 2} \quad (8)$$

where, α' = $(1+j)\alpha$. Now using the RHS of (8), we obtain

$$\alpha' = 1 \pm \sqrt{1 + (2 - 0.5j + 3)} \quad (9)$$

Solving (9), α' = 0.5.

VI. VLSI ARCHITECTURE

One of the most powerful methods to study asymmetrical faults is the "method of symmetrical components". This method converts three phase quantities to positive, negative and zero sequence components. The relation between the two is presented below:

$$\begin{bmatrix} {V_a}^{(2)} \\ {V_a}^{(1)} \\ {V_a}^{(0)} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (10)$$

Here, V_a, V_b and V_c are the voltage phasors for phase A, B and C, α = $1\underline{/120°}$. Va0, Va1 and Va2 are the positive, negative and zero sequence components for phase A. Equation (10) can be mapped using MA_PLUS and UNL cell. The MA_PLUS (Fig. 11) cell has been developed to implement computation-intensive algorithms [13]. The UNL cell is highly efficient, multi-function, and reduced cycle, hardware implementation of nonlinear functions for application to sensor systems, wireless communications, and other DSP algorithms.

Re-writing equation (10), and just considering the real part of the equation.

Please note, only a small part of the mapping is shown (mapping of V_a(2) and V_a(1)). From Fig. 12, V = [V_a, V_b, V_c], and "y" is the output from the MA_PLUS cell and "SEL" is the select line. Similarly, the imaginary part of equation (10) can be obtained.

$$\text{Real}\begin{bmatrix} {V_a}^{(2)} \\ {V_a}^{(1)} \\ {V_a}^{(0)} \end{bmatrix} = \text{Real}\begin{bmatrix} a_3 & a_4 & a_5 \\ a_0 & a_1 & a_2 \\ a_6 & a_7 & a_8 \end{bmatrix} \text{Real}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (11)$$

Re-arranging (11)

$$\begin{aligned} V_a^{(1)} &= a_0 V_a + a_1 V_b + a_2 V_c \\ V_a^{(2)} &= a_3 V_a + a_4 V_b + a_5 V_c \end{aligned} \quad (12)$$

Timing table for Fig. 12 is presented in Table III.

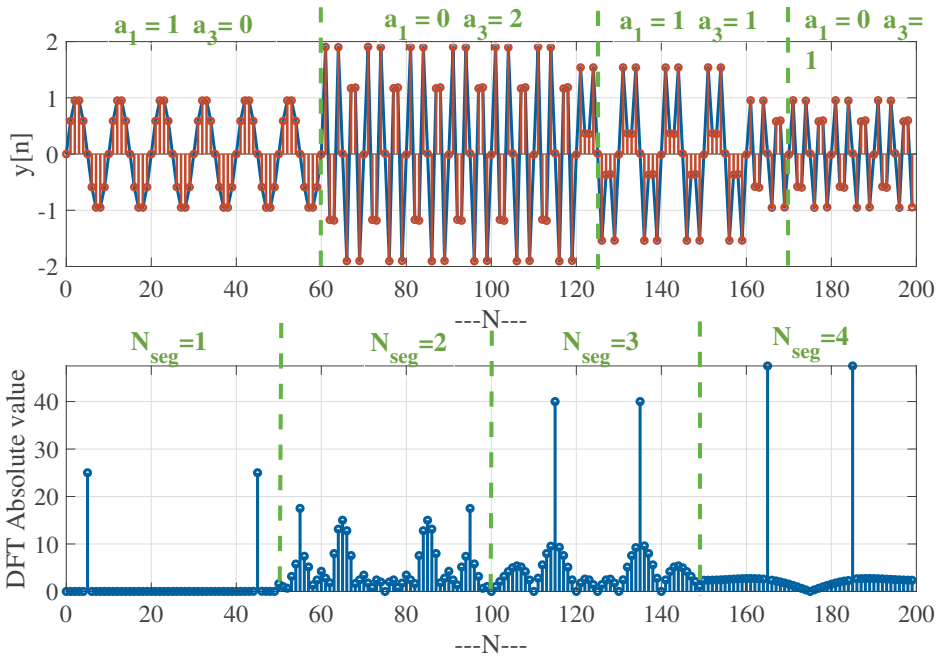


Fig. 9: Results of sliding DFT obtained from TMS320F28335 MCU. The above plot is $y[n]$ and the bottom is the DFT's absolute value.

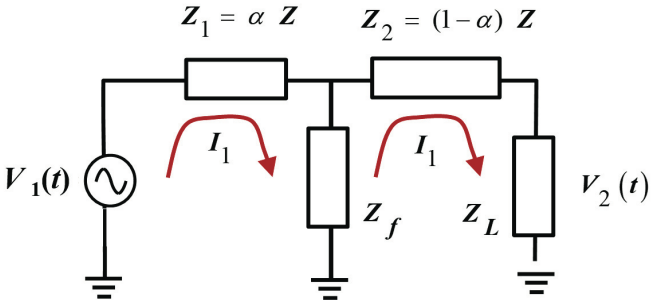


Fig. 10: Model for an LG fault.

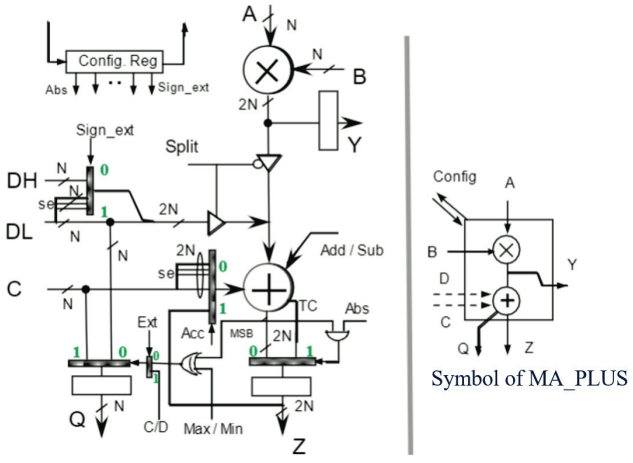


Fig. 11: MA_PLUS Cell core and its symbol.

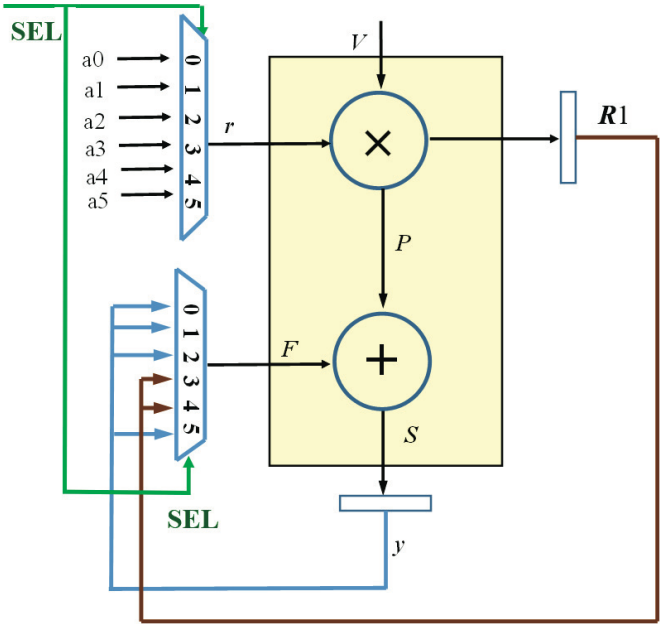


Fig. 12: MA_PLUS cell to obtain real part of $V_a^{(1)}$ and $V_a^{(2)}$.

VII. Conclusion and Future Work

This paper has presented a way to monitor three phases on a single output line from a DSP micro-controller. A second DSP microcontroller was used to perform sliding DFT method, which can be helpful to study harmonics in the system. These DSP micro controllers are very useful in the power grid area, since they are easy to implement and are powerful processing machines. In the power grid fault analysis is a very important

TABLE III: Timing Table for mapping (12) with the help of MA_PLUS.

A	B	C	D	E	F	G	H	I
1	V	V_a	V_b	V_c	V_a	V_b	V_c	V_a
2	r	a_0	a_1	a_2	a_3	a_4	a_5	a_0
3	**SEL**	0	1	2	3	4	5	0
4	P	a_0V_a	a_1V_b	a_2V_c	a_3V_a	a_4aV_b	a_5V_c	a_0V_a
5	S	a_0V_a	a_1V_b+a_0V_a	$V_a^{(1)}$	$a_3V_a + a_2V_c$	$a_4V_b + a_3V_a$	$V_a^{(2)}$	$a_0V_a + a_3V_a + a_4V_b + a_4V_c$
6	Y	0	a_0V_a	$a_1V_b + a_0V_a$	$V_a^{(1)}$	$a_3V_a + a_3V_c$	$a_4V_b + a_3V_a$	$V_a^{(2)}$
7	$R1$	0	a_0V_a	a_1V_b	a_2V_c	a_3V_a	a_4V_b	a_5V_c
8	F	0	a_0V_a	$a_1V_b + a_0V_a$	a_2V_c	a_3V_a	$a_4V_b + a_3V_a$	$a_3V_a + a_4V_b + a_5V_c$

area, hence a fault distance detection methodology was also presented in this article. VLSI architecture was also explored in this paper. In power grids, especially smart grids, VLSI architectures are being used for intelligent smart sensors. The advantage of such VLSI architectures is that they can provide reliable sensing for control and analysis in the modern power grids. In this paper one such VLSI architecture is discussed to obtain the symmetrical components from three phase voltage signals. The symmetrical components are an important tool to study various kinds of faults in a power grid. Future work includes, development of 3D-SoC chips for microgrids (sensing and control), and mutual inductance estimation using SoC between transmission lines.

ACKNOWLEDGMENT

This work was supported in part by National Science Foundation Grant No. 1807974.

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