Number of Turns Optimization for On-Chip Power Inductor Using a 3-D Physical Model

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***Abstract*—High inductance-density with high saturation current on-chip integrated power inductors support achieving high-density integrated power conversion. To guide the design of on-chip planar power inductor, a 3-D physical model in ANSYS®/Maxwell® is developed and utilized in this paper to evaluate the effect of copper winding number of turns on two of the main power inductor performance metrics, namely the inductance value/density and the saturation current. The tradeoff between the inductance value/density and the saturation current as a function of the copper winding number of turns is evaluated using the presented physical model.**

Keywords— Inductance, power inductor, saturation current, physical model, turns, number of turns, 3-D model, simulation, power electronics, magnetic, miniaturization, modeling , ferrite, on-chip.

I. INTRODUCTION

The demand for high-performance and high-density switching power conversion is increasing in a wide range of applications such as portable electronics, energy storage and battery management systems, and electric vehicles [1-14]. Switching power electronic converters and inverters utilize magnetic components such as transformers and inductors. Generally, power inductor accounts for a large portion of the entire device/circuit size and/or volume. Therefore, with the increasing need for miniaturized power conversion, power inductor miniaturization while maintaining high performance and efficient power conversion is increasingly becoming important. On-chip and planar integrated power inductors are a promising solution to miniaturize the power conversion circuit and to realize power system in package (PSiP) and power system on chip (PSoC) [7, 9, 11, 15-17].

Both inductance value and saturation current value depend on multiple design parameters that need to be optimized to achieve a target inductor design performance metrics for a certain application. Design parameters include, but are not limited to, copper winding number of turns, air gap between copper winding and ferrite cores, ferrite core permeability, and copper winding and ferrite cores footprints and thicknesses. Utilizing magnetic ferrite materials results in improving the inductance value compared with air-core inductor [3, 18-20]. However, this comes at the expense of lowering saturation current. Achieving larger saturation current values requires using a larger size of ferrite layers [5].

To optimize the parameters and guide the design for on-chip power inductor, 3-D physical modeling and simulation can be utilized. In this paper, the effect of number of winding turns on the inductance value or density and saturation current (two performance metrics) for a planar-structured on-chip power inductor is investigated. To guide the design, a 3-D physical model in ANSYS®/Maxwell® is developed. The tradeoff between inductance value and saturation current for a given power inductor footprint and volume as a function of the copper winding number of turns is evaluated. The 3-D physical model can be also utilized to visualize the flux density distribution for various inductor designs (i.e., with different number of turns and at different current values).

Section II presents the on-chip power inductor structure and specifications. Simulation results for on-chip power inductor with different number of turns are presented and discussed in Section III. The conclusion is given in Section IV.

II. ON-CHIP POWER INDUCTOR STRUCTIRE, MATERIAL AND SPECIFICATIONS

The on-chip power inductor design considered in this paper has three main different layers (integrated on a silicon wafer), namely, bottom ferrite core layer, copper winding layer, and top ferrite core layer. The structure for the on-chip power inductor is illustrated in Fig. 1. As shown, a planar structure is considered for the copper winding. In this structure, the copper winding is sandwiched between a top ferrite core layer and a bottom ferrite core layer. Fig. 1(b) illustrates how the layers are placed to construct the planar on-chip integrated power inductor. Fig. 1 (c) illustrates how an on-chip power inductor is integrated in a switching power converter (mainly includes the power inductor, capacitor, two MOSFETs, controller, and MOSFET gate driver) on Si substrate layer.

The ferrite material considered for the on-chip power inductor design is Ni-Zn type that has a permeability μ of 100 and a saturation flux density B_s of 0.28 T. The ferrite material specifications (permeability and saturation flux density) are based on the fabrication results presented in [21]. The air gap between the top ferrite core and copper winding (top air gap in Fig. 1b) and the air gap between the bottom ferrite core and the copper winding (bottom air gap in Fig. 1b) are set to be equal. An air gap value of 10 μm is used for both the top air gap and the bottom air gap. The effect of using different values for the top and bottom air gaps is investigated in [22]. Table I summarizes the specifications for the on-chip power inductor design.

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TABLE I
Planar on-chip integrated power inductor design specifications

Layer	Specifications	
Top and bottom ferrite cores	Material	Ni-Zn
	Permeability μ	100 [21]
	Saturation flux density Bs	0.28 T [21]
	Dimensions (Length × Width × Thickness)	5.2 mm × 5.2mm × 0. 525 mm
	Air gap with copper winding	10 μm
Copper winding	Outer dimensions (Length × Width)	5.2 mm × 5.2mm
	Thickness	100 μm
	Number of turns	Varies (see Table II)
	Winding width	Varies (see Table II)
	Winding gap	Varies (see Table II)

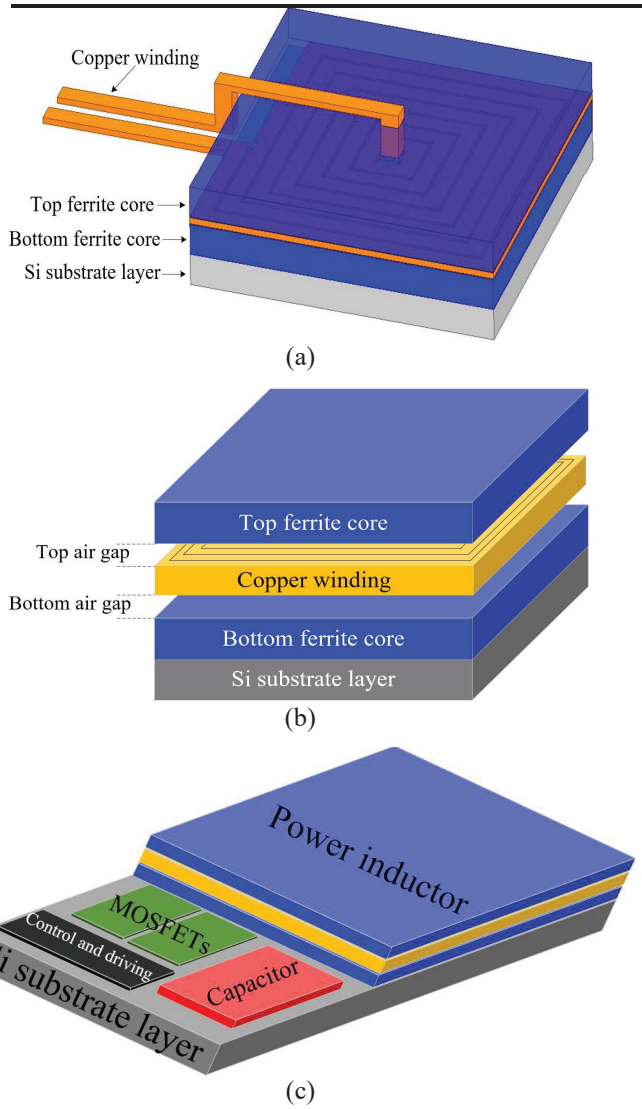

Fig. 1. On-chip integrated power inductor structure. (a) assembled inductor (b) layer placement (c) illustration for on-chip power inductor in a switching power converter (not to scale).

TABLE II
Copper winding specifications

Number of turns	Winding width (mm)	Winding gap (mm)
3	0.7	0.05
5	0.4	0.08
7	0.3	0.05
10	0.2	0.05

The specifications for the copper winding are summarized in Table II. The saturation current and inductance value are investigated at different values for the number of copper winding turns (3 turns, 5 turns, 7 turns, and 10 turns). In Table II, the winding gap represents the distance between the copper winding turns. The copper winding width and gap are adjusted such that the footprint area covered by the copper winding is almost equal to the desired footprint area of the device and the top and bottom ferrite cores.

III. 3-D Physical Model Simualtion Results of the On-Chip Power Inductor

Based on the specifications listed in Table I and Table II for the power inductor, a 3-D physical model in Ansys ®/Maxwell® is developed and utilized to investigate the effect of winding number of turns on the inductance value and the saturation current in order to guide the design. The inductance value and the saturation current value are obtained for the on-chip power inductor for different values of number of turns. The simulation results are summarized in Table III. The overall inductor dimensions are 5.2 mm (length) × 5.2 mm (width) × 1.17 mm (height). This means that the inductor cross sectional area and volume are 27.04 mm^2 and 31.64 mm^3, respectively. Based on the obtained inductance values, the inductance area density (H/m^2) and volume density (H/m^3) are calculated and summarized in Table III. The results in Table III show how the inductance value is proportional to the number of turns for this power inductor design.

TABLE III
Simulation results for on-chip power inductor with different number of turns

Number of turns	Inductance	Inductance density nH/mm^2	nH/mm^3	Saturation current (A)
3	221.6 nH	8.20	7.00	14
5	524.8 nH	19.41	16.59	9
7	949.46 nH	35.11	30.01	7
10	1.85 μH	68.42	58.47	5

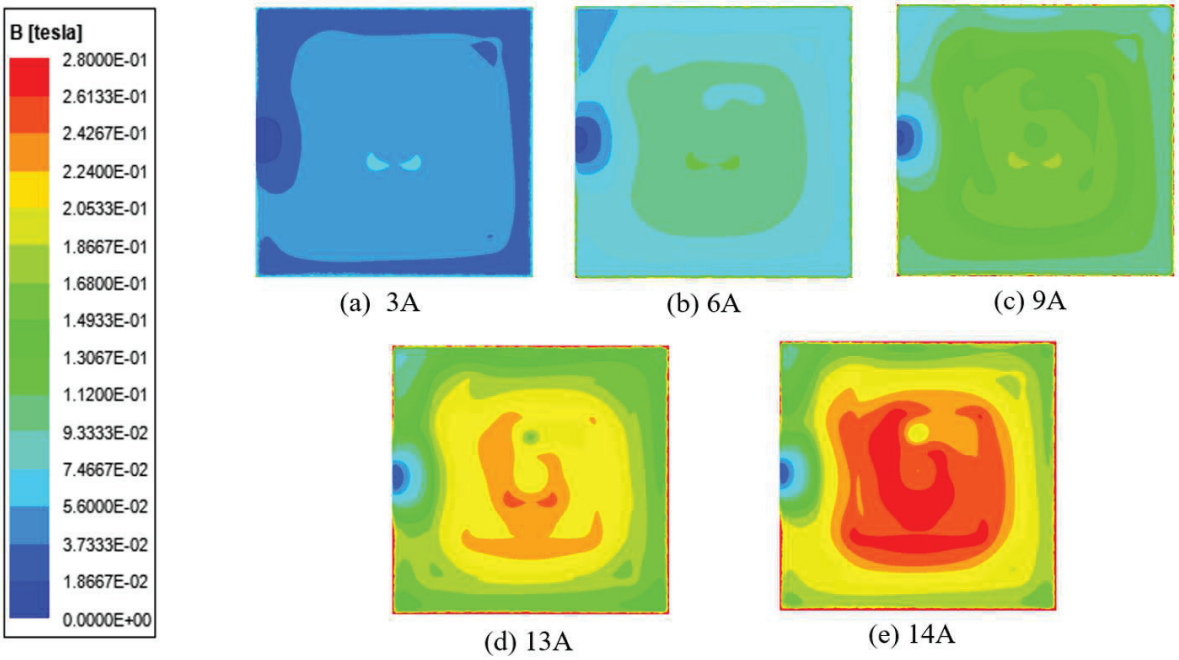

Fig. 2. Flux density *B* distribution of the bottom ferrite core layer for 3-turn on-chip power inductor under different DC input current values (a) 3A, (b) 6A, (c) 9A, (d) 13A, and (e) 14A.

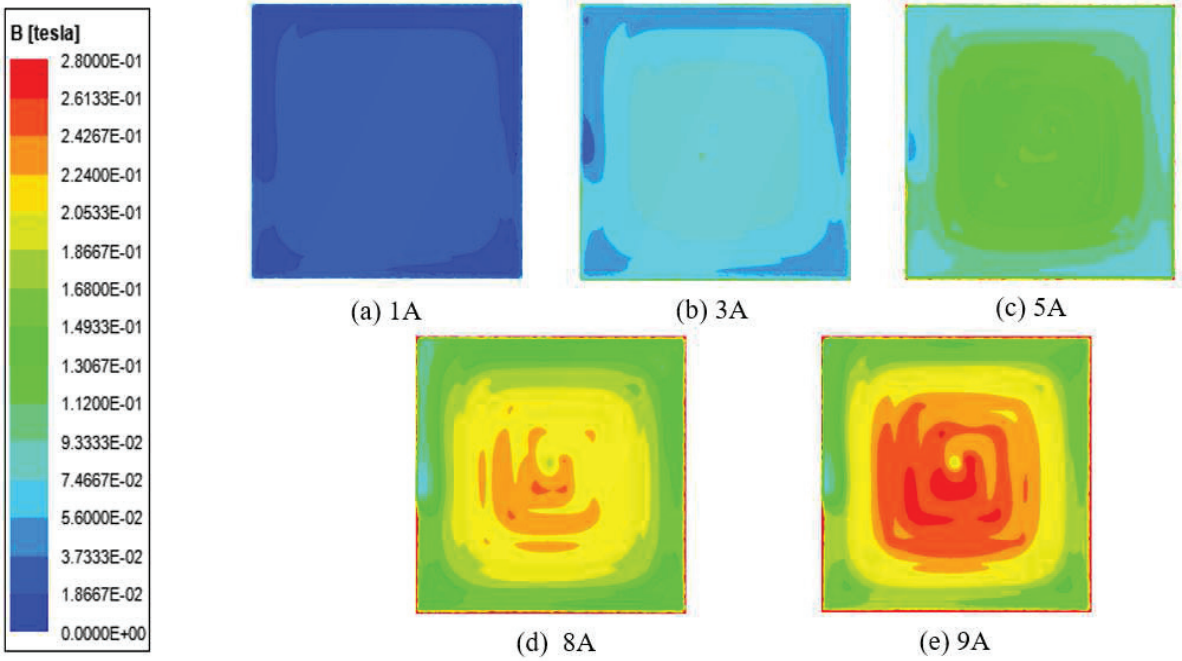

Fig. 3. Flux density *B* distribution of the bottom ferrite core layer for 5-turn on-chip power inductor under different DC input current values (a) 1A, (b) 3A, (c) 5A, (d) 8A, and (e) 9A.

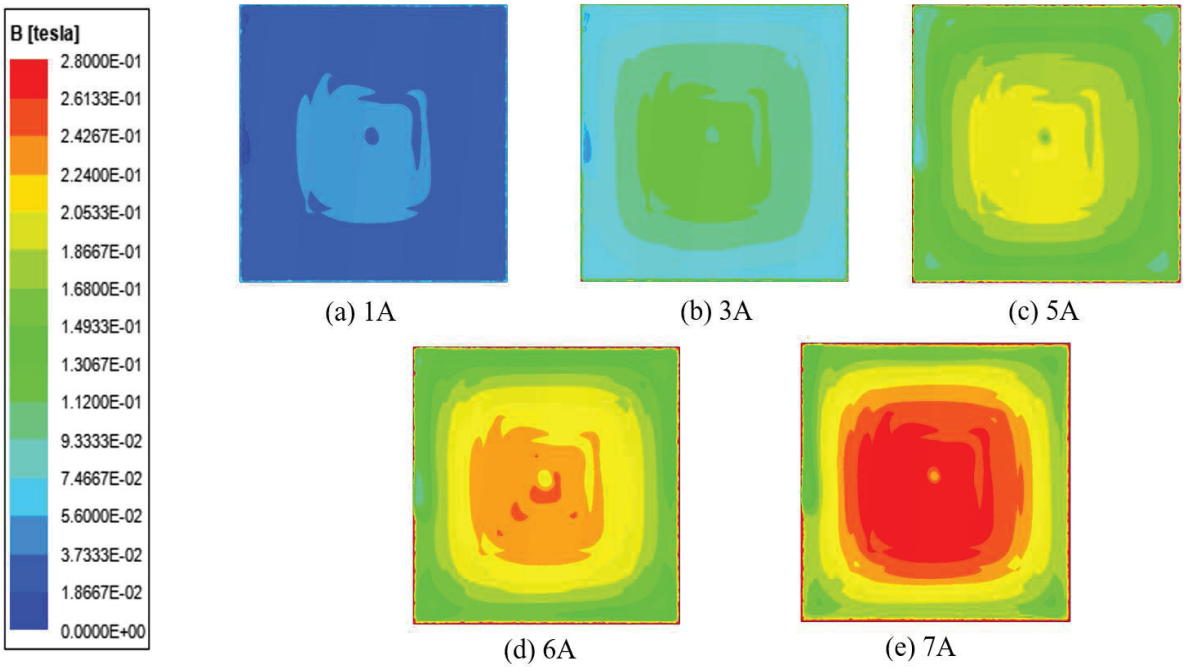

Fig. 4. Flux density *B* distribution of the bottom ferrite core layer for 7-turn on-chip power inductor under different DC input current values (a) 1A, (b) 3A, (c) 5A, (d) 6A, and (e) 7A.

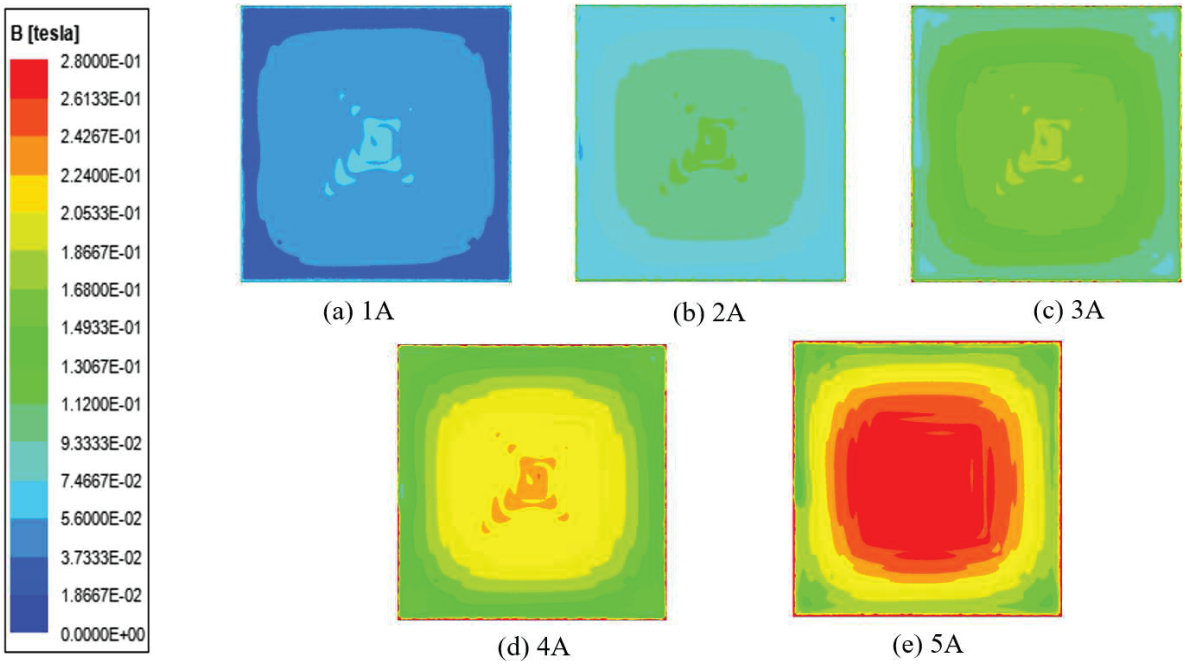

Fig. 5. Flux density *B* distribution of the bottom ferrite core layer for 10-turn on-chip power inductor under different DC input current values (a) 1A, (b) 2A, (c) 3A, (d) 4A, and (e) 5A.

The bottom layer's flux density *B* distributions for different number of turns are shown in in Fig. 2, Fig. 3, Fig. 4, and Fig. 5. Form Fig. 2 through Fig. 5, the flux density *B* of the bottom ferrite layer increases as the number of copper winding turns is increased. In Fig. 3 (e), for example, the red part indicates that the bottom ferrite is saturated at 9 A. In other words, the flux density reached the saturation value of 0.28 T. This also means that the corresponding inductor winding current (9 A) is the saturation current when the number of turns is equal to 5. In other words, the inductor's winding current is increased until the flux density is equal to 0.28 T to estimate the saturation current. The same procedure can be followed to obtain the saturation current for the inductor with different number of turns. From Fig. 2 to Fig. 5, the saturation current values are 14 A for 3 turns, 9 A for 5 turns, 7 A for 7 turns, and 5 A for 10 turns. Based on the obtained values for the inductance and the saturation current values, a tradeoff between the inductance value and the saturation current can be made when fabricating the complete

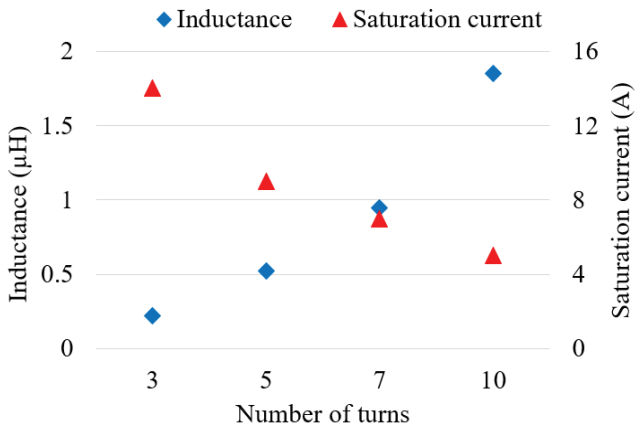

Fig. 6. Tradeoff between inductance value and saturation current value at different numbers of inductor winding turns.

device. The higher the number of turns is, the higher is the inductance value (and hence the higher are the inductance area and volume densities), and the lower is the saturation current. Fig. 6 illustrates this tradeoff using the results obtained from the simulation.

IV. Conclusion

On-chip physical modeling and simulation can be utilized to guide the design and optimize the on-chip power inductor parameters prior to the fabrication process. In this paper, the effect of number of turns of an on-chip power inductor on the inductance value and saturation current value is studied using 3-D physical model in Ansys®/Maxwell®. The tradeoff between the inductance value and the saturation current as a function of number of turns is evaluated.

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