

# Experimental End-To-End Delay Analysis of LTE Cat-M With High-Rate Synchrophasor Communications

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**Abstract**—Micro-phasor measurement units ( $\mu$ -PMUs) are devices that permit monitoring voltage and current in the distribution grid with high accuracy, thus enabling a wide range of smart grid applications, such as state estimation, protection, and control. These devices need to transmit the synchronous measurements of voltage and current, also known as synchrophasors, to the power utility control center at a high rate. The use of wireless networks, such as LTE, to transmit synchrophasor data is becoming increasingly popular. However, synchrophasors are included in small frames and it would be more efficient to use low-power cellular solutions such as LTE cat-M. In this work, we present experimental research on the deployment of a  $\mu$ -PMU with the ability to connect over a commercial LTE cat-M network. The deployed  $\mu$ -PMU is built with off-the-shelf hardware, such as Arduino microcontrollers, and is used to transmit data—compliant with the IEEE C37.118.2 standard—at a variable rate from 1 to 80 frames/s. A detailed network performance analysis is carried out to show the suitability of LTE cat-M to support  $\mu$ -PMU communications. Experimental results on performance indicators, such as delay and jitter, are reported. The effect of the LTE cat-M access mechanism on the time distribution of frame arrivals is also thoroughly analyzed.

**Index Terms**—Internet of Things (IoT), LTE cat-M, micro-phasor measurement unit (PMU), smart grid, synchrophasor.

## I. INTRODUCTION

**P**HASOR measurement units (PMUs) have traditionally been used to monitor the power grid and represent one of the major drivers in the transition from the old centralized power grid into the modern, diverse, and distributed smart grid. These devices permit the computation of the so-called *synchrophasors*, which are *time-synchronized* estimations of the magnitude and phase of voltage and/or current waveforms. PMUs also measure other quantities, such as frequency and rate of change of frequency (ROCOF), and are able to provide estimates of active and reactive power [1]. PMU data are extremely time sensitive and their transmission is mainly regulated by two sets of standard procedures, namely, IEC 61850 [2] and IEEE C37.118.2 [3]. Synchrophasor data are

employed in a number of smart grid applications, which mainly differ in the reporting rate and in the communication requirements, such as delay and frame error rate. A thorough overview of the most common PMU applications along with their reporting and communication requirements is provided in [4], where applications are categorized based on the required time resolution and latency. Latency spans across a wide range of values: for example, protection, and control applications require a maximum latency in the order of a few ms, whereas other applications, such as state estimation or outage management, can tolerate network delays in the order of 1 s. Traditional PMUs, mainly used in the transmission grid [5], provided a total vector error (TVE) precision of  $\pm 0.01\%$ , a phase angle accuracy of  $\pm 0.003^\circ$ , a magnitude resolution of  $\pm 0.0002\%$ , and an angle resolution of  $\pm 0.001^\circ$  with around 120 frames per second [6].

In recent years, a need for higher precision measurements in the distribution systems and microgrids entailed the deployment of a new type of synchrophasor measurement device, i.e., the micro-PMU (or  $\mu$ -PMU). This type of device is characterized by a TVE precision of  $\pm 0.05\%$ , a phase angle accuracy of  $\pm 0.001^\circ$ , a magnitude resolution of  $\pm 0.0002\%$ , and an angle resolution of  $\pm 0.002^\circ$  with up to 100-120 frames per second [7]. In the last decade, with the increased use of distributed generation elements, such as photovoltaic and wind farms,  $\mu$ -PMUs have proliferated and need to be connected to the power grid in order to collect their synchrophasor data. PMUs and  $\mu$ -PMU are connected to phasor data concentrator (PDC), which are in charge of collecting synchrophasors from several PMUs, aligning them, and then forwarding them to the power utility [1]. Traditionally, wired connectivity, such as Ethernet or power line communications (PLCs), have been preferred due to their high performance and low delay. However, in recent years, wireless networks are becoming an increasingly popular solution to connect  $\mu$ -PMUs to the Internet thanks to their flexibility, ease of installation, and scalability. Previous work on wireless networks for PMUs or  $\mu$ -PMUs has predominantly focused on cellular technologies, such as WiMax, UMTS [8], and LTE [9], [10]. However, the coverage of WiMax is not extensively available, consequently undermining large-scale  $\mu$ -PMU deployments. On the other hand, UMTS and LTE, despite providing a quasi-ubiquitous coverage, were conceived to support human traffic, which is considerably different from  $\mu$ -PMU traffic [11]. One basic difference lies in the size of the synchrophasor frames, which are in the order of a few tens of Bytes, as opposed to the

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larger data commonly exchanged in human traffic, such as video streaming or Web surfing. As a result, the large resources required for LTE transmission, in terms of bandwidth and energy, would not be efficiently used to transmit  $\mu$ -PMU data.

Therefore, in this work, we are proposing to wirelessly connect  $\mu$ -PMUs using LTE cat-M, one of the so-called Cellular-Internet of Things (C-IoT) technologies [12]. This LTE-based technology is characterized by a limited use of the frequency spectrum and a lower cost, both in terms of hardware (LTE cat-M radios are cheaper than standard LTE radios) and in terms of data plans, which are cheaper with respect to other cellular networks. In order to test the suitability of LTE cat-M to transmit synchrophasor data, we deployed a  $\mu$ -PMU using Arduino microcontroller boards and a GPS module. This prototype of  $\mu$ -PMU is connected to an AC power signal generator, samples the power signal, generates synchrophasor frames (compliant with the IEEE C37.118.2 standard), and transmits them to a laptop, which represents the PDC, using a commercial LTE cat-M network in the U.S.. To the best of our knowledge, this is the first study to propose using LTE cat-M for  $\mu$ -PMU communications.

The main contributions of this article are: 1) the development of a low-cost low-complexity prototype of a  $\mu$ -PMU with LTE-M transmission capability; 2) the characterization of frames and transmission rates compliant to the IEEE C37.118.2 standard; and 3) experimental analysis of end-to-end delay of LTE cat-M for synchrophasor communications. The remainder of this article is structured as follows. In Section II, an overview of the state of the art is presented. In Section III, the proposed system modeling is described and numerical results are reported in Section IV. Finally, the conclusions of this research are discussed in Section V.

## II. STATE OF THE ART

The pervasive installation of distributed energy resources (DERs) into power distribution systems along with the popularity of demand-response initiatives have led distribution networks to work outside their operational limits. To cope with the more stringent requirements on these systems, recent trends show that improvements in the distribution system management are preferred over network capacity increase [13]. PMUs and  $\mu$ -PMUs are key elements to increase the observability and enhance metering in distribution networks [14]. These devices are expected to bring about substantial improvements in power systems in terms of reliability, security, and overall performance [14].

There is a great deal of literature analyzing the positive effect of synchrophasor devices on the performance of distribution systems [15], [16], [17], [18], [19]. In particular, Mohsenian-Rad et al. [15] provided examples to demonstrate the importance of using PMUs and  $\mu$ -PMUs in the distribution grid. They showed, in one of these examples, how to use data from multiple PMUs to identify a short-circuit fault event, therefore allowing quick deployment of field crews at the fault location. They also advocated the importance of developing predictive analytics based on machine-learning and big data techniques [15]. Chai et al. [16] proposed to

use PMUs to enable real-time state estimation. To cope with the lack of a solid and steady communication infrastructure, the authors introduced C-DAX, a communication platform based on the information-centric networking theory. C-DAX employs a combination of PLC and optical fiber to support synchrophasor communications [16]. A real-time monitoring infrastructure was also proposed by Pignati et al. [18], based on a hierarchical architecture with Ethernet, single-pair high-speed digital subscriber line, and optical fiber. The proposed system was deployed on the EPFL campus and an average end-to-end latency of 65 ms was obtained. A similar hierarchical architecture was considered in [19] with a combination of wired and wireless technology. Wireless links were emulated using the well-known EMANE platform.<sup>1</sup>

The use of wireless networks to support synchrophasor communications has become increasingly popular in recent years [9], [10], [20], [21], [22], [23]. In [20], it was proposed to use WiMax technology for the wide-area PMU communications. The authors employed existing network simulation software (i.e., OPNET) in order to evaluate different scheduling services in a network with a maximum of 50 PMUs, a reporting rate of 25 frames/s, and a maximum application delay of 40 ms. Network simulation for PMU communications was also performed in [10], where the authors considered a smart-city environment with a realistic LTE cellular infrastructure. The employed network simulator,<sup>2</sup> permitted considering up to 21 PMUs and 25 thousand PMUs along with traffic generated from more than 300 thousand smart meters; however, human traffic was not considered [24], [25]. A more realistic study with LTE was carried out in [9], where Dervivskadic et al. used a commercial LTE network to support data transmission from 10 PMUs. The authors analyzed the total PDC reporting latency with four different logics and then compared the experimental LTE results against a wired network benchmark with optical fiber.

Even though the latest generations of wireless networks provide promising results, the variability of wireless transmissions entails the possibility of dropping frames or unpredictable degradation of the performance, leading to large delays and potentially compromising the success of the considered power system applications. In order to cope with this effect, Pourramezan et al. [21] proposed a statistical method to compensate for bad communication data. Pourramezan et al. [23] later proposed a novel method to coordinate different PDCs to mitigate the variability of data transmitted by different PMUs over a commercial LTE network. Zhu and Lin [26] proposed to use spatial-temporal correlations of PMUs data to fix missing measurements and abnormal values.

LTE cat-M was originally introduced by 3GPP in Release 13 with a reduced bandwidth with respect to legacy LTE, coverage enhancement modes, support for half-duplex communications, and power reduction techniques, such as enhanced discontinuous reception. It was later improved with mobility enhancements (Rel. 14), improved spectral efficiency

<sup>1</sup>Networks and Communication Systems Branch: EMANE. Available: <http://cs.itd.nrl.navy.mil/work/emane/index.php>.

<sup>2</sup>Available at [www.trafficm2modelling.com](http://www.trafficm2modelling.com).

TABLE I  
COMPARISON OF EXPERIMENTAL PMU IMPLEMENTATIONS

| PMU Name                  | GridTrak PMU [27]        | OpenPMU V1 [28] | OpenPMU V2 [28] | Mohapatra [29] | Our Design           |
|---------------------------|--------------------------|-----------------|-----------------|----------------|----------------------|
| Approx. cost              | 150\$                    | 400\$           | 100\$           | 500\$          | 150\$                |
| Hardware                  | dsPIC30F microcontroller | NI DAQ          | BeagleBone B.   | Arduino Due    | Arduino Mega         |
| Software                  | C#                       | LabView         | Linux           | Linux, Python  | Python               |
| Open-Source               | Yes                      | No              | Yes             | Yes            | Yes                  |
| IEEE C37.118.2 Compliance | Yes                      | Yes             | Yes             | No             | Yes                  |
| Communication             | Wired                    | Wired           | Wired           | Wired          | Wireless (LTE cat-M) |

(Rel. 15), and ultralow-power wake-up radio operation to extend User Equipment (UE) battery life (Rel. 16). The performance of LTE cat-M has been investigated by a large body of [30], [31], [32], [33], [34], and [35]. In particular, Elsaadany et al. [30] presented an overview of the features and challenges of cellular networks for Internet of Things (IoT) applications, focusing on the characteristics of the physical layer of LTE cat-M and exploring the pros and cons of this technology compared to available alternatives, such as LTE cat-0 and NB-IoT. Masek et al. [31], Ratasuk et al. [32], and Dawaliby et al. [35] used NS-3 to perform simulation at the network layer: Masek et al. [31] analyzed a large-scale scenario with 500 end devices, however no indication of the type of traffic generated by each device was provided; Ratasuk et al. [32] focused on the impact of network parameters, such as the number of repetitions, on the error rate, coverage, and battery life; Dawaliby et al. [35] proposed a comparison of network performance with LTE cat-0 and observed a larger achieved throughput, with lower delay, frame losses, and jitter with respect to LTE cat-0. Medina-Acosta et al. [34] evaluated the possibility of allocating fractions of resource blocks to UEs with small frames to transmit, as in the 5G massive machine-type communication scenario. An experimental study to analyze the coverage enhancement of LTE cat-M with respect to legacy LTE was proposed in [33]. Despite the realistic setup considered in this study, also complemented with simulation results using MATLAB, no information was provided on latency nor on the type of traffic generated by the UEs.

The deployment of PMU prototypes has already been investigated by a good deal of research and a comprehensive literature review can be found in [36]. A comparison of our work against some of the existing low-cost research-oriented PMU deployments is shown in Table I. In particular, Mohapatra [29] employed three micro-controllers for phasor measurement and reporting. The prototype also requires a wired external PC for data processing and visualization which decreases the feasibility of widespread deployment. Another example is the work done in the OpenPMU project [28] to create a low-cost open-source PMU. OpenPMU V1 uses national instrument hardware and LabView software which is proprietary and a huge impediment to deployment. This was remedied in OpenPMU V2 by the use of open-source hardware & software but the exact details of implementation

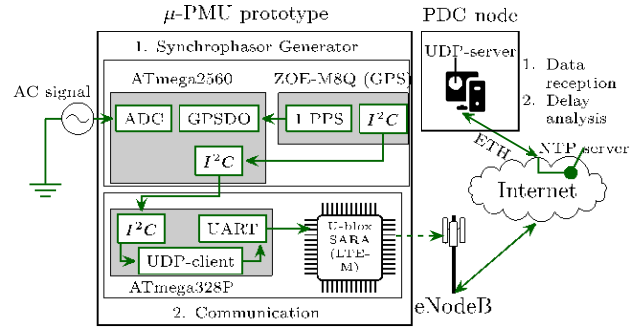


Fig. 1. Schematic of the deployed testbed.

and firmware are not available increasing the complexity of deployment. In the case of GridTrak PMU, presented in [27], two microcontrollers are used, one for Phasor generation and another for pulse per second (PPS) generation. It is a cost-effective alternative but the use of a custom PCB makes it challenging to implement where PCB making is not accessible. Differently from the existing literature, where wired technologies and protocols, such as Ethernet, were adopted for this work we deployed a low cost  $\mu$ -PMU with the ability to transmit data using LTE cat-M. Our modular design created with a prebuilt development board ensures compatibility and lower complexity.

### III. SYSTEM DESCRIPTION

The objectives of this study are to deploy a functional prototype of  $\mu$ -PMU with the ability to wirelessly transmit synchrophasor data to the PDC and to study the suitability of LTE cat-M to transmit synchrophasor frames. In order to achieve these features, our  $\mu$ -PMU consists of two main modules: 1) a synchrophasor generator module and 2) a communication module. The schematic of the system architecture is illustrated in Fig. 1, where the  $\mu$ -PMU prototype and the PDC node are enclosed in dashed boxes. The  $\mu$ -PMU box also contains two dotted boxes, which represent the two aforementioned modules. The PDC node is represented by a laptop connected to the Internet through an Ethernet cable. Our testbed also includes an AC signal generator (which can produce voltage signals with a 0–5 V amplitude and a frequency in the range 1–65534 Hz) and a commercial LTE

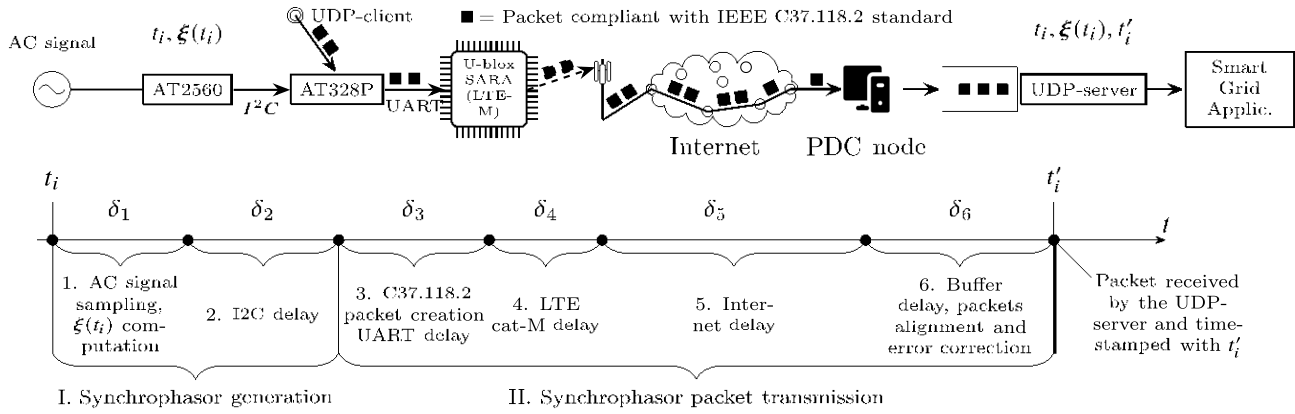


Fig. 2. Workflow of the creation of synchrophasor frames and their transmission with the testbed.

cat-M network with an eNodeB connected to the Internet.<sup>3</sup> In the remainder of this section, the system components are described in more detail.

#### A. Synchrophasor Generation Module

In order to test the creation and transmission of realistic synchrophasor data, we need an AC signal to be monitored and an accurate time source. An Arduino ATmega2560 is employed to get the instantaneous voltage values from the AC signal generator and compute the synchrophasors. We can generally indicate with  $\xi(t_i)$  the vector of synchrophasors measured at time  $t_i$ . In particular,  $\xi(t_i)$  includes the voltage magnitude  $v(t_i)$ , phase  $\phi(t_i)$ , frequency  $f(t_i)$ , and ROCOF  $\rho(t_i)$ . The system schematic for the synchrophasor generation module can be found in the upper portion of Fig. 1. The baseline version of ATmega2560 mounts a 10-bit analog to digital converter (ADC), which is used to sample the AC signals. The accuracy of the sampling timing is extremely important as any irregularity can undermine the successful computation of the power indicators in  $\xi(t_i)$ . The sampling is controlled by an interrupt service routine (ISR), which detects the rising edges of pulse-width modulation (PWM) signals. PWM signals are generated by a GPS digital oscillator (GPSDO), implemented within the ATmega2560. The main function of the GPSDO is to generate predefined, equidistant pulses synchronized with the detection of 1 PPS from the ZOE-M8Q GPS module by means of an ISR. Thus, a 1600 Hz PWM signal generated by the GPSDO will lead to a 1600 Hz sampling by the ADC, which is enough to run a 32-point discrete Fourier transform (DFT) on a 50 Hz signal. Different rates can be used to sample power signals at different nominal frequencies. For example, a frequency of 60 Hz would require a sampling rate of  $60 \cdot 32 = 1920$  Hz.

The GPS module, connected to the ATmega2560 over  $I^2C$  interface, is used to maintain accurate time synchronization. Fresh timing data is requested from the GPS at the start of every second, marked by the rising edge of the 1 PPS signal. The time between subsequent PPS peaks is calculated using internal timers of the micro-controller rendering accuracy of

<sup>3</sup>The core of the LTE cat-M network is not shown in Fig. 1, as it is not within the scope of this work.

$1 \mu\text{s}$  for time-stamping. The primary reason for limiting timing requests to once per second only is due to the hardware limitations of the GPS module. The timestamp of a given generated phasor  $\xi(t_i)$  is denoted by  $t_i$ .

As already indicated, a  $\mu\text{-PMU}$  must be able to measure the frequency  $f(t_i)$  and calculate the ROCOF  $\rho(t_i)$  of the AC signal. For that purpose, a sine-to-square wave converter circuit with a step-down transformer is implemented, similarly to what was done in [29]. The AC signal is fed into the circuit and the output is a square wave with voltage ranging from 0 to 3 V. Another ISR is used to keep track of the rising edges of the square wave to calculate the time difference between two consecutive rising edges, which represents the period  $T$  of the signal. The frequency  $f(t_i)$  is then calculated as the reciprocal of the period. The ROCOF  $\rho(t)$  was computed as  $[(f(t_i) - f_0) \cdot f_0]$ , as shown in [37].

A 32-point DFT is used for estimating the magnitude  $v(t)$  and phase  $\phi(t)$  of the AC signal. A 32-element buffer is updated as soon as a new sample is generated by the ADC, which is controlled by the PWM signal from the GPSDO. A counter keeps track of the number of samples and as soon as it reaches 32, DFT is run. The power signal sampling and the subsequent  $\xi(t_i)$  computation correspond to the first step of the *Synchrophasor generation* phase, displayed on the timeline in Fig. 2. The second step in this phase is represented by the transmission (using the  $I^2C$  interface) of synchrophasor  $\xi(t_i)$  to the ATmega328P, which is responsible for the wireless transmission to the PDC node.

#### B. Communication Module

Fig. 2 illustrates the workflow related to synchrophasor frames, represented here by black squares, from their creation in the ATmega328P device to their reception at the UDP server hosted in the PDC node, which is represented by a laptop connected to the Internet. In particular, in the upper portion of the figure, we have a system schematic with the different components included in the testbed: they appear from left to right according to their sequential use in the workflow. In the bottom part of Fig. 2, it is possible to observe a timeline representing the two main phases in the workflow: 1) synchrophasor generation and 2) synchrophasor frame transmission, and the six



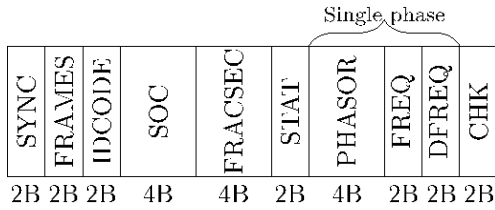


Fig. 3. Frame structure of a data frame in IEEE C37.118.2 [3].

required steps. The first two steps (included in Phase I) take place within the Arduino ATmega2560 and were extensively described in the previous section. In order to perform the third and fourth steps (i.e., frame creation and frame transmission, respectively), we have used an ATmega328P, which is connected to the ATmega2560 over  $I^2C$  interface. This interface between the synchrophasor generation module and the communication module is also visible in Fig. 1.

Once a synchrophasor  $\xi(t_i)$  is computed and timestamped with time  $t_i$ , the next step is to incorporate it in a frame, which corresponds to step 3 in Fig. 2. In this work, we are following the IEEE C37.118.2 standard [3], whose main structure is shown in Fig. 3: the frame size for a single phase system is 26 bytes and for a 3-phase system is 42 bytes. These values are related to a scenario with fixed 16-bit formats. Among the frame fields, it is worth highlighting: 1) the second of century (SOC) and fraction of second (FRACSEC), which represent the timestamp; 2) PHASORS, which includes the estimated magnitude and phase of the monitored AC signal; 3) FREQ, representing the operating frequency, and 4) DFREQ, which represents the ROCOF indicator. The last field CHK is a checksum used for burst error detection according to the cyclic redundancy check (CRC) technique [3]. Further details on the IEEE C37.118.2 frame structure can be found in [1] and [3].

As shown in Fig. 2, the transport protocol we used for the transmission of the synchrophasor frames is UDP, which assures low overhead and low latency communication as opposed to TCP, which is more suitable for reliable data transfers. A Python-based UDP client application was implemented in the ATmega328P to transmit synchrophasor frames and a Python-based UDP server was deployed at the PDC node to receive and collect these frames. Once synchrophasor frames are created, they are sent to the U-blox SARA module for transmission over LTE cat-M. Frame creation and transmission over UART interface to the network module correspond to step 3 in Fig. 2. The U-Blox SARA module is then used to transmit frames to the LTE cat-M eNodeB (step 4). Frames are then transmitted over the Internet (step 5) until reaching the PDC node, where they are realigned<sup>4</sup> and eventual errors are corrected using CRCs (step 6). Frames are finally received by the UDP server, which adds a timestamp (i.e.,  $t^0$ ). Received frames can be then used in a broad range of smart grid applications, as discussed in Section I. The timestamp  $t^0$  is used in the end-to-end delay analysis provided in the next section.

<sup>4</sup>With UDP, frames can be received out-of-order.

### C. End-to-End Delay and Data Analysis

Once frames are received by the UDP server, they can be used to evaluate network performance and analyze the synchrophasor data. One of the most important parameters to evaluate network performance (and assess the suitability of LTE cat-M for synchrophasor transmission) is the end-to-end delay, hereafter denoted as  $D(t_i)$ , which is defined as the time elapsed from  $t_i$ , when  $\xi(t_i)$  is generated to  $t_i^f$ , when  $\xi(t_i)$  is received. Therefore, we have that  $D(t_i) = t_i^f - t_i$ . In Fig. 2, it is shown that the reception time  $t_i^f$  is computed at the PDC, after the frame is correctly received by the UDP server. However, in order to have meaningful and consistent values for  $t_i$  and  $t_i^f$ , the two devices measuring them, i.e., ATmega2560 and the laptop, respectively, need to be accurately synchronized. In order to achieve high-precision synchronization, we used an NTP server, which is synchronized with the same GPS satellite used by our ZOE-M8Q GPS module.

As shown in Fig. 2,  $D(t_i)$  consists of the sum of the delays for each of the six steps, denoted by  $\delta_k$  with  $k = 1, \dots, 6$ : in particular,  $\delta_1$  represents the time needed to sample the power signal and compute  $\xi(t_i)$ ;  $\delta_2$  represents the time needed to transmit  $\xi(t_i)$  from the ATmega2560 to the ATmega328P over  $I^2C$  interface;  $\delta_3$  represents the time to create a frame and transmit it over the UART interface to the LTE cat-M card;  $\delta_4$  and  $\delta_5$  represent the network delay;  $\delta_6$  represents the buffer delay, i.e., the time needed to sort frames that are received at the PDC not in the correct order.

### D. Overview of LTE Cat-M Technology

The synchrophasors  $\xi(t_i)$ , generated according to the mechanisms described in Sections III-A and III-B, need to be transmitted over a wireless network. In light of a steep increase of distributed generation elements to be integrated into the power distribution grid, a cheap and easy-to-install cellular IoT network is a good candidate to support this kind of high-rate and small-size communications. The main alternatives in the cellular IoT technologies are LTE cat-M and NB-IoT [41], [42]. Other communication technologies like LoRa and LTE CAT-1 should also be part of the discussion. The main reason behind not considering LTE CAT-1 for this application was the high-power consumption and the main area where it excels, a high data rate is not a requirement. On the other hand, LoRa is highly power efficient but its low data rate and high latency make it an in-viable option. A comparison between the standards is shown in Table II. LTE cat-M was preferred over NB-IoT thanks to lower latency, higher peak data rate, and better coverage [43]. LTE cat-M is a low-power wide-area (LPWA) air interface that enables connection between IoT and M2M devices with medium data rate requirements. It can support up-link and down-link speeds of 375 kb/s in half-duplex mode which is ideal for IoT applications requiring a low to medium data rate [44]. Another benefit of LTE-M is “frequency hopping” among LTE sub-carriers making LTE-M more resistant to fading, interference as well as network congestion issues [45]. For this work, we use a commercial LTE cat-M network from a U.S.-based

TABLE II  
COMPARISON OF LEADING COMMUNICATION TECHNOLOGIES [35], [38], [39], [40]

|                    | CAT-NB1                 | CAT-M1              | CAT-1             | LoRa                    |
|--------------------|-------------------------|---------------------|-------------------|-------------------------|
| Peak Data Rate     | 27.2/33.25 kb/s (DL/UL) | 375 kb/s (DL/UL)    | 10/5 Mb/s (DL/UL) | 0.3-50 (DL/UL)          |
| Radio Spectrum     | 180 KHz                 | 1.4 MHz             | 20 MHz            | 125 KHz                 |
| Latency            | 1.5-10 s                | 100-150 ms          | 50-100 ms         | High (Device Dependent) |
| Max. Coupling Loss | 164 dB                  | 155.7 dB            | -                 | 157 dB                  |
| Tx Power           | 46dBm/23dBm (DL/UL)     | 43dBm/23dBm (DL/UL) | 23dBm (DL/UL)     | 27dBm (DL/UL)           |
| Number of antennas | 1                       | 1                   | 2                 | 1                       |
| VoLTE support      | No                      | Yes                 | Yes               | No                      |
| Power Consumption  | LOW                     | LOW                 | HIGH              | LOW                     |

carrier to transmit the synchrophasor data generated with the AT-mega2560.

#### IV. EXPERIMENTAL RESULTS

In this section, experimental results on the generation of synchrophasors  $\xi(t_i)$  and on the performance of the proposed communication solution are reported.

##### A. Synchrophasor Generation

Experimental results were obtained with the AC signal generator yielding a power signal with nominal values for magnitude and frequency of  $v_0 = 2$  V and  $f_0 = 50$  Hz, respectively. Synchrophasors  $\xi(t_i)$  are computed and reported at a rate of 50 frames/s and the obtained values are shown in Fig. 4. This figure includes, from the top to the bottom, magnitude  $v(t_i)$ , phase  $\varphi(t_i)$ , frequency  $f(t_i)$ , and ROCOF  $\rho(t_i)$ , obtained in a 50 s experiment.

The frequency plot, depicted in Fig. 4(c), shows that  $f(t_i)$  fluctuates around the nominal value of  $f_0 = 50$  Hz. These fluctuations can have several causes, such as imperfections in the signal generator device or in the sine-to-square wave converter circuit described in Section III-A. In particular, the AC signal generator could operate at a frequency  $f(t_i) = f_0$ . As previously identified in [29], this fluctuation leads to incorrect DFT computation, whose sampling frequency is based on  $f_0$ , and causes: 1) a fluctuation in the magnitude as a sinusoidal at a frequency  $f(t_i) - f_0$ , as shown in Fig. 4(a) and 2) a “saw-tooth” behavior of the phase  $\varphi(t_i)$ , confirmed by Fig. 4(b), where  $\varphi(t_i)$  keeps on growing from  $-\pi$  to  $\pi$  when  $f(t_i) > f_0$ . Since  $f(t_i)$  is predominantly (92% of the observed values) greater than  $f_0$  [see Fig. 4(b)], we can notice a similar trend to a sinusoidal in the magnitude plot in Fig. 4(a) and the expected saw-tooth behavior in the phase plot in Fig. 4(b).  $\rho(t_i)$ , computed as  $(f(t_i) - f_0) \cdot f_0$  [37], has a similar trend to  $f(t_i)$  [Fig. 4(d)]. This analysis shows the capability of the deployed  $\mu$ -PMU to estimate the magnitude, phase, and frequency of a voltage waveform. In the remainder of this section, we provide a detailed analysis of the experimental LTE cat-M network performance results.

##### B. Network Performance

Network performance is extremely important to assess the feasibility of the proposed synchrophasor sensing and communication framework and to understand how to use the generated synchrophasor data. In this section, we carry out a detailed analysis of relevant network key performance indicators (KPIs), such as the delay  $D(t_i)$  and jitter. The delay  $D(t_i)$  has six components  $\delta_k$ , as discussed in Section III-C. From our experimental results,  $\delta_1$  and  $\delta_3$  last less than 1 ms, whereas  $\delta_2$  takes on average 1–2 ms.  $\delta_6$  is equal to zero for almost all the synchrophasor frames in our experiments. Therefore, in what follows, we will focus on the LTE cat-M delay and on the Internet delay, which corresponds to  $\delta_4$  and  $\delta_5$ , respectively.

As was illustrated in Fig. 2, synchrophasors  $\xi(t_i)$  are reported using a UDP socket: the client is located in the AT328P, and transmits the synchrophasors  $\xi(t_i)$  at a fixed rate  $\lambda$ ; the server is running at a laptop, connected to the Internet through a DSL router and an Ethernet cable. The server functionally represents the PDC and is in charge of receiving the frames containing synchrophasor data, realigning them, and compensating for errors in the communication: these data are then available to be analyzed and used, as an example, for control and monitoring applications. Moreover, as previously mentioned, the PDC must compute the delay  $D(t_i)$ , which represents the time elapsed from the moment  $\xi(t_i)$  is generated, i.e.,  $t_i$ , and the time instant when  $\xi(t_i)$  is received at the destination, i.e.,  $t$ . These delay values are stored on the laptop hosting the UDP server for post-processing and data analysis. The intertransmission time between consecutive frames, hereafter denoted as  $1t$ , can be easily computed as  $1t = t_i - t_{i-1} = 1/\lambda$ .

In Table III, statistics on the delay  $D_i$  obtained with our experimental setup are provided for different values of reporting rate  $\lambda$ , ranging from 1 to 80 frames/s. The most common values for  $\lambda$  are 50 and 60 frames/s, however, we decided to test the communication system with a broad range of reporting rates in order to gain a deeper insight into the suitability of LTE cat-M for a wide variety of smart grid applications. In Table III, we included minima and maxima, standard deviations, first and third quartiles (i.e.,  $Q1$  and  $Q3$ ), jitters, 95%-confidence intervals of the true mean of the delay and

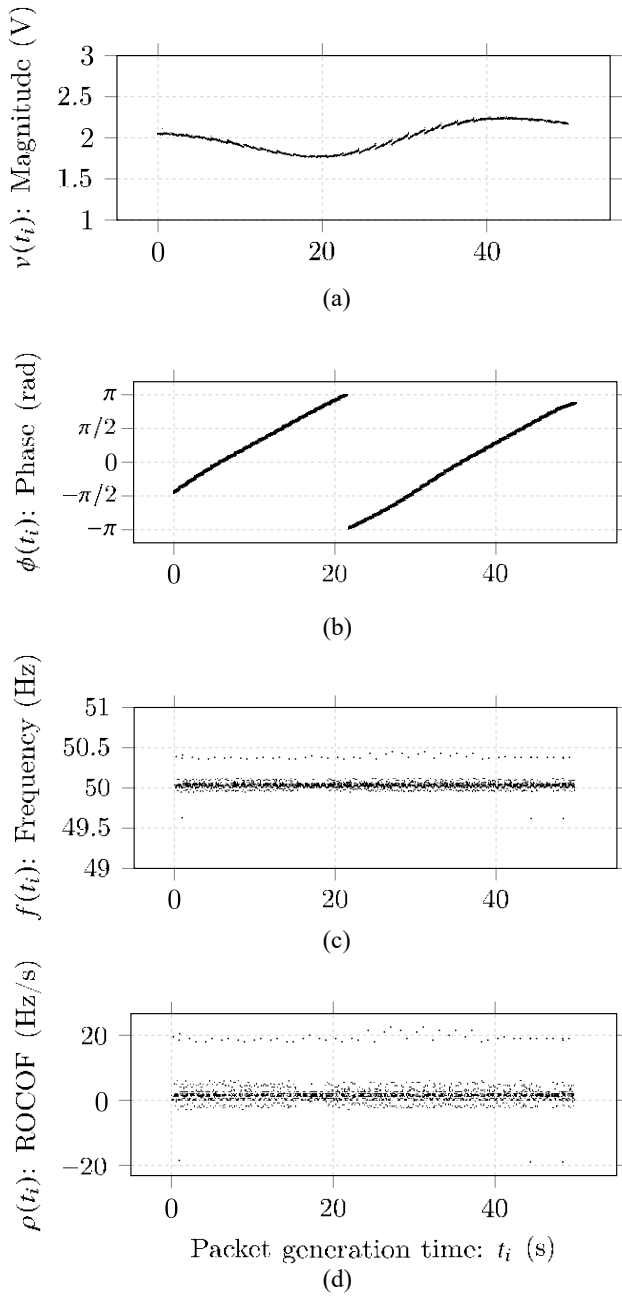


Fig. 4. Synchrophasor characteristics with  $f_0 = 50$  Hz,  $v_0 = 2$  V, and a reporting rate of 50 frames/s. (a) Magnitude plot. (b) Phase plot. (c) Frequency plot. (d) ROCOF plot.

frame loss. The average value of the delay, which can be found in the last column on the right, ranges from 162.95 ms, obtained with  $\lambda = 80$  frames/s, to 173.50 ms, obtained with  $\lambda = 60$  frames/s. It is worth pointing out that no frame loss or performance degradation is observed when the reporting rate grows. From this observation, it can be inferred that LTE cat-M is able to successfully and promptly deliver synchrophasor frames being transmitted at rates of at least up to 80 frames per second. It is also worth highlighting that the standard deviation is very small, ranging from 17.05 to 22.47 ms, which also translates into narrow confidence intervals. The main source of variability in the delay  $D_i$ , as it will become evident in the rest of the analysis, comes from the access portion  $\delta_4$ .

TABLE III  
DELAY STATISTICS VERSUS REPORTING RATE

| Report. rate<br>$\lambda$ (frames/s) | Delay $D_i$ (ms) |        |       |        |        |        |                   |          |
|--------------------------------------|------------------|--------|-------|--------|--------|--------|-------------------|----------|
|                                      | min              | max    | st.d. | Q1     | Q3     | jitter | 95%-CI            | Fr. Loss |
| 1                                    | 145.37           | 201.17 | 20.19 | 147.22 | 187.29 | 40.02  | $168.11 \pm 2.29$ | 0%       |
| 10                                   | 136.14           | 231.89 | 22.47 | 156.29 | 196.16 | 30.03  | $168.78 \pm 0.57$ | 0%       |
| 50                                   | 138.47           | 514.56 | 18.34 | 159.93 | 184.75 | 19.61  | $172.69 \pm 0.29$ | 0%       |
| 60                                   | 136.69           | 246.34 | 17.96 | 157.33 | 188.12 | 18.36  | $173.50 \pm 0.26$ | 0%       |
| 80                                   | 132.97           | 226.44 | 17.05 | 148.86 | 177.91 | 14.14  | $162.95 \pm 0.22$ | 0%       |

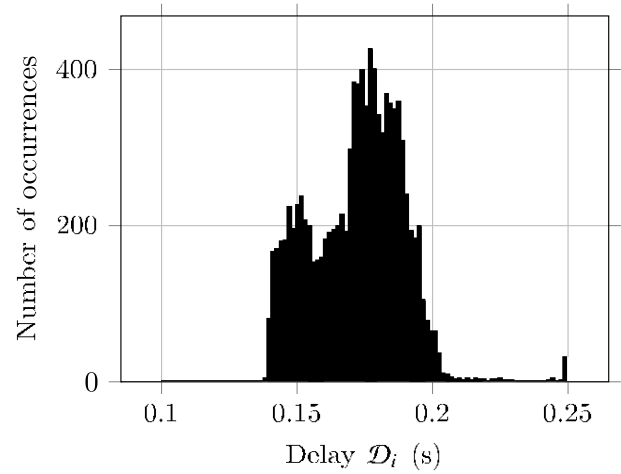


Fig. 5. Histogram of the delays obtained with  $\lambda = 50$  frames/s.

TABLE IV  
MULTI-PMU DELAY STATS ( $\lambda = 50$  FRAMES/S)

| PMU num. | Delay $D_i$ (ms) |     |       |        |        |        |                   |          |
|----------|------------------|-----|-------|--------|--------|--------|-------------------|----------|
|          | min              | max | st.d. | Q1     | Q3     | jitter | 95%-CI            | Fr. Loss |
| 1        | 123.84           | 550 | 56.10 | 148.28 | 183.99 | 20.23  | $175.77 \pm 0.63$ | 0%       |
| 2        | 138.65           | 330 | 41.92 | 166.19 | 199.35 | 25.54  | $183.9 \pm 0.47$  | 0%       |
| 3        | 136.46           | 651 | 49.65 | 162.04 | 195.07 | 22.5   | $182.84 \pm 0.56$ | 0%       |

The distribution of the delay obtained with  $\lambda = 50$  frames/s is shown in Fig. 5. Delays are distributed in the interval between 140 and 250 ms, even though approximately 98% of frames is received within 200 ms. The maximum value of 514 ms, reported in Table III, is not shown in the distribution graph as it is a single value obtained in the first frame transmission (due to the time needed to establish the connection), which makes it irrelevant to the network performance analysis. These results further corroborate the finding that LTE cat-M is a suitable communication solution to transmit synchrophasor data.

A multi-PMU setup and frame size variation were also considered as part of the analysis. Table IV depicts the frame statistics of a 3 PMU setup which transmits simultaneously at 50 frames/s. The 95%-confidence interval of the delay as well as the frame loss is consistent with the results obtained

TABLE V  
DELAY STATS VERSUS FRAME SIZE ( $\lambda = 50$  FRAMES/S)

| Frame Size<br>(bytes) | Delay (ms) |        |       |        |        |        |                   | Loss |
|-----------------------|------------|--------|-------|--------|--------|--------|-------------------|------|
|                       | min        | max    | std.  | Q1     | Q3     | jitter | 95%-CI            |      |
| 26 (1-Phase)          | 138.47     | 514.56 | 18.34 | 159.93 | 184.75 | 19.61  | 172.69 $\pm$ 0.29 | 0%   |
| 42 (3-Phase)          | 160.64     | 293.08 | 14.61 | 182.20 | 204.73 | 16.83  | 193.99 $\pm$ 0.23 | 0.2% |
| 52 (2x)               | 164.11     | 259    | 17.29 | 158.9  | 183    | 31.67  | 170.88 $\pm$ 0.27 | 0.6% |
| 78 (3x)               | 168.14     | 367.62 | 20.37 | 195.96 | 226.41 | 30.14  | 211.38 $\pm$ 0.32 | 3.3% |

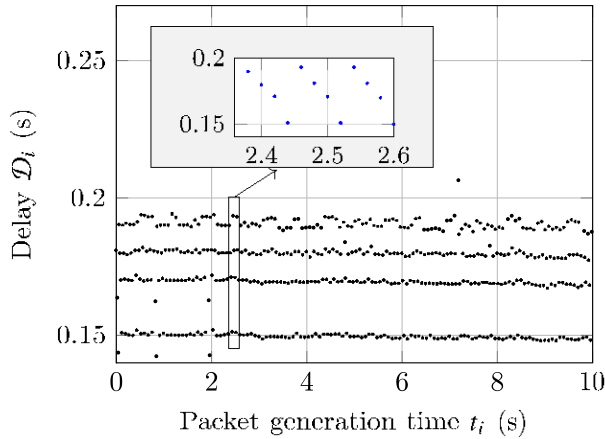


Fig. 6. Delay  $D_i$  with respect to the frame generation time  $t_i$  in an experiment with  $\lambda = 50$  frames/s.

before. Table V shows the impact of frame size variation on the frame statistics, where single phase (26 bytes), 2x single phase (52 bytes), 3x single phase (78 bytes), and 3-Phase (42 bytes) frames were considered. We observed that an increase in the frame size corresponds to increased frame losses. This behavior can be attributed to performance degradation of the LTE module when dealing with larger frame sizes. In fact, as frame sizes are increased, the processing time on the LTE module subsequently increases, and, with packet generation being interrupt driven, any extended delay in the LTE module may lead to packets being dropped from the buffer. However, the delay does not seem to be majorly impacted by the use of multiple  $\mu$ -PMUs or by the increased frame size. In the former, only a very slight increase in the average delay was observed with respect to the single  $\mu$ -PMU case. In the latter case, frames with sizes up to 52 Bytes incurred a delay that, as indicated by the 95% CI, stays consistently within the 160–195 ms range whereas frames with 78 Bytes size were received with more than 200 ms delay, which may be due to the increased processing time at the LTE module. It is important to remark that 78 Bytes frames were also the ones with the largest delay standard deviation, reflecting the moderate performance degradation of the device when dealing with larger frames.

Further insight into the network performance can be gained by analyzing Fig. 6, which displays how the delay  $D_i$  evolves with respect to the transmission time  $t_i$  in a scenario with  $\lambda = 50$  frames/s. In the 10 s observation window reported in this figure, it is possible to notice that the delays are not

uniformly distributed in the range between 150 and 200 ms but are concentrated in the vicinity of 150, 170, 180, and 190 ms. A zoom with the delay of 12 consecutive synchrophasor frames is depicted in a box on top of Fig. 6. A pattern is identified for each group of four consecutive synchrophasor frames, whose delay decreases from the first to the last. In particular, in each group, the first frame is received with a delay of around 190 ms, the second with a delay of around 180 ms, the third with a delay of around 170 ms, and the fourth and last with a delay of around 150 ms. This behavior is observed throughout the whole experiment with  $\lambda = 50$  synchrophasors per second.

In order to explain the reason for such a pattern in the observed delays, it is important to consider the mechanism used to allocate radio resources in LTE cat-M networks. In particular, before each frame transmission, the UE must send a *scheduling request* control message to the eNodeB and must wait for a scheduling grant, which indicates the time and frequency resources to be used for frame transmission. However, scheduling grants are transmitted, along with other data, in the system information (SI) with a periodicity that depends on the network parameter *si-WindowLength-BR-r13*, which could range from 20 to 200 ms [46]. In the commercial network used to obtain our results, this parameter is equal to 80 ms. In the scenario at hand, we have a reporting rate  $\lambda = 50$  frames/s, which leads to an interdeparture time  $1t = 1/\lambda = 20$  ms. Therefore, four frames are expected to be transmitted between two consecutive SI frames. In each 4-frame group, the delay decreases from the first to the last due to decreasing waiting time until the following SI transmission.

To better visualize this effect, in Fig. 7, we have reported the generation time  $t_i$  and the reception time  $t_i^r$  for a number of consecutive synchrophasor frames. It is worth highlighting that  $t_i$  is very close to the transmission time of the synchrophasor frame, as  $\delta_1$ ,  $\delta_2$ , and  $\delta_3$  are negligible, as discussed in Section III-C. Note also that each synchrophasor frame is represented by a segment with the starting point in the  $t$ -timeline at the top and the ending point in the  $t^r$ -timeline at the bottom. For the experiment with  $\lambda = 50$  frames/s, groups of four frames are observed in Fig. 7(a), and the segments representing frames in the same group are drawn with the same color in the grayscale. It is worth highlighting the differences in time distributions of frame transmissions (represented by filled circles on the top timeline) and of the frame receptions (represented by empty circles on the bottom timeline): frame transmission times are equally spaced by 80 ms, whereas the reception times of frames in the same group are just a few ms apart. It is also possible to note that the delay of frames in each group decreases from the first, which has the longest waiting time to the following SI transmission, to the last one, which is the one with the lowest waiting time to the following SI transmission. In Fig. 7(b), a similar plot was generated for a scenario with  $\lambda = 12.5$  frames/s, where a considerably more regular distribution of frame arrival times can be observed. This is due to the fact that frames are transmitted at an interdeparture time of  $1t = 1/12.5 = 80$  ms, which is equal to the SI periodicity parameter: this means that frames



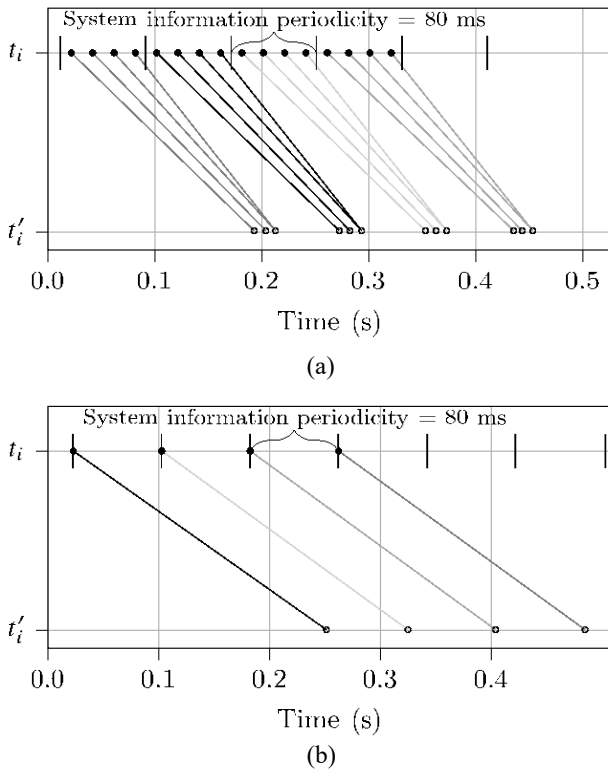


Fig. 7. Timeline with generation time  $t_i$  and the reception time  $t'_i$  for synchrophasor frames with (a)  $\lambda = 50$  frames/s and (b)  $\lambda = 12.5$  frames/s.

wait, on average, the same time before being transmitted over LTE cat-M.

## V. CONCLUSION

In this article, we presented research on the experimental deployment of a  $\mu$ -PMU device and an analysis of the feasibility of using the LTE cat-M network to support high-rate data collection from these devices. A functional prototype of a  $\mu$ -PMU was deployed using simple hardware, such as Arduino micro-controllers and GPS antennas. The deployed  $\mu$ -PMU was equipped with a wireless card to transmit over an LTE cat-M commercial network.

A wide variety of reporting rates for synchrophasor data (i.e., 1–80 frames/s) was considered in order to represent the traffic generated by a broad range of potential smart grid use cases, such as protection and control applications, state estimation, and outage management. Synchrophasor data were generated in compliance with the widely adopted IEEE C37.118.2 standard.

A detailed LTE cat-M network performance analysis was carried out, with average delays below 200 ms in all the considered scenarios, making LTE cat-M particularly suitable to support this type of traffic. Finally, the effects of network parameters, such as the SI periodicity, on the network performance were studied. It was shown that this parameter considerably affects the time distribution of the frame arrivals, which is strikingly different from the periodic distribution of the frame generations.

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