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Numerical demonstration of a topologically-protected electroacoustic transistor

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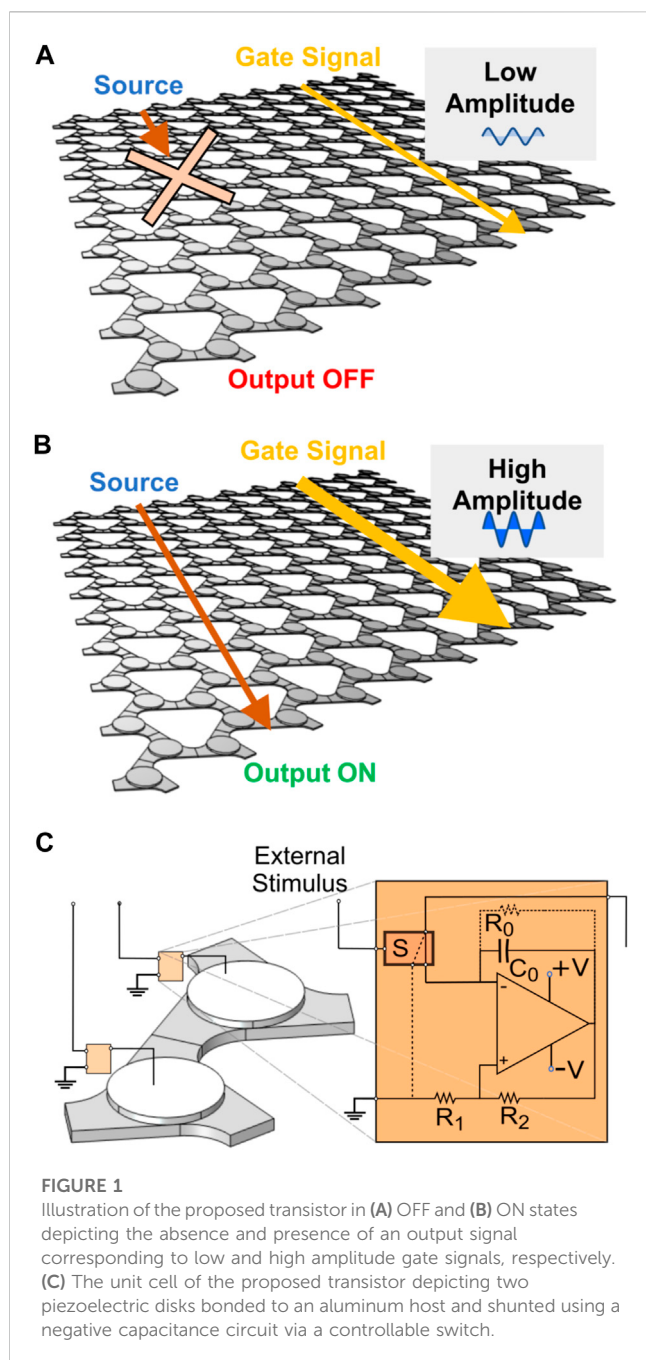
In this paper we conceptualize electroacoustic transistors based on topologically protected interface states in a reconfigurable valley-Hall topological insulator. Using piezoelectric media and active shunt circuits, we numerically model the spatial inversion symmetry breaking in a unit cell to produce topological bandgaps. These gaps are known to host robust modes for wave propagation along an interface. We use two such modes to design a transistor where the wave propagation in one topological channel switches on or off a second topological channel between a source and receiver elsewhere in the structure. Multiple such transistors may be combined to develop logic gates. Further, we develop and simulate the behavior of an electronic circuit which enables the transistor action. Our design opens a pathway to novel wave-based devices which may find applications in structure-based computing, as hybrid multiplexers in communication devices, and as structural switches or embedded sensors in robotics and internet of things.

KEYWORDS

wave-based logic, valley-hall effect, elastic topological insulators, reconfigurable metamaterials, piezoelectric devices, shunt circuits

1 Introduction

Topological acoustics has attracted attention in recent years owing to the robustness of edge and interface states exhibiting scattering-free wave propagation. First identified as electronic states in condensed matter (Hasan and Kane, 2010; Qi and Zhang, 2011; Lu et al., 2014), such phenomena have now been established in photonic (Haldane and Raghu, 2008; Raghu and Haldane, 2008; Khanikaev et al., 2013), electromagnetic (microwave frequencies) (Wang et al., 2009; Poo et al., 2011) and acoustic media (Fleury et al., 2014; Yang et al., 2015; He et al., 2016). Topological modes found in acoustics are analogs of quantum effects such as the quantum Hall effect (QHE) (Von Klitzing, 1986), quantum spin-Hall effect (QSHE) (Kane and Mele, 2005), or quantum valley-Hall effect (QVHE) (Mak et al., 2014). While the quantum Hall effect requires breaking time reversal symmetry (TRS) in the system, the other two only require spatial inversion symmetry (SIS) to be broken. The robustness associated with the simpler SIS breaking is lower than with TRS breaking (Noh et al., 2018). However, the waveguiding offered by such topological insulators is still superior to conventional waveguides (Mousavi et al., 2015). Amongst the three, QVHE-analogs are the simplest to achieve as they do not require external bias, like QHE-analogs, or strong coupling of modes, like QSHE-analogs. QVHE was first predicted in graphene (Rycerz et al., 2007; Xiao et al., 2007; Yao et al., 2008; Zhang et al., 2011) and subsequently observed in solid-state devices (Gorbachev et al., 2014; Mak et al., 2014; Sui et al., 2015).



A valley-Hall topological insulator (VHTI) is typically designed from a hexagonal unit cell with SIS (or closely-related mirror symmetry (Lu et al., 2017)) known to possess Dirac cones (Ochiai and Onoda, 2009; Mei et al., 2012; Li et al., 2014)) in its band structure. The inversion symmetry is broken to open a topological bandgap at the vertex of the Dirac cone. At frequencies within the gap, topologically protected waves propagate along an interface of two mediums composed of distinct, mirrored SIS-broken unit cells on either side. VHTIs have been demonstrated using photonic (Ma and Shvets, 2016; Dong et al., 2017) and acoustic periodic media (Zhang et al., 2018; Kliewer et al., 2021; Qu et al., 2021; Wang et al., 2021). Particularly in elastic systems, VHTIs have been demonstrated by

breaking mirror symmetry through thickness variations (Ma et al., 2019), strain field tuning (Liu and Semperlotti, 2018), arrays of resonators (Pal and Ruzzene, 2017), arrangement of localized masses (Vila et al., 2017), and other scatterers (Darabi and Leamy, 2019; Gao et al., 2021).

Topological insulators are attractive candidates for acoustic logic devices as they offer the advantage of nearly scattering-free (lossless) wave propagation through topological channels, which may be scaled using MEMS/NEMS technology. Reconfigurability is a highly desired feature in topological media for supporting the development of wave-based devices offering acoustically-controlled output. In recent literature, researchers have demonstrated a programmable acoustic topological insulator where the sound propagation path is altered by physically moving cylindrical inserts in a hexagonal lattice using solenoids (Xia et al., 2018). Another work proposed topological phononic logic by reconfiguring the geometry of a hexagonal unit cell using ultrasonic heating (Pirie et al., 2022). However, these acoustic topological insulator designs reconfigure on relatively slow time scales. An alternative means to achieving reconfigurability is through changes in material properties. Such reconfigurable topological insulators have been demonstrated using piezoelectric media and active shunt circuits (Darabi et al., 2020a; Darabi et al., 2020b; Darabi et al., 2021). As such, topological waveguiding is achieved near-instantaneously by switching electrical shunts in the system.

In this work, we propose and model an electroacoustic transistor where wave propagation between two locations on the periphery of the device is controlled by an input wave at a peripheral gate location, similar to the operation of a field effect transistor (FET). FETs typically contain three terminals; namely a gate, drain and a source. A voltage at the gate terminal determines the current flow between the drain and source terminals. Similarly, in our proposed device, the presence of a wave input at a gate terminal is used to *establish* a topological channel between a wave source and a drain (output) located elsewhere in the transistor structure. The amplitude of the input gate wave below or above a set threshold results in OFF or ON states of the output as shown in Figures 1A, B, respectively. We present a general design procedure to develop such electroacoustic transistors and demonstrate, using finite element (FE) simulations, the presence of the required topological interfaces. Further, we develop an electronic circuit which supports the transistor action. The proposed device opens a pathway towards rapid structure-based logic using hybrid electrical-acoustic elements and may find applications in industry 4.0; internet of things (IoT) and robotics as embedded sensors and structural switches; and as multiplexer/demultiplexer elements in next-generation communication devices.

2 Electroacoustic unit cell

We begin with the unit cell depicted in Figure 1C. Conceptually, it consists of two piezoelectric disks [e.g., made of lead zirconate titanate (PZT)] bonded to a host material (e.g., aluminum). By using an active shunt circuit, specifically a negative capacitance shunt circuit (Date et al., 2000; Beck et al., 2013; Chen et al., 2014), we can break the spatial inversion symmetry in the unit cell by shunting one

piezoelectric disk and short-circuiting the second. The equations governing the piezoelectric media are given as (Erturk and Inman, 2011)

$$\begin{aligned} \mathbf{S} &= \mathbf{s}_E \mathbf{T} + \mathbf{d}^T \mathbf{E} \\ \mathbf{D} &= \mathbf{d} \mathbf{T} + \epsilon \mathbf{E} \end{aligned} \quad (1)$$

where $\mathbf{S}$ denotes the strain, $\mathbf{T}$ the stress, $\mathbf{D}$ the electric displacement, and $\mathbf{E}$ the electric field. The material compliance, electromechanical coupling, and permittivity are denoted by $\mathbf{s}_E$, $\mathbf{d}$, and ϵ , respectively. Upon shunting either piezoelectric disk with a negative capacitance circuit, the charge on the PZT for a given strain can be increased or decreased, which results in the variation of the effective elastic modulus via the piezoelectric effect. The elastic modulus, Y , for a simplified case of uniform electric field in the out-of-plane direction, is given as (Date et al., 2000),

$$Y = Y_0 \left[1 - \frac{k_{31}^2}{(1 - \alpha)} \right]^{-1} \quad (2)$$

where Y_0 denotes the short-circuit Young's modulus of the piezoelectric medium, k_{31} the electromechanical coupling coefficient, and $\alpha = |C_n|/C_p$ the ratio of negative capacitance, C_n , offered by the shunt circuit, to the inherent capacitance, C_p , of the piezoelectric disk. The negative capacitance shunt circuit can be constructed using an operational amplifier, passive resistances R_0 , R_1 and R_2 , and capacitance C_0 , as shown in the circuit depicted in Figure 1C. In this scheme, the circuitry offers a negative capacitance $C_n = -C_0 R_2 / R_1$ and can be used to reduce the elastic modulus of the piezoelectric disk. A relay S can be used to switch between shorted and shunted states of the piezoelectric disk. This gives an electrical handle on the unit cell symmetry. Alternatively, the relay could be used to turn on or off the operational amplifier power supply as used in Ref. (Darabi et al., 2021). This would reduce the number of relays used. However, the powered off condition of the supply would result in an open or nearly open circuit configuration of the piezoelectric disk depending on the electrical impedance of the powered-off operational amplifier and passive components. We consider typical values of $Y_0 = 74$ GPa, $k_{31} = 0.37$ and $C_p = 3.5$ nF (e.g., Steminc part # SMD15T09S411) for the PZT disk in the unit cell. A value of α close to 1 results in a large deviation from short-circuit elastic modulus of the PZT. However, practical implementation of such a shunt circuit is prone to instabilities. We consider $\alpha = 1.2$ to keep the circuit sufficiently away from an electrical instability (Marconi et al., 2020). Using Eq. 2, the shunted PZT modulus obtained with $\alpha = 1.2$ is $Y = 44$ GPa. The required $C_n = -5.6$ nF can be constructed with any combination of the passive components of the NC circuits. For instance, $C_0 = 1.6$ nF, $R_1 = 1$ k Ω and $R_2 = 3.5$ k Ω can be used for this purpose. Typically, a high value for R_0 (~ 1 M Ω) is used to keep the shunt circuit stable at high frequencies. Using the elastic modulus for the shorted and shunted PZTs, the unit cell (and the transistor) can be studied by solving the governing equation for elastic waves (Graff, 2012) with appropriate boundary conditions,

$$\frac{E}{2(1+\nu)(1-2\nu)} \nabla(\nabla \cdot \mathbf{U}) + \frac{E}{2(1+\nu)} \nabla^2 \mathbf{U} = \rho \ddot{\mathbf{U}}, \quad (3)$$

where $\mathbf{U}$ denotes the displacement field in the domain. E and ν represent the elastic modulus and Poisson's ratio of the

constitutive material model in various regions of the wave propagation domain. Specifically, $E = Y(Y_0)$ for the shunted (short-circuited) PZT disk and $E = 69$ GPa for the aluminum host domain. Poisson's ratio of 0.31 and 0.33 are used for PZT and aluminum, respectively. To obtain large asymmetry in the unit cell, we maximize the region in the host geometry bonded to PZT disks. The area of the host not bonded to the PZT disks can be further altered to enhance bandgaps or shift the frequency of the Dirac cones, thus providing a handle on the operating frequency of the transistor. We formulate an eigenvalue problem by applying Bloch boundary condition to a single cell (Phani et al., 2006). Using a commercial FE package (Multiphysics®C. v. 6.0, 2022), we solve the eigenvalue problem and compute the band structure of the unit cell.

Figure 2A depicts the band structure computed along the irreducible Brillouin zone (IBZ) of the unit cell without (left) and with (right) SIS breaking. Multiple Dirac cones can be identified at the K point in the band structure corresponding to the symmetric unit cell, while bandgaps [shaded in Figure 2A] open in the band structure corresponding to the SIS-broken unit cell, as expected. The color represents the flexural polarization of the mode. A value of 1 on the colorbar indicates that the mode is predominantly flexural while a value of 0 indicates longitudinal modes. A complete bandgap of 3 kHz width is found around 48 kHz in the asymmetric unit cell dispersion. Note that the unit cell symmetry can be broken by shunting either the "lower" disk or the "upper" disk while short-circuiting the other. The two resulting asymmetric unit cells are mirror images of each other and have the same eigenvalues, but are topologically distinct (as described below). For the two asymmetric unit cells, the displacement fields at the K points in the Brillouin zone above and below the gap (marked by $K+$ and $K-$ in Figure 2A, respectively) are depicted in Figure 2B. The mode shapes indicate band inversion and the topological nature of the gap. We further confirm this by computing the Berry curvature and the valley-Chern number given by,

$$\Omega(\bar{k}) = \nabla_{\bar{k}} \times \langle \bar{u} | i \nabla_{\bar{k}} | \bar{u} \rangle, \quad (4)$$

and

$$C_v = \frac{1}{2\pi} \int_{K \text{ or } K'} \Omega(\bar{k}) d\bar{k}, \quad (5)$$

respectively. Figure 2C shows the Dirac cones in the dispersion (in the reciprocal vector basis) near 48 kHz at the K and K' points in the Brillouin zone with the colorbar indicating the flexural polarization of the modes. The numerically computed Berry curvature (Blanco de Paz et al., 2020) of the lower band is depicted in Figure 2D. The K and K' valleys differ in the valley-Chern number by a minus sign as expected. The numerical value (calculated to be ± 0.19) deviates from the ideal theoretical value of $\pm 1/2$ due to strong SIS breaking (Zhu et al., 2018). For a weaker breaking of inversion symmetry (e.g., shunted PZT modulus of 70 GPa) and thus a smaller bandgap, we obtained a value of ± 0.45 for the analogous numerically-computed valley-Chern numbers. With the topological bandgap established, we analyze various possible interfaces to construct an appropriate supercell for the transistor.

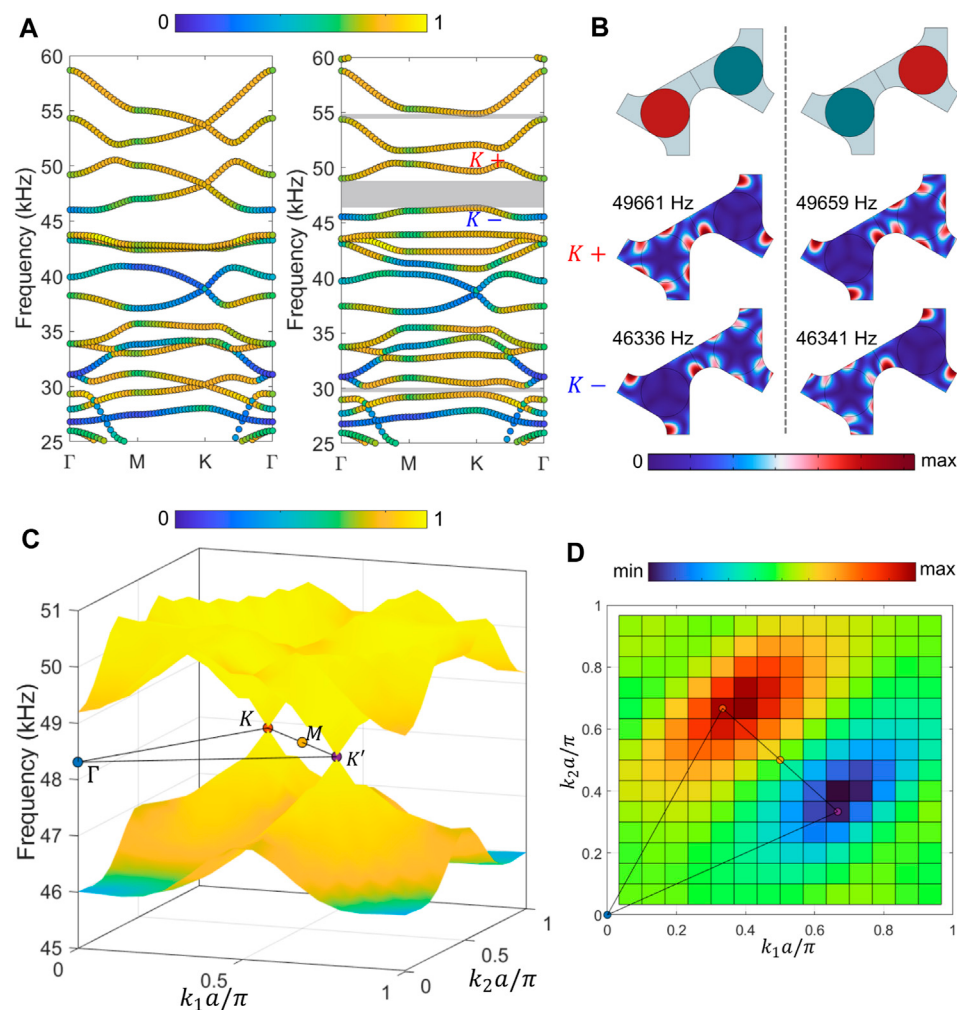


FIGURE 2

(A) Band structure of the unit cell along the IBZ with (left) and without (right) SIS. (B) Displacement field at the $K+$ and $K-$ marked in (A) for mirrored unit cells with broken SIS—red (green) circle indicates shunted (shorted) piezoelectric disk. (C) Dirac cones in the dispersion of the symmetric unit cell at K and K' points in the Brillouin zone. (D) Numerically computed Berry curvature for unit cell with broken SIS.

3 Topological states for electroacoustic logic

To identify the interface states useful for designing the proposed transistor, we study the eigenmodes of supercells made by repeating the unit cell 10 times in one lattice direction. We apply Bloch boundary condition in the other lattice direction and compute the eigenvalues for the system. The PZT disks neighboring an interface can either be shunted or short-circuited. Further, there can be three different types of interfaces, i.e. armchair, bridge and zigzag (Orazbayev and Fleury, 2019). Here, we consider shorted (type A and B) and shunted (type C and D) interfaces of the zigzag (type B and C) and bridge (type A and D) arrangement such that the interface direction is same as one of the lattice vector directions. The states found in the topological gap are identified as either edge modes or interface modes by visually inspecting their mode shape. Figure 3 depicts the four interfaces that are studied. Also shown are the supercell band structures in the frequency range of interest and the mode shape of the interface state close to a frequency of 49 kHz,

marked by a dashed circle in the band structure. The specific operating frequency for the transistor is identified later in the analysis. We refer to the marked state as the ‘first interface mode’ even if it occurs at a higher frequency than other interface modes. In addition to the first interface mode, the supercells with shunted ends (type A and C) or shunted interfaces (type C and D) are observed to host additional modes inside the gap with localization of energy at the respective locations which is similar to the presence of Tamm modes in SSH-like systems (Wang et al., 2018; Chen et al., 2019; Kuchibhatla and Leamy, 2022). We refer to the additional interface state as the “second interface mode”. Figure 4 depicts the out-of-plane displacement field of the two interface modes in the type D interface. The field is normalized to the maxima of the respective eigenmodes for better visualization. The displacement is localized in both the cases with the first interface offering a relatively tighter localization. For constructing the transistor, we look for two interfaces which can be incorporated into a single supercell to enable two distinct states with amplitude localization at the interfaces such that one of them can be switched

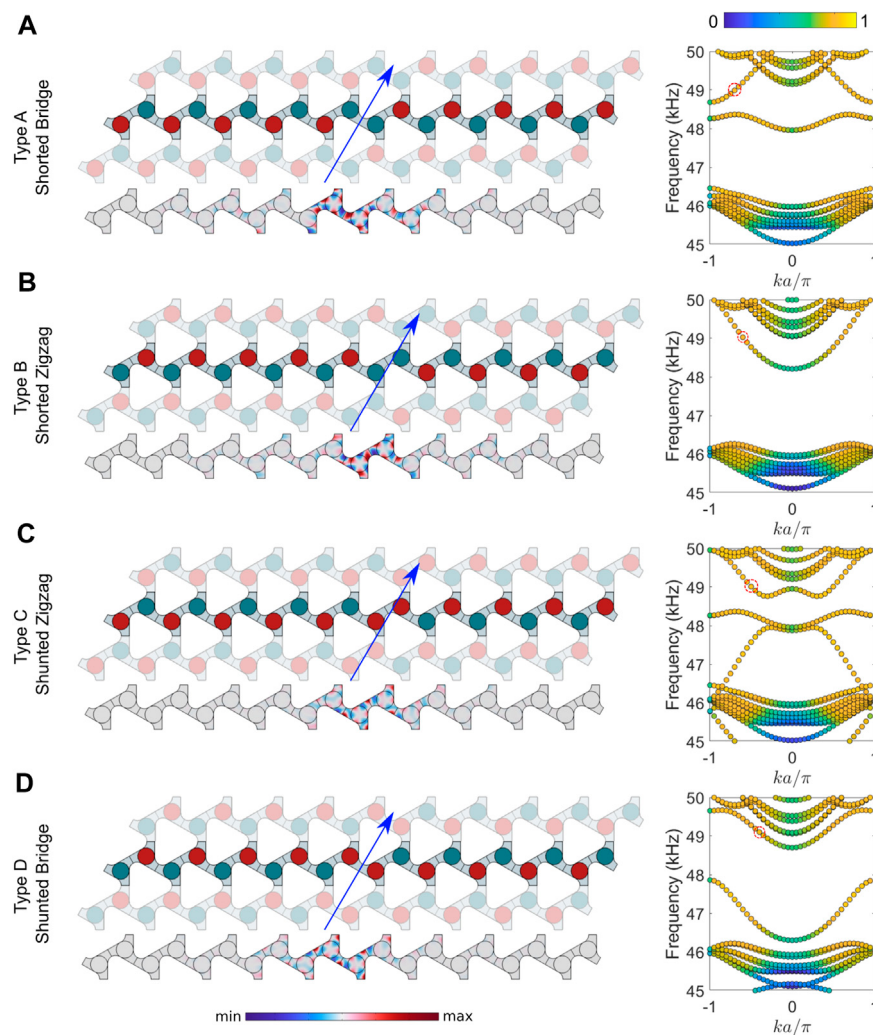


FIGURE 3

Band structures of supercells with two possible cases, neighboring (A,B) shorted and (C,D) shunted PZT disks, of zigzag and bridge type interfaces. The different types of supercells are illustrated with red (green) circles indicating shunted (shorted) PZT disks. The mode shape of the interface state marked by a red dashed circle in the band structure is shown at the bottom of each subfigure.

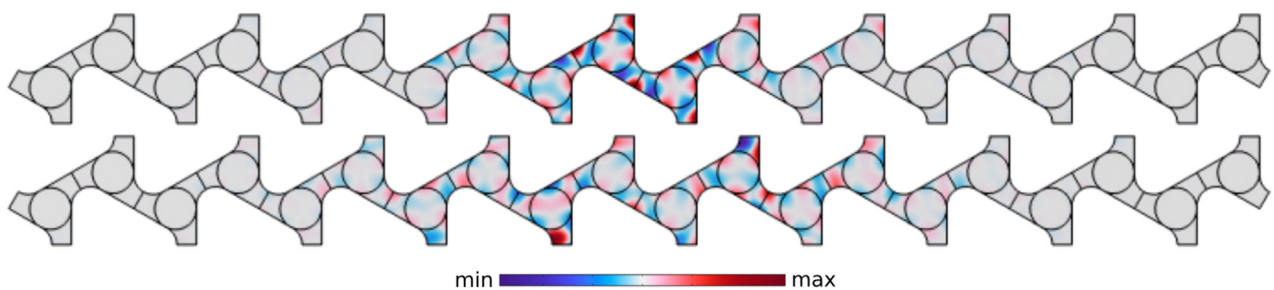


FIGURE 4

Displacement localization in the first (top) and second (bottom) interface mode in the type D interface.

off by reconfiguring a portion of the supercell. The choice of the type of interface is driven by the availability of distinct topological states over a relatively wide range of frequency within the gap.

Since either side of the interface must have a differently configured unit cell, it is not possible to combine two of the same type of interfaces into a transistor supercell without causing

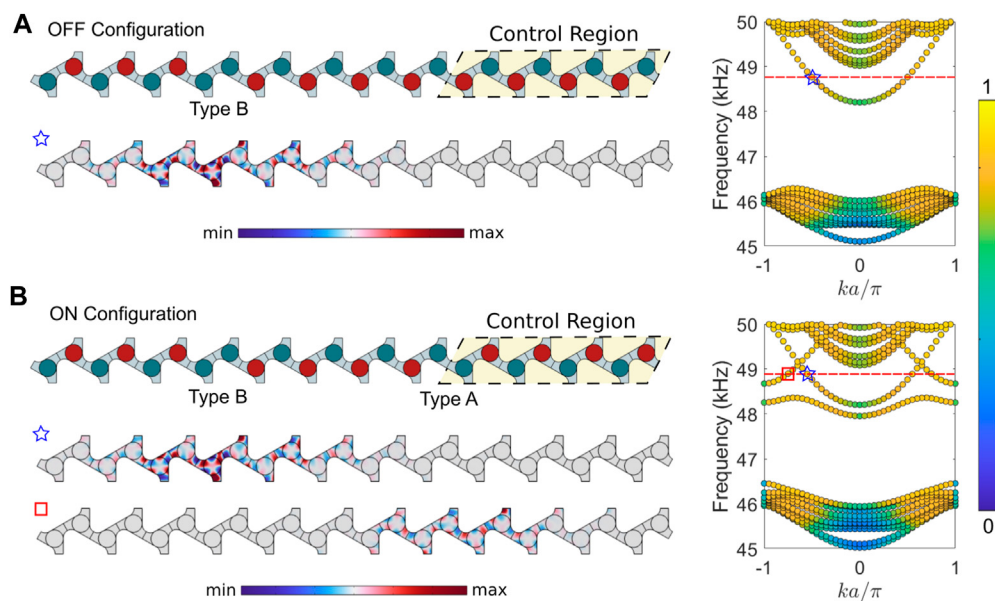


FIGURE 5

(A) OFF and (B) ON states of the transistor supercell constructed using the first interface modes—each subfigure shows the configuration (left), band structure (right) and typical mode shape(s) (bottom) of the interface states. Interface modes for Type B and A are denoted using stars and squares, respectively.

a defect in periodicity or introducing a third interface (which results in extra localized modes). Instead, we choose two different types of interfaces, A and B, to construct the transistor supercell. The imaginary part of the Bloch wavenumber determines the decay of interface waves into the bulk of the medium. The separation between the two interfaces, or between an interface and the terminated end of the supercell, must be chosen based on the imaginary part of the Bloch wavenumber within the unit cell bandgap. For small values of imaginary Bloch wavenumbers the separation distance needs to be large to ensure the waves originating in the two waveguides, or reflected from the ends of the supercell, do not constructively interfere to result in high amplitude displacements other than at the interfaces. For narrow gaps with small values of imaginary Bloch wavenumber, keeping a large separation distance allows for distinguishable localization at the interfaces. This comes at the cost of an increase in the total size of the transistor structure. Taking advantage of the wide topological gap obtained, we chose 12 unit cells with at least 3 cells between interfaces, or an interface and the end of the supercell. Figures 5A, B depict the proposed transistor supercell in the OFF and ON configurations, along with their band structures indicating the presence of a single interface for the OFF configuration and two interfaces for the ON configuration. Typical mode shapes of the transistor supercell depict the localization of displacement at the two interfaces. One of these interfaces (here type B) can be used at the gate terminal (referred to as the gate interface) for the transistor while the other (type A) serves as the topological channel between the source and drain terminals. The transistor can be switched between the two configurations by changing the shunt status of the piezoelectric disks within the control region in supercells marked in Figure 5. At the chosen operating frequency of 48.8 kHz, we note the presence of the type B interface in both OFF and ON states, while the type A interface only

presents in the ON state. As seen in the band structures in Figure 5, there are no other eigenmodes in the system around this frequency and we expect strong localization along these interfaces in a finite structure. As discussed previously, the second interface mode also shows localization at the interface. It is possible to combine, for instance, type C and D interfaces to form a supercell. Using the wider range of frequency offered by the second interface mode, we construct a transistor supercell with 10 unit cells hosting a type D interface at the gate and a type C interface between the source and drain. The supercell is depicted in Figure 6 along with its band structure for OFF and ON configurations. At 47.1 kHz, we find localization in the type D interface in both the OFF and ON states while localization in the type C interface is only present in the ON state (as seen in the modeshapes at the bottom of Figures 6A, B). Again, there are no other eigenmodes in the system around this frequency. These results suggest that the transistor based on the second interface mode is functionally identical to the one based on the first interface mode, albeit at a different operating frequency. We chose to study the transistor behavior using the first interface mode. A transistor based on the second interface mode can be analyzed in the same manner. The transistor action is achieved by switching the control region between ON and OFF states based on an input at the gate using an electrical circuit discussed next.

3.1 Switching topological modes

We next describe an electronic module consisting of active feedback circuits using operational amplifiers (OAs) (Sedra and Smith, 1998) which reads the voltage of a PZT disk in the gate interface and outputs an amplified voltage to the relay S in the shunt circuit of Figure 1C. This module is used to control the PZT disks in

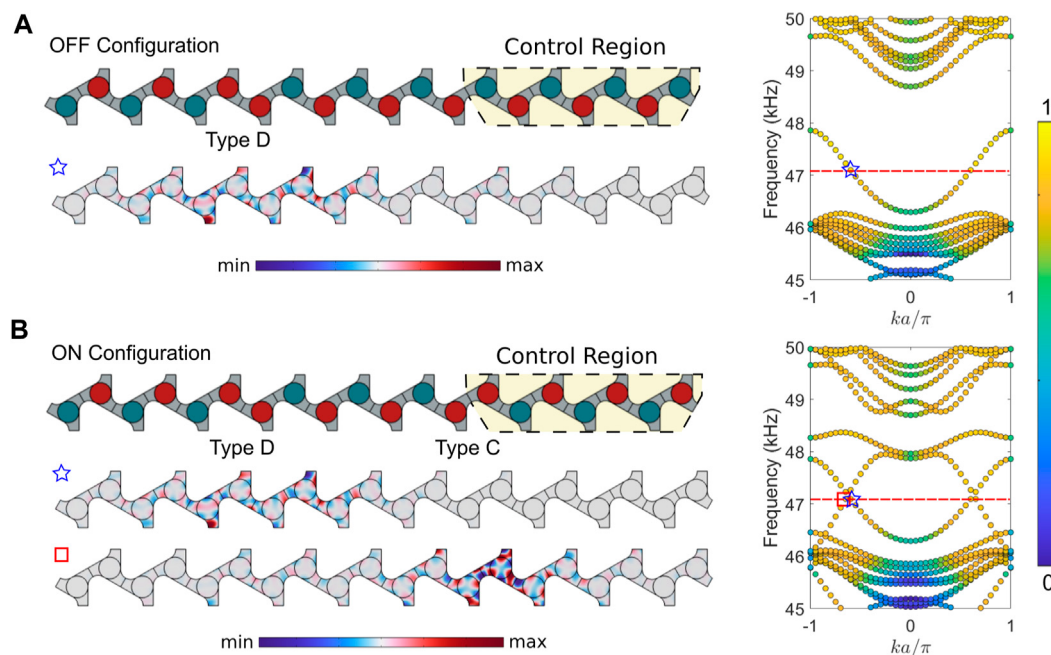


FIGURE 6

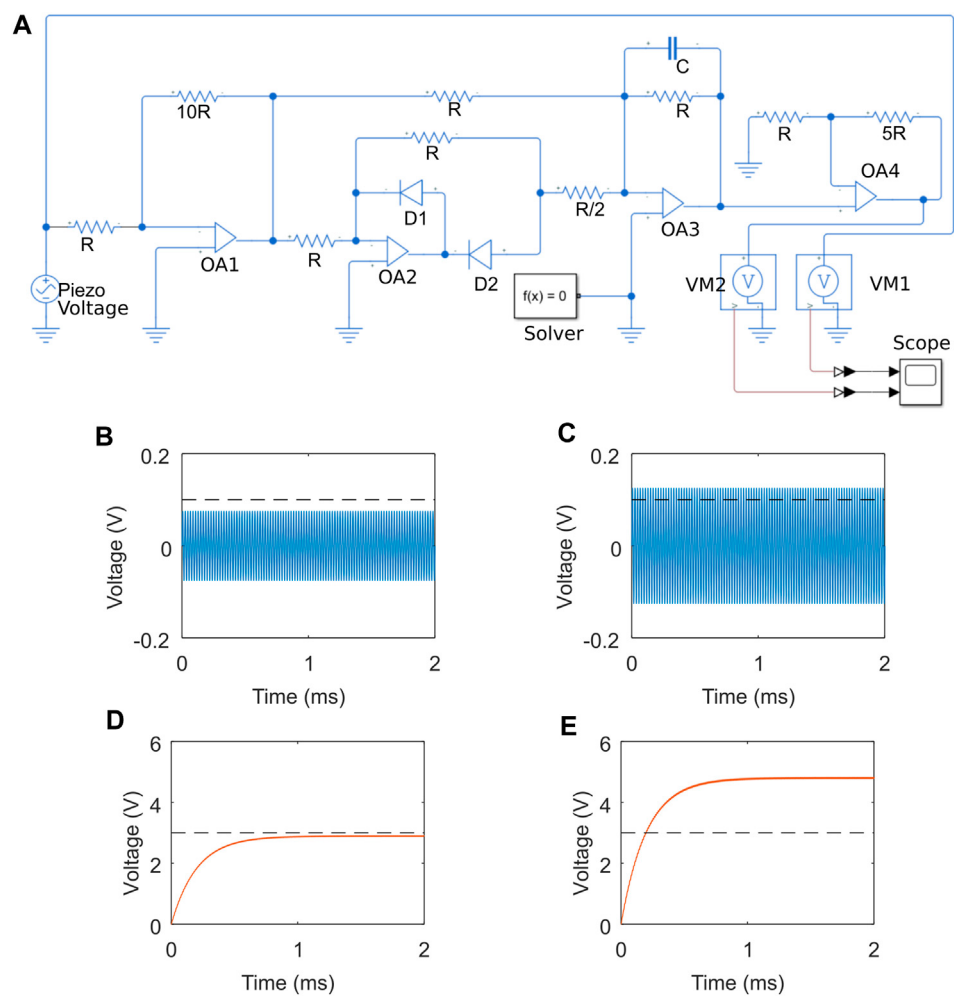
(A) OFF and (B) ON states of the transistor supercell constructed using the second interface modes - each subfigure shows the configuration (left), band structure (right) and typical mode shape(s) (bottom) of the interface states. Interface modes for Type D and C are denoted using stars and squares, respectively.

the control region of the transistor supercell. The module is tuned such that an input wave amplitude above a set threshold generates an output voltage sufficient to trigger the relays, thereby shunting the short-circuited PZTs and short-circuiting the shunted PZTs. Figure 7A depicts the circuit diagram of the electronic module as modeled in Simulink (MATLAB, 2023). The voltage generated across the PZT for small strains is represented by a voltage source. The module amplifies this voltage (using OA1) and rectifies it (using a precision full-wave rectifier implemented with OA2 and OA3) to provide a smooth DC output, which is then amplified by OA4 to supply the trigger voltage. Two different sinusoidal voltages at 48.8 kHz shown in Figures 7B, C, below and above set threshold of 0.1 V (dashed line), are provided as input. The corresponding output of the developed electronic module is shown in Figures 7D, E. The voltage required to trigger a relay (3 V, typical) is marked by a dashed line. Clearly, the module can distinguish a low and high amplitude incoming wave and can trigger the reconfiguring of the control region to switch between the OFF and ON states of the transistor. The threshold values can be conveniently tuned by varying the feedback resistance (marked in Figure 7A as 5R) at the final stage in the electronic module. Next we discuss the predicted response of a finite-sized transistor.

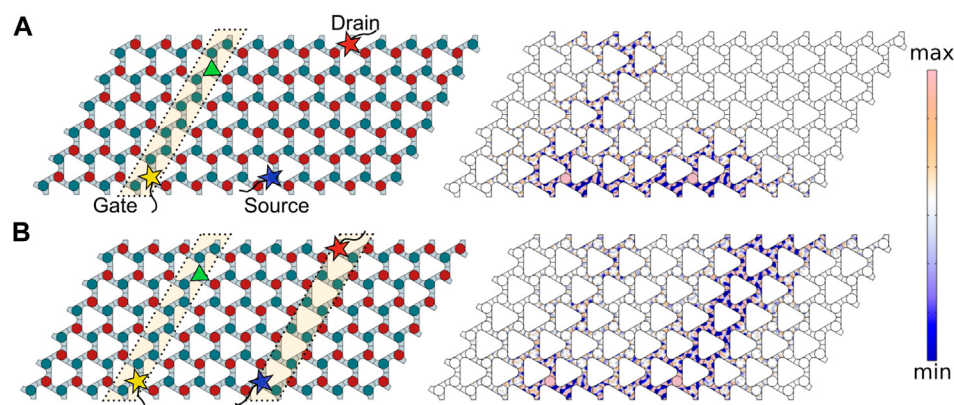
4 Binary output of the topological transistor

The ability to distinguish low and high amplitude waves allows for bit abstraction using the proposed transistor. With

respect to a set threshold, a low (or zero) amplitude wave represents a logical low and a high amplitude wave represents a logical high. We construct a finite transistor structure with 6 repetitions of the supercell in Figure 5. We prescribe a wave input at the gate terminal to mimic an incoming signal. In practice, such an input signal could be generated by an event in the physical surroundings of the transistor, which results in a wave impinging on the domain wall of the device or could be coming from the drain terminal of another transistor. The positions of gate, source and drain are marked using stars and the PZT disk whose voltage is used as input to the electronic module is indicated by a triangle in Figure 8 (left). A continuous wave input independent of the gate is provided at the source. The operating frequency of 48.8 kHz (eigenfrequency of the two interface states identified in the supercell) is used to simulate the harmonic response of the system. Figure 8A depicts the transistor OFF configuration (left) and the displacement field at steady state (right) while the same is depicted in Figure 8B for the ON state. The topological interface between the source and drain has no wave/vibration energy in the OFF state, whereas in the ON state we see a high-amplitude localized standing wave pattern established along the interface. We note that the response in the gate interface is relatively low. This is primarily due to the difference in the wavenumber associated with the interface modes at this frequency which results in different amplitudes of standing waves in the finite structure. The threshold of the electronic module can be tuned to recognize the difference between low and high amplitude inputs specifically in the gate interface. Moreover, each transistor

**FIGURE 7**

(A) Electrical circuit designed to switch a topological interface. Voltage across a PZT disk (B) below and (C) above a set threshold (dashed line) provided as input to the electrical circuit. (D,E) corresponding output voltage of the circuit.

**FIGURE 8**

The configuration (left) and the displacement field (right) across the finite-sized transistor in the (A) OFF and (B) ON states at an operating frequency of 48.8 kHz. The gate, source and drain terminals of the device are indicated by stars. The triangle indicates the position of the PZT disk in gate interface connected to the electronic module. The topological interfaces in the configurations are highlighted with dashed borderline.

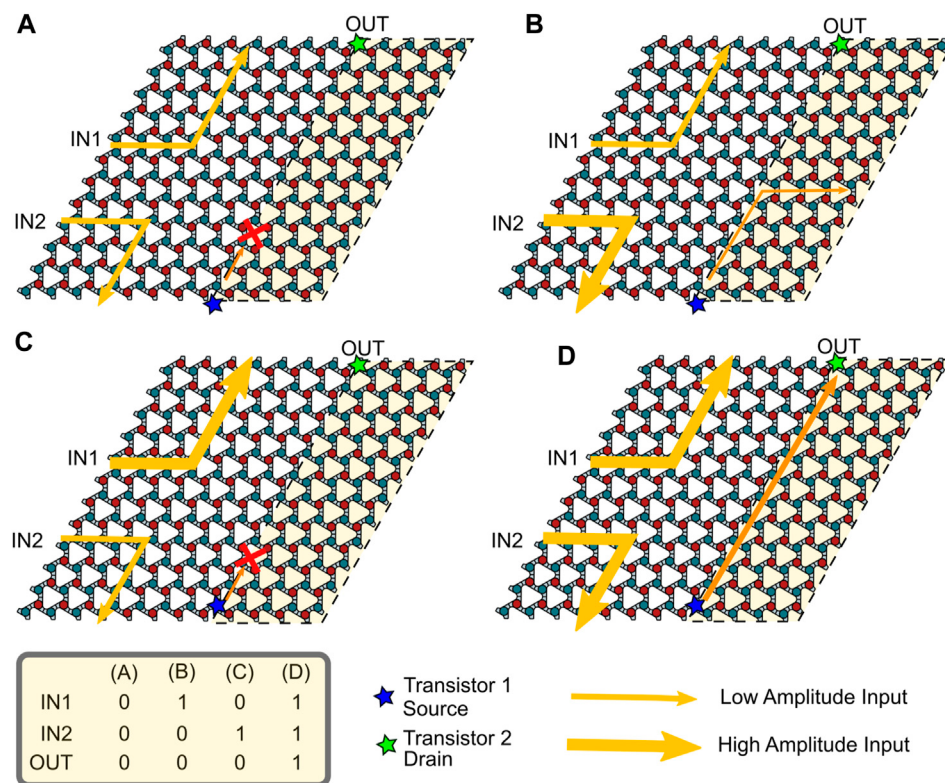


FIGURE 9

Configuration of an AND logic gate for different combinations (A–D) of inputs (IN1 and IN2) listed in the truth table shown at the bottom. 0 (1) in the truth table represents low (high) amplitude wave. Red (green) filled circles represent shunted (shorted) PZT disks. The control region of the logic gate which is reconfigured based on the inputs is marked by dashed line and highlighted.

can have a different threshold setting as required by its application.

4.1 Boolean operations

The transistor is designed as a monolithic structure and allows us to combine multiple transistors to produce logic gates in a manner similar to conventional FETs. As an example, we present here the design of an AND gate. The designed logic gate is a combination of two transistors. It takes inputs at two gate terminals (IN1 and IN2) to reconfigure the control regions of the two transistors hosted within a single electroacoustic structure. This results in the flow of the wave energy between the source of one transistor and the drain of the second in accordance with the truth table of the logic gate. The reconfigured states corresponding to the different rows of the truth table are shown in Figure 9. A value of 0 in the truth table is equivalent to a low-amplitude wave while a value of 1 indicates a high-amplitude wave at the gate. Since there are no other (edge) modes for wave propagation near the operating frequency the two input waveguides are isolated. Further, as the topological waves are known for minimal scattering at corners, a high amplitude wave in IN1 does not trigger IN2. In a similar manner, logic gates such as OR and NAND can be developed using the proposed transistor by appropriately configuring topological wave paths in tandem.

5 Concluding remarks

In summary, we proposed and numerically verified electroacoustic transistors enabled by reconfigurable interface states in valley-Hall topological insulators. We outlined a design procedure to obtain such interface states in piezoelectric media by using active shunt circuits. We demonstrated through band structure and harmonic response computation that several such states can be leveraged to construct a transistor. Further, we designed and numerically modeled an electronic circuit that enables the transistor action. Such transistors provided two logically distinct states for bit abstraction and can be combined together like conventional electronic transistors to create logic gates. We envision the proposed electroacoustic transistors finding applications as structural switches or embedded sensors for robots and IoT. For example, an autonomous inspection robot deployed in harsh environments may use the proposed transistor on its outer body to distinguish between hard and soft contacts in its path. An impact with an external object (which can be expected to excite a wide frequency spectrum including the operating frequency of the transistor) may be used as the gate signal while the transistor output can be used for course correction or decision making. Further, a similar implementation of the electroacoustic transistor with topological surface acoustic waves may open a pathway for devising robust hybrid devices with applications in telecommunications.

Data availability statement

The original contributions presented in the study are included in the article/Supplementary material, further inquiries can be directed to the corresponding author.

Author contributions

SK and ML conceived the idea. SK performed the numerical simulations and data analysis under the supervision of ML. All authors contributed to the article and approved the submitted version.

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Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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