Realizing symmetry-protected topological phases in a spin-1/2 chain with next-nearest-neighbor hopping on superconducting qubits

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Quantum simulation on near-term quantum hardware is a topic of intense interest. The preparation of novel quantum states of matter provides a quantitative assessment of the capabilities of near-term digital quantum computers to implement circuits with structure of relevance to quantum simulation. Here, we conduct a benchmark study by realizing symmetry-protected topological (SPT) phases of a spin-1/2 Hamiltonian with next-nearest-neighbor hopping on up to 11 qubits on a programmable superconducting quantum processor using adiabatic state preparation. Using recompilation techniques to reduce the gate count to around 50 two-qubit gates, we observe clear signatures of the two distinct SPT phases, such as excitations localized to specific edges and finite string-order parameters. We identify a parasitic phase associated with the two-qubit gate as the dominant imperfection that limits the depth of the circuits, indicating a research topic of interest for future hardware development.

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I. INTRODUCTION

Quantum computers have long been of interest for their potential to simulate quantum many-body systems [1–6]. A recent emphasis has been on using quantum computers to treat classically challenging chemistry and condensed matter problems [5–9]. Advances in near-term quantum hardware now make prototype versions of these simulations possible, for instance in the computation of the ground-state properties of chemical [10–17] and solid-state [12,18–20] quantum systems as well as simulation of their real-time dynamics for closed [21–31] and open [32–38] systems. Several recent studies also reported the simulation of finite-temperature physics on near-term devices [39–42].

The realization of topological phases of matter is another area of considerable interest. These phases do not fit within the Landau paradigm of local order parameters associated with symmetry breaking, and the study of their ground-state properties and excitations is an active area of research in condensed matter physics [43–46]. Analog quantum simulators are able to realize some of these phases and associated phenomena such as models with topological band structures [47–51], Thouless charge pumps [52–54], various symmetry-protected topological (SPT) phases [55–60], and quantum spin liquids [61]. On digital quantum computers, the preparation of various topological phases has been reported, including spin-1/2 chain models with three-body interactions [62–65], the toric code [66], and topological Floquet phases [67,68].

Beyond realizing the quantum phase of interest, a comparison of the hardware data against theory can serve to benchmark quantum devices and identify the hardware imperfections that limit circuit complexity [29,69]. These imperfections have varying impacts depending on the particular structure of the circuits, implying benchmarking methods which employ dissimilar circuit structures are inadequate for characterizing devices for quantum simulation applications [70]. For example, many protocols used to assess the performance of quantum computers employ randomized circuits [71,72], which do not accurately reflect the impact of coherent errors in more structured circuits [73,74].

Circuits which perform representative quantum simulation tasks are expected to provide more relevant information on the capabilities of near-term hardware. Spin-1/2 models with beyond-nearest-neighbor interactions are an attractive target of study for quantum simulation due to their richer physics [75,76] and more complex circuits compared to those with only nearest-neighbor (NN) couplings. Of particular interest are topological phases in these models characterized by nonlocal string-order parameters and edge excitations [77]. Hence, the preparation of such phases may serve as a relevant benchmark of the capabilities of present digital quantum computers for quantum simulation.

Here, we report the preparation of SPT phases of a spin-1/2 chain with next-nearest-neighbor interactions on up to 11 qubits of a programmable superconducting quantum processor, Google's Rainbow processor. Circuits with up to 50 two-qubit gates are found to yield the topological signatures of the SPT phases, including finite or zero values of different string-order parameters and edge excitations localized to different sides of the chain depending on the particular SPT phase. Examination of the discrepancies with theory demonstrates that a parasitic phase in the two-qubit gate is the leading limitation on the gate depth. Based on these findings, we estimate the gap between the present achievable gate depth and that required for realization of other novel phases such as chiral spin liquids. Our results provide a benchmark of

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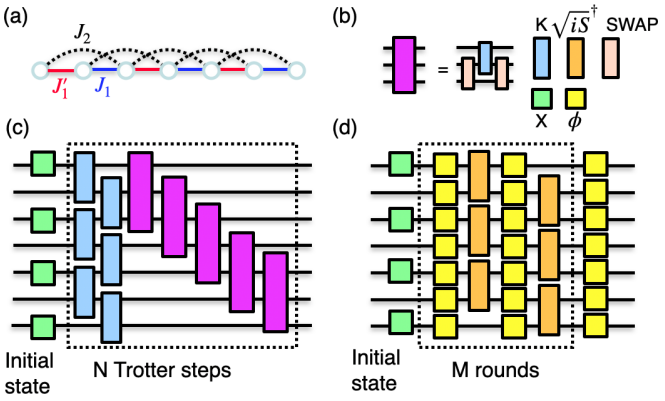

FIG. 1. Schematic of quantum circuits used to prepare the SPT phases. (a) Arrangement of sites in a 1D lattice of seven sites. The strength of interactions going from even-labeled to odd-labeled (odd-labeled to even-labeled) sites are given by J_1' (J_1); those for NNN couplings are given by J_2. For this study, we also consider chains with 9 and 11 sites. (b) Quantum gates used to construct the circuits for the demonstrations. Their matrix representations are provided in Ref. [83]. The gates PHASEDXZ(ϕ) and $\sqrt{iS}^\dagger$ are the native one-qubit and two-qubit gates on the Google Rainbow processor. (c) Circuit to implement Trotterized ASP for a system with seven sites. (d) Schematic of the recompiled circuit with M gate rounds.

the current capabilities and limitations of today's quantum processor in performing quantum simulations based on digitized adiabatic state preparation.

II. THEORY

A. SPT phases of spin-1/2 chain with NNN hopping

We consider a one-dimensional spin-1/2 chain with NN and next-nearest-neighbor (NNN) interactions as shown in Fig. 1(a). Its Hamiltonian is given by

$$\begin{aligned} H_T = &-\sum_k J_1'\left(\sigma_{2k}^x\sigma_{2k+1}^x + \sigma_{2k}^y\sigma_{2k+1}^y\right) \\ &+ J_1\left(\sigma_{2k+1}^x\sigma_{2k+2}^x + \sigma_{2k+1}^y\sigma_{2k+2}^y\right) \\ &+ J_2\left(\sigma_k^x\sigma_{k+2}^x + \sigma_k^y\sigma_{k+2}^y\right), \end{aligned} \tag{1}$$

where $\sigma^x, \sigma^y, \sigma^z$ are Pauli operators, J_1' (J_1) denotes the strength of the NN interactions from the even to odd sites (odd to even), and J_2 denotes the strength of the NNN coupling.

The phase diagram of H_T contains two distinct gapped SPT phases known as the even-parity dimer (ED) and singlet-dimer (SD) phases. The model is in the ED (SD) phase when $J_1' = 2J_1 < 0; J_1 > 0$ ($J_1 = -2J_2 > 0; J_1' < 0$). The solution of the edge states in the two phases were derived by Zou *et al.* [77]. Each edge state is two-fold degenerate and protected by time-reversal (TR) symmetry. The two phases are topologically distinct because they cannot be deformed into one another without breaking TR, inversion, and D_2 symmetry of spin rotation by π about the x, y, and z axes [78].

These phases can be distinguished by the location of their edge excitations; for a lattice with an odd number of lattice points, the ED (SD) phase has an edge excitation on the right (left) edge of the chain. In addition, the phases can be distinguished by string-order parameters, defined as

$$O_{z_n} = -\lim_{r\to\infty}\left\langle\left(\sigma_n^z + \sigma_{n+1}^z\right)e^{i\pi\sum_k\sigma_k^z}\left(\sigma_{2r+n}^z + \sigma_{2r+n+1}^z\right)\right\rangle, \tag{2}$$

where the sum over k is restricted to $n+2 \leqslant k \leqslant 2r+n-1$ and r should be as large as possible. Generally, a nonzero string-order parameter indicates the presence of hidden long-range order and a topologically nontrivial phase. In the present model, the ED (SD) phase exhibits a finite O_{z_n} value for odd (even) n. In this work, n is chosen to be 0 or 1. To select r, we choose the largest value that satisfies the constraint that the number of operators used to construct O_{z_0} and O_{z_1} are the same. This requirement is equivalent to using the maximum integer value of r that satisfies $2r+1+1 \leqslant M$, where M is the number of sites of the system. For systems with $M = 7, 9, 11$, this constraint corresponds to $r = 2, 3, 4$, respectively.

B. Preparation of SPT phases on a digital quantum processor

We used circuits based on adiabatic state preparation [79,80] (ASP) to prepare the SPT phases of H_T on the superconducting quantum processor. The system is initialized in the ground state of an initial Hamiltonian H_I and evolved to the ground state of the target Hamiltonian H_T over time duration T using a linear interpolation $H(s) = (1-s)H_I + sH_T$ where $s \equiv t/T$. In this study, H_T is given in Eq. (1). The initial Hamiltonian is given by

$$H_I = -B_z\sum_k(-1)^k\sigma_k^z, \tag{3}$$

with B_z a uniform external field. For $B_z > 0$ and an odd number of sites, the ground state of H_I is given by $|0101\ldots01010\rangle$ which can be prepared by applying X-rotation single-qubit gates on sites labeled by odd indices.

To carry out ASP, we Trotterized the adiabatic evolution to first order and implemented the resulting steps using quantum circuits constructed from single-qubit and two-qubit quantum gates, as shown in Fig. 1(b) The two-qubit gate K, known as the fermionic simulation (FSIM) gate, can be constructed using the native gate set available on the Rainbow chip [29]. An example of a circuit that implements a single Trotter step for a system of seven sites is shown in Fig. 1(c). Despite extensive experimentation, the overall circuit that carries out the full ASP was found to produce qualitative inaccuracies with theory. To assess the maximum gate depth that could be achieved while yielding quantitative agreement, we used a circuit recompilation scheme [42] by fitting the circuits needed to realize the state at each time in the adiabatic evolution to a parameterized circuit. In Ref. [42], the parameterized circuits consisted of alternating layers of single-qubit gates and two-qubit gates. We used this ansatz in our benchmark studies by using the native gate $\sqrt{iS}^\dagger$ for the two-qubit gate and the native gate PHASEDXZ(ϕ) for the single-qubit gate, respectively. A schematic of the final recompiled circuit is shown in Fig. 1(d). The reduction in circuit depth is discussed in Appendix A.

We used the Google Rainbow and Weber quantum processors for this study. The Rainbow and Weber processors consist of a two-dimensional array of 23 and 54 transmon qubits,

respectively, with each qubit tunably coupled to its neighbors. The native single-qubit gates are the PHASEDXZ gate which consists of a rotation about an axis in the XY plane of the Bloch sphere with an extra phase about the Z axis. The native two-qubit gates are the $\sqrt{iS}^{\dagger}$ gates. Further information on the device parameters are available in Ref. [81]. Simulated data in the absence of noise are generated using Google's circuit emulator QSIM [82].

We perform 8192 repetitions of each circuit with measurements in the Z basis for all sites at each Trotter step. While the quantum circuits implemented conserve the total S_z, the presence of hardware error can lead to S_z nonconservation. We mitigate this error by postselecting the measurements for $\Delta S_z = 0$. The quantities required to compute string order parameters in Eq. (2) can be computed from the measurements in the Z basis. Similarly, the occupancy of the ith site is simply related to the expectation value $\langle \sigma_i^z \rangle$. Both quantities can be directly computed by performing the appropriate sums with the measurement bitstrings. Only those bitstrings with $\Delta S_z = 0$ are used in the computation.

III. RESULTS

A. Signatures of SPT phases

We first report calculations of the string order parameters O_{z_1} for the ED phase versus ASP time s for spin chains with 7, 9, and 11 sites. We collected data from 15 configurations of qubits; based on the $\sqrt{\text{ISWAP}}$ gate cross-entropy benchmarking (XEB) average error per cycle, we selected the ten best configurations, from which we computed the mean and standard deviations for all observables. To prepare the ED phase, the Hamiltonian parameters were set to $J_1 = 0.2$, $J_1' = -1.5$, $J_2 = -0.1$, $B_z = 2.5$, and $T = 3.0$, and $M = 5$ layers of gate rounds were used for circuit recompilation. Emulated results were obtained by running the Trotterized ASP circuit on Google's circuit emulator QSIM.

We plot $|O_{z_1}|$ versus ASP time s on seven sites in Fig. 2(a). We observe good agreement between the final value of $|\langle O_{z_1} \rangle|$ at $s = 1$ obtained from Trotterized ASP using QSIM and the value from exact diagonalization in Fig. 2(a). This result indicates that a Trotter step size of 0.25 is sufficiently small enough to approximate the ASP evolution that yields the ED phase with high fidelity.

We next compare the data obtained by running Trotterized ASP trajectories on QSIM with the data obtained by running recompiled circuits on Rainbow without any error mitigation for seven sites. These circuits required 30 $\sqrt{iS}^{\dagger}$ gates. Although the trend of O_{z_1} increasing with ASP time is reproduced as seen in Fig. 2(a), a clear discrepancy exists for the final value of O_{z_1} at the end of the adiabatic trajectory. To mitigate this discrepancy, we perform postselection based on S_z conservation. We observe a marked improvement in the quality of the hardware data, with quantitative agreement obtained between the hardware data and the simulator. With this error mitigation step, the quantum processor is able to reproduce the adiabatic trajectory with sufficient fidelity to arrive at the expected nonzero value of the string-order parameter in the ED phase.

We next compute O_{z_1} for system sizes of 9 and 11 qubits. The number of two-qubit gates used in the recompiled circuits

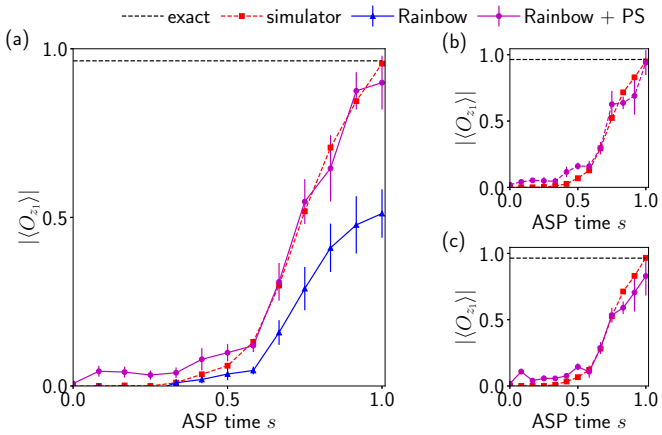

FIG. 2. Preparation of ED phase for increasing system sizes on Rainbow quantum processor. Absolute value of the string-order parameter O_{z_1} versus ASP time s for a system size of (a) 7, (b) 9, and (c) 11 qubits, respectively. Data from Rainbow were collected using 15 different configurations of qubits, and only the best 10 configurations were selected based on their $\sqrt{\text{ISWAP}}$ gate XEB average error per cycle. The hardware data without any error mitigation (blue triangles) yield qualitative agreement with the emulated ASP trajectory (red squares). Quantitative agreement is obtained when postselection is used (purple circles). The ED phase can be prepared reliably for system sizes of up to 11 qubits. The parameters $J_1 = 0.2$, $J_1' = -1.5$, $J_2 = -0.1$, $B_z = 2.5$, and $T = 3.0$ are used to prepare the ED phase. The lines through the symbols are guides to the eye.

was 40 and 50, respectively, compared to 30 in the seven-qubit case. Despite the larger number of gates, we observe good agreement in the value of the string-order parameter over the adiabatic trajectory in Figs. 2(b) and 2(c), although with a slight degradation that likely arises from the deeper circuits. The data indicate that the SPT phases for a system of 11 sites can be prepared with enough fidelity to observe its topological features on the Rainbow quantum processor.

Next, we verify that we can distinguish the SD and ED phases using the string order parameters. Figure 3(a) and 3(b) shows $|O_{z_0}|$ and $|O_{z_1}|$ versus s on 11 qubits when the model is tuned into the ED phase. We observe good agreement between the hardware data and the simulator over the adiabatic path. At the end of the adiabatic path, we measure 0.029 ± 0.007 and 0.829 ± 0.147 for O_{z_0} and O_{z_1}, respectively, which is in good agreement with the expected values of ~ 0 and 0.964. Similarly, we tune the model into the SD phase by setting the Hamiltonian parameters to $J_1 = 1.5$, $J_1' = -0.2$, $J_2 = -0.1$. The string-order parameters O_{z_0} and O_{z_1} versus s are given in Figs. 3(c) and 3(d), respectively. Again, the final values of the string-order parameter from the hardware are 0.981 ± 0.085 and 0.034 ± 0.013, which are in quantitative agreement with the numerically determined exact values of 0.962 and ~ 0. In both cases, we measured a finite value for the appropriate string-order parameters and nearly zero for the other, indicating that the correct SPT phases were successfully prepared.

Finally, we plot the occupancy of each site at the end of the adiabatic evolution for the ED and SD phases in Figs. 3(e) and 3(f), respectively. In the ED (SD) phase, an edge excitation is predicted to exist on the right (left) end of the chain. This feature is indeed observed using the exact solution obtained

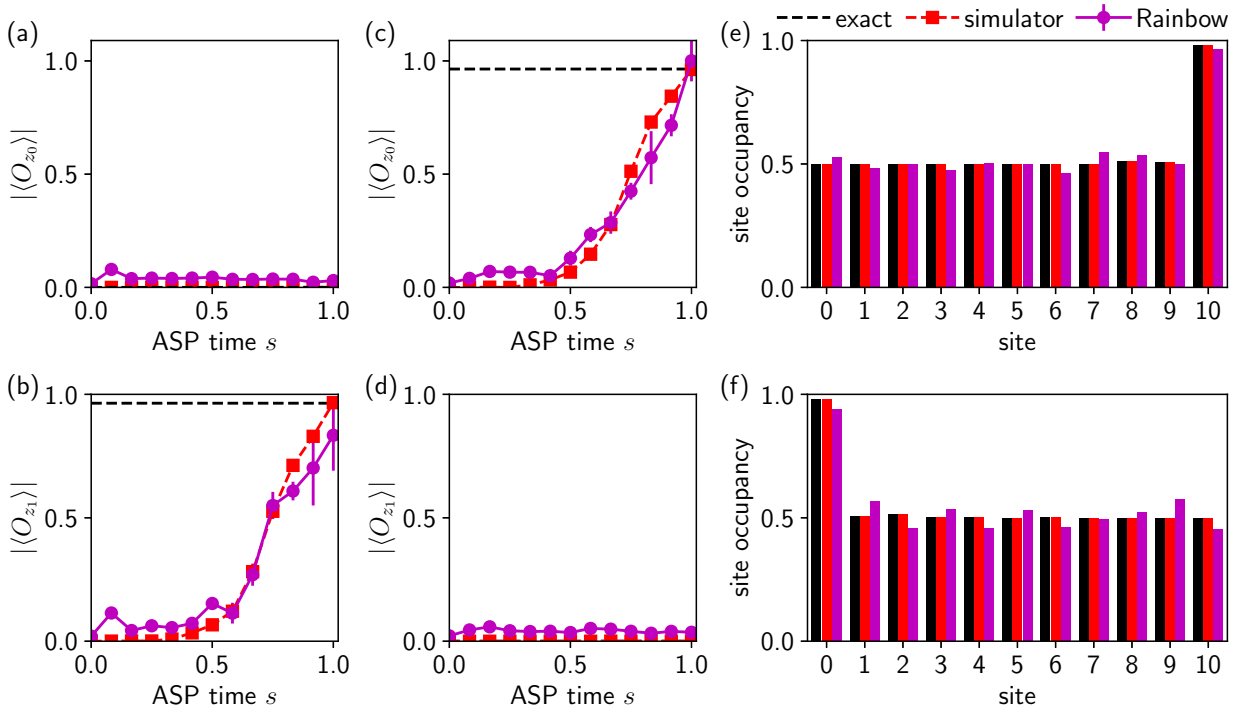

FIG. 3. Preparation of ED and SD phases using 11 qubits on the Rainbow quantum processor. Absolute value of the string order parameters (a) O_{z_0} and (b) O_{z_1} versus ASP time (s) in the ED phase. (c, d) Analogous result for the SD phase. Occupancy of each site at the end of the ASP trajectory for the (e) ED and (f) SD phases. The two SPT phases can be prepared and distinguished clearly by finite or zero string-order parameter and location of edge excitation. The parameters $J_1 = 0.2$, $J_1' = -1.5$, $J_2 = -0.1$, $B_z = 2.5$, $T = 3.0$ were used to prepare the ED phase. The parameters $J_1 = 1.5$, $J_1' = -0.2$, $J_2 = -0.1$, $B_z = 2.5$, $T = 3.0$ were used to prepare the SD phase.

from exact diagonalization. The results from the hardware clearly indicate a difference in the occupancy on the appropriate edge of the chain for each phase and the rest of the chain, with the value in good agreement with the exact result. This observation provides additional evidence that the SPT states prepared on the hardware exhibit the key features expected of these topological phases.

B. Origin of gate depth limitations

The results obtained above required the use of circuit recompilation techniques to reduce the gate depth for ASP to a maximum of around 50 two-qubit gates. Without circuit recompilation, the number of required two-qubit gates was around 170 for seven sites, and the hardware results were in only qualitative agreement with the expected final string-order parameter value. To investigate the origin of this circuit depth limitation, we examined the nonidealities of the two-qubit gates on the Rainbow processor. The most general excitation-number-conserving two-qubit gate, denoted by $U(\theta, \zeta, \chi, \gamma, \phi)$ takes the following form (with the basis states in the order $|00\rangle$, $|01\rangle$, $|10\rangle$, and $|11\rangle$) [15]:

$$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & e^{-i(\gamma+\zeta)}\cos\theta & -ie^{-i(\gamma-\chi)}\sin\theta & 0 \\ 0 & ie^{-i(\gamma+\chi)}\sin\theta & e^{-i(\gamma-\zeta)}\cos\theta & 0 \\ 0 & 0 & 0 & e^{-i(2\gamma+\phi)} \end{pmatrix}. \quad (4)$$

While the ideal native two-qubit gate on Rainbow and Weber is given by $U(\pi/4, 0, 0, 0, 0)^\dagger$, additional interactions lead to nonzero values of ζ, χ, γ, and ϕ. We numerically simulated the effects of these nonidealities on the value of the string-order parameter along the adiabatic trajectory by plotting $|\langle O_{z_1}\rangle|$ versus ASP time s on seven sites for different values of ϕ, γ, ζ, and χ.

Figure 4 shows the string order parameter versus ASP time s for various values of ϕ, γ, ζ, and χ. We also collected data from four different qubit configurations on Weber, a quantum processor with similar specifications as Rainbow, and plot the mean and standard deviations of the string-order parameter. For comparison, we plot the ideal trajectory obtained using QSIM [82]. Comparing the ideal trajectory with data from Weber, we observe a nonmonotonic trend at the end of the trajectory in the hardware data. Similar behavior was observed in the simulator results for various values of ϕ, γ, ζ, and χ. The nonmonotonic trend is observed to be most sensitive to ϕ, and the results with $\phi = \pi/50$ yielded the best qualitative agreement with the hardware results. These observations suggest that the parasitic controlled phase ϕ is a dominant factor in limiting the gate depth of the present simulations.

IV. DISCUSSION AND FUTURE OUTLOOK

We now discuss the implications of our findings regarding the role of the parasitic phase in limiting gate depth for quantum simulation. Error mitigation strategies such as randomized compiling [84] may be applicable to mitigate coherent errors. However, in the present simulations, this protocol cannot be implemented because the two-qubit native gate does not commute with the Pauli group. Other strategies to mitigate coherent gate errors may be possible, but

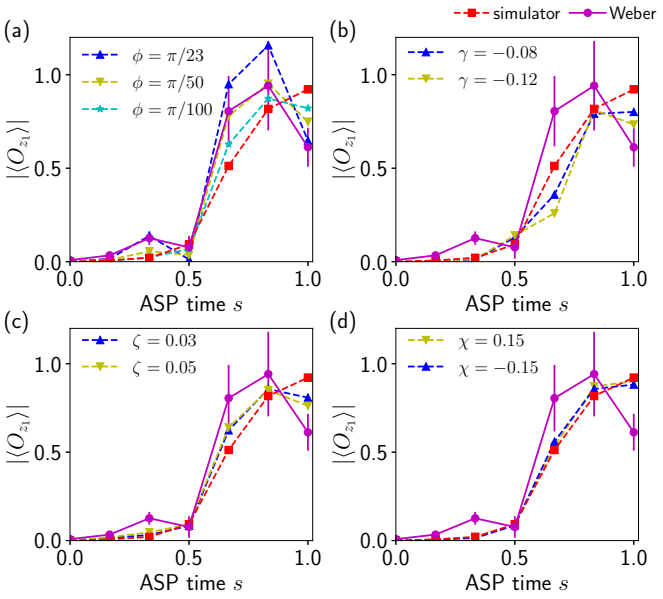

FIG. 4. Effects of gate imperfections on $|\langle O_{z_1}\rangle|$ in the ED phase. Absolute value of the string-order parameters O_{z_1} versus ASP time (s) in the ED phase when (a) ϕ, (b) γ, (c) ζ, and (d) χ are varied. Error bars for the hardware data (Weber) were obtained from four different qubit configurations. The parameter ϕ best explains the observed trend in string-order parameter with s. The parameters $J_1 = 0.2, J_1' = -1, J_2 = -0.1, B_z = 1.5, T = 3.0$ were used to prepare the ED phase.

their effectiveness is, in general, problem-dependent. Several strategies were attempted in this work, but were ultimately unsuccessful (see Appendix B). Supposing that the parasitic phase can be successfully mitigated, emulations using CIRQ indicate that the maximum number of two-qubit gates is around 100 for the present simulations given reported error rates [29], which agrees well with the findings of a recent work which simulated correlated molecules and materials on the same device [85].

Given the capabilities of present quantum processors, we examine the resources required to prepare more complex chiral spin liquids that are thought to exist in a spin-1/2 frustrated honeycomb with similar couplings studied in our work [75,76,86]. For a system size of 20 spins in a hexagonal lattice, corresponding to four unit cells, the total number of two-qubit gates required to implement a single Trotter step of the ASP trajectory is 210. Assuming six Trotter steps are needed in total, 1260 two-qubit gates would therefore be required. This value exceeds our estimate of the achievable gate depth by around an order of magnitude. Our results provide quantitative metrics regarding the improvements needed for future quantum devices to realize more exotic topological phases using ASP.

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TABLE I. Comparison of number of two-qubit gates in target unitary U_{targ} for 12 Trotter steps and in $U_{\text{rec}}(\boldsymbol{\theta})$ for different system sizes.

System size	U_{targ}	$U_{\text{rec}}(\boldsymbol{\theta})$
7	336	30
9	468	40
11	564	50

APPENDIX A: CIRCUIT RECOMPLIATION SCHEME

This Appendix describes the circuit recompilation technique originally introduced in Ref. [42] and which is used to reduce the depth of the circuits implemented on the Rainbow quantum processor. Let the target unitary be U_{targ} and the parameterized circuit be $U_{\text{rec}}(\boldsymbol{\theta})$, where $\boldsymbol{\theta}$ is a composite vector of all the free variables in the parameterized circuit. Given a reduced density operator ρ on the finite domain acted on by the target unitary, the optimal parameterized circuit is found by performing a gradient descent to maximize the function

$$F(\boldsymbol{\theta}) = |\text{Tr}(U_{\text{rec}}(\boldsymbol{\theta})^\dagger U_{\text{targ}}\rho)|^2, \tag{A1}$$

which can be interpreted as the fidelity between $U_{\text{rec}}(\boldsymbol{\theta})$ and U_{targ} with respect to the reduced density matrix ρ. For the purpose of this work, we set $F(\boldsymbol{\theta}) = 0.999$ as the stopping criterion. We compare the number of two-qubit gates present in the target unitary U_{targ} at the end of 12 Trotter steps and in the parameterized circuit $U_{\text{rec}}(\boldsymbol{\theta})$ in Table I. The number of two-qubit gates required decreases by around an order of magnitude with recompilation.

APPENDIX B: PARASITIC CONTROLLED PHASE IN NONRECOMPILED CIRCUITS

This Appendix describes attempted strategies to mitigate the parasitic controlled phase. The first approach constructs $\text{CPHASE}(\psi)$ and appends it to the back of the native gate with $\psi = -\phi$ to compensate for the parasitic phase; that is, we implement $\sqrt{iS}^\dagger_{\text{hardware}}\text{CPHASE}(\psi = -\phi)$. This gate can be constructed exactly by using a series of single-qubit rotations and two $\sqrt{iS}^\dagger_{\text{hardware}}$ to compensate for the phase in each $\sqrt{iS}^\dagger$. By noting that $\sqrt{iS}^\dagger_{\text{hardware}}$ is approximately $\sqrt{iS}^\dagger\text{CPHASE}(\phi)$ for some parasitic phase ϕ, a controlled-phase gate between control qubit i and target qubit j, $\text{CPHASE}(\psi = -\phi)_{ij}$ can be constructed exactly as [87]

$$\begin{aligned}\text{CPHASE}(\psi)_{ij} =& [R_{Z_i}(\pi - \psi/2) \otimes R_{Z_j}(-\psi/2)] \\ & [R_{X_i}(-\xi_i) \otimes R_{X_j}(-\xi_j)] \\ & \sqrt{iS}^\dagger_{\text{hardware},ij} \\ & [R_{Z_i}(\pi + \phi/2) \otimes R_{Z_j}(\phi/2)] \\ & [R_{X_i}(-2\alpha) \otimes \mathcal{I}_j] \\ & \sqrt{iS}^\dagger_{\text{hardware},ij} \\ & [R_{Z_i}(\psi/2) \otimes R_{Z_j}(\psi/2)] \\ & [R_{X_i}(\xi_i) \otimes R_{X_j}(\xi_j)],\end{aligned} \tag{B1}$$

where R_Z, R_X are the single-qubit rotations around the z axis and x axis, and the decomposition parameters α, ξ_i, ξ_j are given by

$$\sin(\alpha) = \sqrt{\frac{\sin^2(\psi/4) - \sin^2(\phi/2)}{\sin^2(\pi/4) - \sin^2(\phi/2)}} \tag{B2}$$

$$\xi_i = \tan^{-1}\left(\frac{\tan(\alpha)\cos(\pi/4)}{\cos(\phi/2)}\right) + \frac{\pi}{2}(1 - \mathrm{sgn}(\cos(\phi/2))), \tag{B3}$$

$$\xi_j = \tan^{-1}\left(\frac{\tan(\alpha)\sin(\pi/4)}{\sin(\phi/2)}\right) + \frac{\pi}{2}(1 - \mathrm{sgn}(\sin(\phi/2))). \tag{B4}$$

The cost of this approach is the addition of two native two-qubit gates for each original two-qubit gate, thereby increasing the gate depth by a factor of 3.

We tested this scheme on Weber by performing Floquet characterization to estimate the parasitic phase ϕ present on each qubit [29], then used the average value to construct a compensated CPHASE($-\phi_{\mathrm{avg}}$) that was appended to the hardware gate $\sqrt{iS}^{\dagger}_{\mathrm{hardware}}$. The results with these compensated circuits are presented in Fig. 5(a). We observe greater deviations from the exact result when the compensated circuits are used. The likely origin of the worse performance is the larger number of two-qubit gates are used in the compensated circuits (510 versus 170 to reach the end of the adiabatic path).

The second approach is based on the observation that the phase present in the $|11\rangle$ can be removed at the expense of adding half the phase to the $|01\rangle$ and $|10\rangle$ using single-qubit Z rotations. Assuming that fidelity is a quadratic function of gate parameters, a higher fidelity can be obtained by splitting the phase into two. We tested this scheme by performing Floquet calibration to estimate the ϕ present on each qubit and used the average to perform single-qubit Z rotations on the qubits. The result is shown in Fig. 5(b). Although some improvement in the final value of the string-order parameter is observed, the nonmonotonic trend remains largely unchanged, indicating that manipulation of the parasitic phase is inadequate to remove the discrepancy.

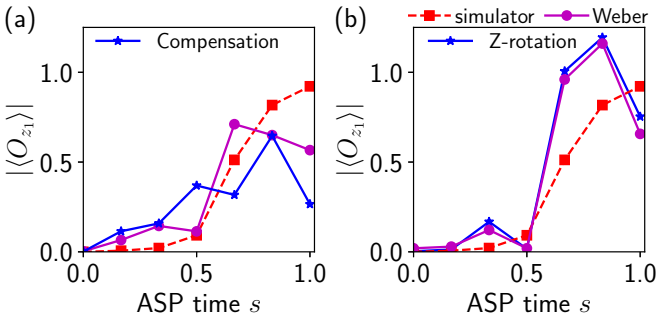

FIG. 5. Attempts to compensate for parasitic controlled phase. Absolute value of the string-order parameters O_{z_1} versus ASP time (s) in the ED phase for circuits with (a) CPHASE(ϕ) appended to each native two-qubit gate to compensate for the parasitic controlled phase; (b) single-qubit Z rotations added to split the parasitic phase among two basis states. The data obtained from Weber and the noiseless data from the simulator are also shown. The qualitative trend of the string-order parameter is qualitatively unchanged by the two strategies. The parameters $J_1 = 0.2$, $J_1' = -1$, $J_2 = -0.1$, $B_z = 1.5$, $T = 3.0$ were used to prepare the ED phase.

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