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An Examination of Power Converter Architectures for Utility-Scale Hybrid Solar Photovoltaic and Battery Energy Storage Systems

THE FEATURES OF SEVERAL POWER CONVERSION ARCHITECTURES

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RECENTLY, THE FALLING COSTS OF PHOTOVOLTAIC (PV) and battery storage (BS) technologies have raised interest in the creation of hybrid PV+BS power plants. Together with increasing energy storage capacity by storing clipped energy, hybrid plants broaden a power plant's grid services

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by featuring fast dispatch flexibility and voltage-ampere reactive support. Although many proposed PV plants are being developed with colocated batteries, the dominant architecture of utility-scale PV+BS power plants is uncertain. Moreover, power architectures are expected to evolve over time based on future trends. The primary goal of this article is to critically examine and compare several dc–dc and dc–ac power converter architectures that are suitable candidates for hybrid PV+BS power plants. In particular, the article presents characteristics of several power conversion architectures from the point of view of power semiconductor requirements, efficiency, reactive component requirements, modularity, control complexity, and so forth. Detailed analytical models are utilized, along with a benchmark design example to present a comparative evaluation of the alternatives for performing engineering tradeoff studies.

A utility-scale PV power plant can comprise several PV modules that connect in series and/or in parallel to form PV strings or PV arrays.

Introduction

The increasing share of intermittent sources of energy such as solar and wind intensifies the need for energy storage technologies such as batteries and pumped-storage hydropower. Although pumped-storage facilities account for nearly 92% of the U.S. energy storage capacity [1], battery energy storage systems are growing quickly [2], [3]. This is due to their high energy densities and smaller size and weight, which leads to added flexibility and ease of installation [4], [5]. More recently, the falling costs of PV and BS technologies have raised interest in the creation of hybrid PV+BS power plants. These technologies are enabled by the development of advanced power electronics with unprecedented functionality, efficiency, reliability, and power density critical for an electrified world economy. According to some estimates, 80% of all U.S. electricity could pass through power electronics devices by 2030 [6]. Further, continuous advancements in control architectures are critical to support electrified systems that present different and challenging characteristics as compared to conventional electrical generators [7], [8], [9].

Most of the utility-scale battery energy storage systems that are expected to come online in the United States from 2021 to 2023 are to be colocated with PV power plants, a change in trends from recent years [10], [11]. Further, considering the interconnection queues in the United States, 34% of the proposed PV plants are being developed with colocated batteries [11]. It may, however, be noted that the dominant architecture for the proposed and future utility-scale PV+BS power plants is highly uncertain. Most of the interconnection queue data do not include information about the inverter characteristics [12], [13]. Moreover, power architectures are expected to evolve over time based on future trends.

Currently, hybrid PV+BS power plants can be broadly classified as either ac grid- or converter-coupled systems based on their point of common coupling. These systems do not share any components and the storage systems can act independent of the PV system. From the perspective of power converter architectures, ac grid-coupled systems are expected to have similar characteristics to independently operated PV and BS plants [13]. On the other hand, in converter-coupled systems, PVs and BSs share the dc–ac grid-connected inverter. This article focuses on converter-coupled configurations for utility-scale hybrid PV+BS power plants because of their distinct characteristics and expected advantages. Further, the design of converter-coupled configurations are more complex and integrated due to the sharing of electronic and control systems and hence requires detailed studies.

Although the growth of hybrid plants is driven by significant declines in project costs due to cost savings by sharing equipment, cutting interconnection, and permitting costs and leveraging federal tax credits [14], there are several other technical advantages as well. First, converter-coupled systems permit the energy storage of otherwise clipped energy that occurs when the inverter loading ratio (ILR) exceeds one. Typically, the ILR varies between one and two and is assumed to be 1.3 in this study, which is equal to the average value for utility-scale PV systems [13]. Further, as the batteries are directly charged from the PV system, converter-coupled systems have higher charging efficiency due to a lower number of power electronic stages. Finally, independent of the point of coupling, hybridization of the PV power plants with BSs broaden the plant's grid services, including fast dispatch flexibility, frequency regulation, and voltage-ampere reactive support. In summary, PV+BS power plants have the potential to offer 1) energy savings by capturing clipped energy from PV panels, 2) higher round-trip efficiency during battery charging times, and 3) improved dispatch flexibility, making them more attractive for grid operations. It must be noted that converter-coupled systems also suffer from challenges compared to ac grid-coupled systems. Due to the highly integrated structure in converter-coupled systems, they are expected to have a higher structural balance of systems due to distributed and smaller battery packs, in comparison to a larger centralized battery pack in colocated ac systems [13].

The primary goal of this article is to critically examine and compare several dc–dc and dc–ac power converter architectures and their control strategies that can

enable converter-coupled hybrid PV+BS power plants. The results from this article are geared toward supporting the current and future planned studies of hybrid PV and battery storage power plants from the point of view of converter designs. The structure of the article is as follows: The "Block Diagram of PV+BS Power Plants" section presents simplified block diagrams of the configurations of hybrid PV+BS systems; the "DC-Stacked Architectures" and "Cascaded Bridge Architectures" sections examine dc-stacked and modular power converter architectures in terms of power semiconductor switch and energy storage element ratings, respectively; the "Control Strategies for Hybrid PV+BS Plants" section discusses the control architectures suitable for the topologies under consideration; the "Double-Star Configuration" section briefly discusses double-star design configurations for hybrid power configurations; the "Results and Discussion" section presents detailed comparative results for a design example; and finally, the "Conclusion" section summarizes the article.

Block Diagram of PV+BS Power Plants

Figure 1 illustrates the simplified block diagram of a converter-coupled hybrid PV+BS power plant. The PV and BS power plants share a common dc–ac grid-connected inverter that connects the two dc systems (i.e., the PV and the BS) to the ac grid. The two dc systems interface to each other, either at the dc or ac node. Figure 1(a) and (b) illustrates block diagrams for dc- and ac-coupled systems, respectively. Based on the coupling-node configuration, galvanic isolation between the dc sources and the ac grid may be at the ac grid or at the converter level, which is discussed later.

The following assumptions about hybrid power plant systems have been made while examining several power converter architectures.

- The hybrid power-transfer capability of the PV+BS plant to the ac grid is P_{inv}. Hence, the dc–ac conversion system is rated for P_{inv}, which is also noted in Figure 1. Here, P_{inv} refers to the power rating of the inverter.
- The ILR is assumed to be 1.3, which is equal to the average value for utility-scale PV systems. Hence, the PV power plant's rated power is $P_{pv} = 1.3 \times P_{inv}$. The BS-rated power is assumed to be P_{batt}. Typically, $P_{batt} \approx 0.5 \times P_{inv}$ in today's hybrid power plants [13]. In summary, the PV and the battery converter are rated for P_{pv} and P_{batt}, respectively.

As hybrid PV+BS power plants become common, the average ILR is expected to increase [13] as more clipped energy can be stored in the BS. Analytical results from the article will still hold true for many purposes, and the tools provided in the article can be used for extended designs. In the remainder of the article, the following notations are commonly used across all the considered power converter architectures: f_s represents the switching frequency; $T_s = 1/f_s$ represents the switching cycle; V_{ac}, I_{ac} represent the root-mean-square (RMS) values of the ac grid-phase voltages and currents; $\hat{V}_{ac}$, $\hat{I}_{ac}$ represent peak values of the ac grid voltages and currents, respectively; f_{ac}, T_{ac} represent the ac grid frequency and time period, respectively; VA represents the voltage × current ratings of the semiconductor switches; and subscript p and b indicate variables for PV and BS, respectively.

DC-Stacked Architectures

Topology and Operation

Three-phase two-level voltage source converters (VSCs) have traditionally been ubiquitous and are the workhorse topology in many applications such as traction inverters, industrial motor drive systems, uninterruptible power supplies, and so on [15], [16]. In fact, two-level VSCs have

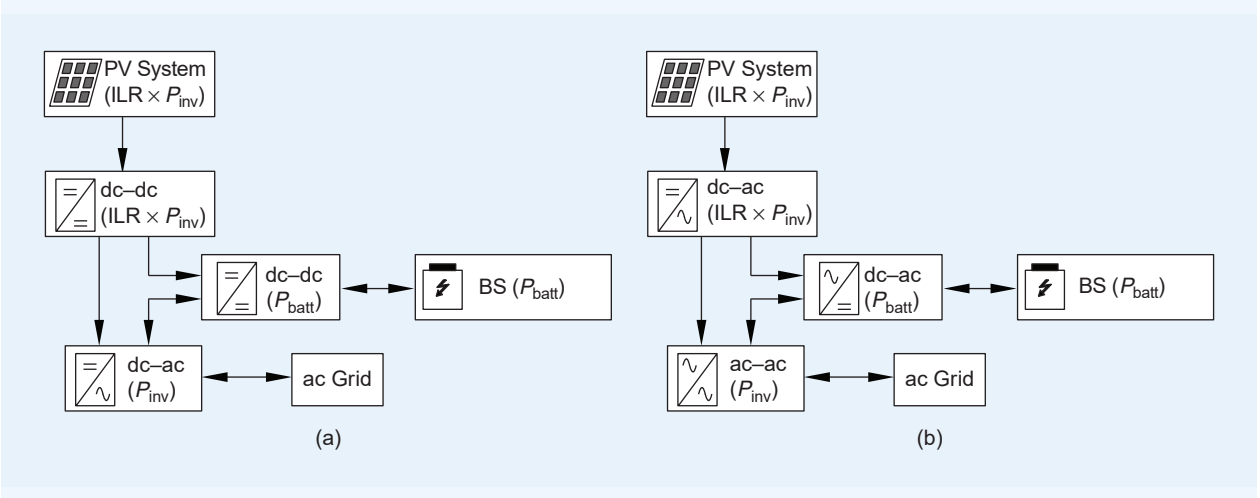

FIGURE 1. A block diagram of converter-coupled PV and BS power plants with (a) a dc-coupled configuration and (b) an ac-coupled configuration. *ILR*: inverter loading ratio.

dominated industrial-scale grid-connected energy storage projects [17], [18]. Further, VSCs offer an architectural solution for hybrid utility-scale power plants. The connection of low-voltage battery and PV systems to the medium-voltage utility grid is enabled by 1) series connection of several low-voltage systems and 2) utilization of a low-frequency step-up transformer, which may be a solid-state-based transformer for increased efficiency and power density.

To provide galvanic isolation, the cascaded bridge architecture can feature a low-frequency transformer at the ac grid or module level.

Figure 2 illustrates the circuit schematic for the solution. Although dc batteries may be directly connected to the dc link, PV systems are typically cascaded via dc–dc converters featuring distributed maximum power point tracking (MPPT) algorithms. In the case of hybrid PV+BS systems, dc–dc converters that interface each of the dc systems with each other and the ac grid play a distinct role in the control of power flow. As the common point of coupling between the PV, BS, and the ac grid converters is dc, this topology is a dc-coupled configuration in Figure 1(a).

Decentralized Converter Architecture Approach

DC energy sources such as PV panels and batteries are all series and/or parallel connections of a basic cell. These cells operate at a low voltage, ranging from less than 1 to 4 V [19], [20]. These low-voltage systems do not interface well with higher-voltage systems and hence, several PV or battery cells are connected in series to form a PV module or a BS.

Considering PV module technologies, PV modules can be categorized into three categories: 1) high-voltage (≈ 240 V) amorphous silicon modules, 2) medium-voltage (≈ 60 V) amorphous silicon modules, and 3) low-voltage multicrystalline silicon modules (≈ 30 V) [21]. A utility-scale PV power plant can comprise several PV modules that connect in series and/or in parallel to form PV strings or PV arrays. Traditional PV power plants feature a central dc–dc converter that cascades to a grid-connected dc–ac inverter for power transport. The dc–dc converter implements the MPPT algorithm to maximize energy yield. In contrast to central dc–dc converters, distributed dc–dc converters are growing quickly due to several advantages, including energy-yield improvements during shading, module mismatch, elimination of single-point failure, and added monitoring and diagnostics. Literature studies indicate that an energy-yield gain of 4–12% can be obtained for distributed systems over central inverter systems [21], [22], [23]. The distribution of dc–dc converters, along with the MPPT controllers associated with them for dc-stacked architectures can be one of the following: 1) a multistring, 2) string, or 3) module distribution. In the case of large utility-scale installations (beyond 100 kW), the prospect of a per-module power converter is limited [21], [23]. Large-scale installations feature improved module-level uniformity, in contrast to residential or commercial rooftop installations. Further, the additional part count, monitoring and installation time, and cost-effectiveness are disadvantages to per-module power electronics in large installations. Hence, this article assumes the distribution of dc–dc converters at the string level for PV systems.

Several strings interface to the dc link using dc–dc converters while implementing MPPT algorithms to maximize energy yield. String-level dc–dc converter systems, which integrate into the utility-scale grid, can feature a boost or buck-boost converter configuration [22], [24]. Similarly, based on the voltage class of the battery energy storage, dc–dc converters can feature either a boost or buck-boost configuration, as detailed next. Due to the presence of a low-frequency transformer between the ac converter and ac grid, an isolated dc–dc converter configuration may not be necessary. On the other hand, ac-coupled PV+BS systems will typically feature transformer-coupled converters, as discussed in the "Cascaded Bridge Architectures" section. This article considers nonisolated dc–dc converters for dc-stacked architectures.

The remaining sections discuss voltage × current (VA) ratings of the semiconductor components and the energy storage ratings of the inductors and capacitors that together play a key role in determining the efficiency, power density, cost, and reliability of the architectures.

VA Ratings of Semiconductor Components

The VA ratings that are imposed by the converter design and operation assist in the selection of power semiconductor devices for the converter design. Here, the VA rating calculation incorporates the peak voltage stresses and RMS current values on the devices.

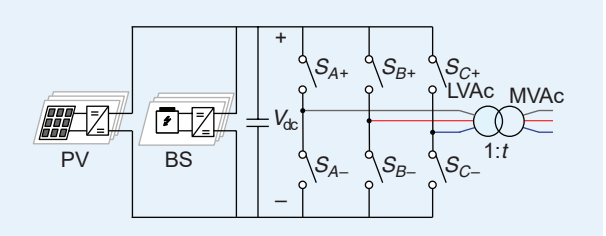

FIGURE 2. The converter topology of a three-phase two-level VSC with cascaded BSs, and cascaded PV systems connected to the dc link.

DC–ac Grid Inverter

DC-link voltage utilization is determined by modulation strategies [15]. Hence, selection of the modulation strategy plays a role in determining the final VA ratings of semiconductor switches. The effect of the modulation strategy is characterized in the article using a duty-ratio factor d_m, where subscript m refers to the term *modulation*. The set of equations (1) characterize the VA rating of the solid-state switches S_{k+} and S_{k-}, where $k = A, B, C$.

$$\begin{aligned} V^{1-\mathrm{SW}} &= V_{\mathrm{dc}} = \frac{1}{t}\frac{V_{\mathrm{ac}}}{d_m} \\ I^{1-\mathrm{SW}} &= t \times \frac{I_{\mathrm{ac}}}{\sqrt{2}} \\ n &= 6 \\ \mathrm{VA} &= \frac{\sqrt{2}P_{\mathrm{inv}}}{d_m} \end{aligned} \tag{1}$$

where $V^{1-\mathrm{SW}}$ and $I^{1-\mathrm{SW}}$ represent the peak voltage and RMS current ratings, respectively, imposed on a single switch; n represents the total number of switches; P_{inv} represents the total power throughput from dc to the three-phase ac system (and is equal to the dc–ac inverter rating in Figure 1); and t represents the low-frequency transformer turns ratio. Based on the modulation strategy, the factor d_m can be determined. Equation set (2) documents the advantage of using space-vector modulation (SVM) over sine-pulsewidth modulation (PWM) in reducing the VA ratings of the switches.

$$d_m = \frac{1}{t}\frac{V_{\mathrm{ac}}}{V_{\mathrm{dc}}} = \begin{cases} \le \dfrac{1}{2\sqrt{2}}, & \mathrm{Sine-PWM} \\ \le \dfrac{1}{\sqrt{6}}, & \mathrm{SVM} \end{cases}. \tag{2}$$

The utilization of SVM results in higher link voltage utilization, which also results in optimizing the size of energy storage elements (which is discussed next). Note that the effect of the transformer turns ratio does not feature explicitly in the final VA calculation output as the transformer operation is considered lossless.

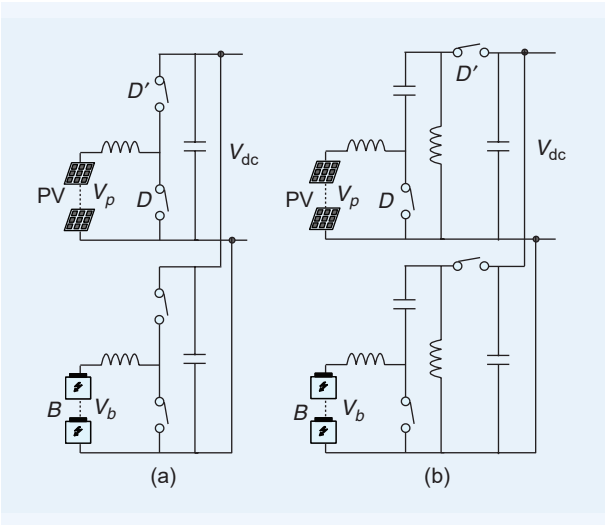

FIGURE 3. Common dc–dc converter topologies used to control the power flow between PV modules, batteries, and the dc–ac grid-tied inverter. (a) A boost configuration and (b) buck-boost configuration.

DC–DC Converter

In theory, any unidirectional and bidirectional dc–dc converter can be used for integration of the PV systems and the BSs, respectively. However, as the two dc systems interface with the utility-scale ac grid, only boost or buck-boost configurations are considered in the article. Availability of the boost mode of operation helps reduce the number of series-connected PV modules or BSs, thus potentially extending life expectancy and mismatch issues [25], [26].

Several power conversion topologies are proposed in the literature. This article examines the following configurations for a detailed analysis: 1) a simple-boost converter, 2) buck-boost converter, 3) single-ended primary-inductor converter (SEPIC), and 4) Ćuk converter. Figure 3 illustrates circuit schematics of the boost and SEPIC topologies. Equation (3) characterizes the ratio of the input to the output dc voltage ($V_{p/b}/V_{\mathrm{dc}}$) in terms of the duty ratios, where $V_{p/b}$ refers to the PV/BS voltage, and V_{DC} refers to the dc-link voltage.

$$\frac{V_{p/b}}{V_{\mathrm{dc}}} = \begin{cases} D', & \mathrm{Boost} \\ \dfrac{D'}{D}, & \mathrm{Buck\ boost, SEPIC, \acute{C}uk} \end{cases} \tag{3}$$

and D refers to the duty ratio of the switches, as annotated in Figure 3, and $D' = 1 - D$ refers to the complementary duty ratio. Using the duty-ratio expressions, the per-unitized VA ratings of the power semiconductor switches can be derived for the four dc–dc converters, which are also summarized in (4).

$$\mathrm{VA\ per\ unit\ (p.u.)} = \begin{cases} \dfrac{\sqrt{D}+\sqrt{D'}}{D'}, & \mathrm{Boost} \\ \dfrac{\sqrt{D}+\sqrt{D'}}{DD'}, & \mathrm{Buck\ boost, SEPIC, \acute{C}uk} \end{cases}. \tag{4}$$

It may be noted that the VA rating is a function of the operating point of the converter and may vary significantly as a function of the voltage-transfer ratio ($V_{p/b}/V_{\mathrm{dc}}$). Figure 4 plots the per-unitized VA rating of the switching devices as a function of the voltage-transfer ratio ($V_{p/b}/V_{\mathrm{dc}}$) for the simple-boost converter and the three-buck/boost topologies under discussion.

Although a simple-boost converter features the lowest VA rating for the power semiconductor devices, it will not offer the buck mode of operation. In contrast, the other converters offer the buck mode of operation with a device VA rating as a tradeoff. Hence, unless required by the PV, battery, or dc-link specifications, boost configuration may be an ideal choice as buck-boost configurations suffer from additional device stresses.

Battery/PV Energy Storage Ratings

DC–AC Grid Inverter

To filter the switching action of the six semiconductor switches, the topology typically features a dc-link capacitor and an input inductor to smoothen the dc-link voltage and input current, respectively. Equation (5) characterizes the capacitor size, which is a function of the current magnitude, modulation strategy, and the allowed ripple voltage at the dc link ($r_{V_{dc}}$).

$$C_{\text{link}} \approx \frac{\hat{I}_{\text{ac}} \times \hat{d}_{0-\text{dc}} T_S}{r_{V_{\text{dc}}}} \tag{5}$$

where $\hat{d}_{0-\text{dc}}$ represents the maximum value of the dc-side zero-state duty ratio when only the peak ac current ($\hat{I}_{\text{ac}}$) flows into the capacitor. Due to the buck mode of operation from the dc to the ac side, ac-side currents will be of higher magnitude. Hence, the capacitor ripple calculation features the peak value of the ac current during the freewheeling duration of the dc current when the net capacitor current is not offset by the dc current. Note that the dc- and ac-side switches may be operating at a different switching frequency and may not be synchronized.

Similarly, (6) characterizes the net size of the filter inductance to limit the ripple in the dc current ($r_{I_{\text{dc}}}$).

$$L_{\text{Batt}} = \frac{r_{V_{\text{dc}}} \times \hat{d}_{0-\text{ac}} T_S}{4 r_{I_{\text{dc}}}} \tag{6}$$

where $\hat{d}_{0-\text{ac}}$ represents the maximum value of the ac-side zero-state duty ratio when only the peak dc current flows into the capacitor. In summary, it can be observed that in the case of dc-stacked topologies, energy storage elements are sized to filter-switching harmonics, which is in contrast to some power architectures that require low-frequency filtering, as discussed later. These energy storage elements may be incorporated within the dc–dc converter stage. The "Results and Discussion" section demonstrates the performance of such dc-stacked topologies using a design example.

DC–dc Converter

Table 1 tabulates filter-sizing equations in terms of the duty ratios (D or $D' = 1 - D$), switching frequency (f_s), per-unit ripple (r), and the PV/BS or the dc-side impedance ($Z_x = V_x/I_x$ where $x = p, b$, or dc). Note that the subscript p/b in the table refers to the dc–dc converter variables for the PV and the BS system and subscript dc refers to the dc current at the V_{dc} terminals. Unlike the other buck/boost converters, the output voltage polarity of the input and output sides remain the same in an SEPIC converter. On the other hand, a Ćuk converter has nonpulsating currents, both at the input and output. Together with minimal VA ratings, a boost converter features the lowest energy storage and filtering requirements.

Efficiency Calculations

The article presents analytical models to quantify and compare efficiency of the power electronic architectures under discussion by characterizing the RMS and average current calculations in the semiconductor switching devices, transformers, and the filtering and energy storage elements. Table 2 summarizes the current expressions for loss calculations for the dc–dc conversion stage in terms of the duty ratios. For switching-loss calculations, the switching energies provided by the data sheets for the reference operating conditions are employed (characterized by k_{SW} in the equations and defined in "Loss Calculations"). The switching-loss equation per switch for dc–dc converters is given by (7).

$$P_{\text{sw}} = \begin{cases} k_{\text{sw}} V_{\text{dc}} I_{p/b}, & \text{Boost} \\ k_{\text{sw}} V_{p/b+\text{dc}} I_{p/b+\text{dc}}, & \text{Buck boost, SEPIC, Ćuk} \end{cases} \tag{7}$$

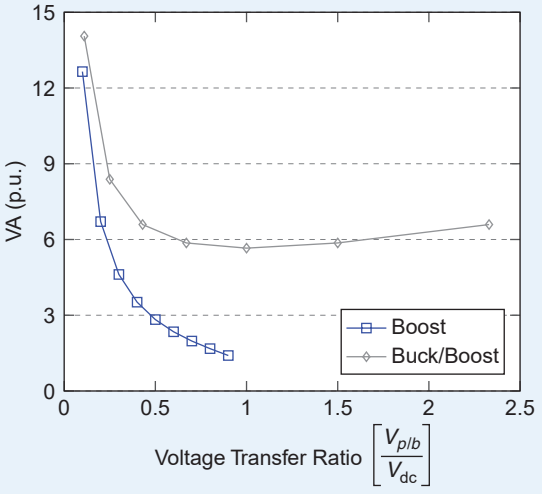

FIGURE 4. A plot of the per-unitized VA rating of the total power semiconductor devices as a function of the voltage-transfer ratio.

Table 1. The sizing of filtering elements in dc–dc converters

Topology	PV/BS	DC Link	Intermediate
Boost	$L = \frac{DZ_{p/b}}{rf_S}$	$C = \frac{D}{rf_S Z_{\text{dc}}}$	—
Buck boost	$C = \frac{D'}{rf_S Z_{p/b}}$	$C = \frac{D}{rf_S Z_{\text{dc}}}$	$L = \frac{DV_{p/b}}{rf_S I_{p/b+dc}}$
SEPIC	$L = \frac{DZ_{p/b}}{rf_S}$	$C = \frac{D}{rf_S Z_{\text{dc}}}$	$C = \frac{DI_{\text{dc}}}{rf_S V_{p/b}}$ $L = \frac{D'Z_{\text{dc}}}{rf_S}$
Ćuk	$L = \frac{DZ_{p/b}}{rf_S}$	$L = \frac{D'Z_{\text{dc}}}{rf_S}$	$C = \frac{DI_{\text{dc}}}{rf_S V_{p/b+\text{dc}}}$

where $V_{p/b+\text{DC}} = V_{p/b} + V_{\text{dc}}$ and $I_{p/b+\text{DC}} = I_{p/b} + I_{\text{dc}}$

The ac inverter conduction losses are given by (8) and (9) for uniformly distributed zero vectors.

$$I_{\text{avg}} = \begin{cases} \hat{I}_{\text{ac}}\left[\frac{1}{2\pi} + \frac{M}{8}\cos\phi\right], & \text{transistor} \\ \hat{I}_{\text{ac}}\left[\frac{1}{2\pi} - \frac{M}{8}\cos\phi\right], & \text{diode} \end{cases} \tag{8}$$

$$I_{\text{RMS}} = \begin{cases} \hat{I}_{\text{ac}}\sqrt{\frac{1}{8} + \frac{M}{3\pi}\cos\phi}, & \text{transistor} \\ \hat{I}_{\text{ac}}\sqrt{\frac{1}{8} - \frac{M}{3\pi}\cos\phi}, & \text{diode} \end{cases} \tag{9}$$

$$P_{\text{sw}} = \left\{ k_{\text{sw}} V_{\text{dc}} \frac{2}{\pi} \hat{I}_{\text{ac}}, \quad \text{per inverter leg} \right. \tag{10}$$

where M represents the modulation index, and ϕ represents the phase angle. The equations hold for sine-PWM and SVM with reasonable approximations [27]. Finally, the switching-loss equation per one leg for dc–ac converters is given by (10), where the dc output-equivalent current is the average of one-half sine wave.

Cascaded Bridge Architectures

In contrast to dc-stacked topologies wherein the dc sources/loads are connected in series and interfaced to the ac grid using a single inverter, modular topologies feature smaller inverters that interface the several dc sources/loads to the ac grid. Several converters cascade in series to interface low-voltage dc sources to the ac grid. To provide galvanic isolation, the cascaded bridge architecture can feature a low-frequency transformer at the ac grid or module level. The "Cascaded Bridge Topology With a Low-Frequency Grid Transformer," "Triple-Active Bridge With a Three-Winding High-Frequency Transformer Topology," and "TAB With a Five-Winding High-Frequency Transformer Topology" sections present detailed examinations of the two approaches.

Cascaded Bridge Topology With a Low-Frequency Grid Transformer

This section benchmarks the cascaded bridge converter (CBC) topology suitable for hybrid power plants. Figure 5 illustrates the circuit topology featuring p PV systems and b BSs. For simplicity, $p = b$. The several dc systems connect to the ac grid via several nonisolated dc–dc and dc–ac converters and enable voltage compatibility via series connection of smaller converters. Although the ac grid transformer may provide a step-up function, the primary purpose is to provide galvanic isolation between the dc sources and the ac grid. As the common point of coupling between the PV, BS, and ac grid converters is dc, this topology is a dc-coupled configuration in Figure 1(a). The next few sections characterize the ratings of the semiconductor components and energy storage elements within this modular CBC.

VA Ratings of Semiconductor Components

The dc–dc converter topologies discussed in the "DC–dc Converter" section can be utilized to interface the PV and the BS systems to the dc point of coupling. The following analysis assumes a full-bridge (FB) converter for dc–ac conversion to the grid and is the main focus of this section. Similar to a dc-stacked topology, the total VA rating is a function of the modulation strategy. However, in contrast, the VA ratings of a single switch is scaled based on the level of modularity represented by p for PV systems and b for BSs. The set of equations (11) that characterize per-switch and total VA ratings for the topology are

$$\begin{aligned} V^{1-\text{SW}} &= \begin{cases} \frac{V_{\text{ac}}}{2 \times p \times d_m}, & \text{PV} \\ \frac{V_{\text{ac}}}{2 \times b \times d_m}, & \text{BS} \end{cases} \\ I^{1-\text{SW}} &= \frac{I_{\text{ac}}}{\sqrt{2}} \\ n^{\text{SW}} &= 4 \times 3 \\ \text{VA}^{\text{SW}} &= \frac{\sqrt{2}\, P_{\text{inv}}}{d_m} \end{aligned} \tag{11}$$

where the modulation factor d_m is defined similar to the dc-stacked topologies discussed in (2) in the "DC–dc Converter" section, and the factor of two represents the

Table 2. RMS and average current expressions for dc–dc converters useful for loss calculations

	I_{RMS}						I_{avg}	
			Filtering		Energy Storage			
Topology	Switch 1	Switch 2	L	C	L	C	Switch 1	Switch 2
Boost	$\sqrt{D}\, I_{p/b}$	$\sqrt{D'}\, I_{p/b}$	$I_{p/b}$	$\sqrt{D}\sqrt{D'}\, I_{p/b}$	—	—	$DI_{p/b}$	$D'I_{p/b}$
Buck boost	$\sqrt{D}\, I_{p/b+\text{dc}}$	$\sqrt{D'}\, I_{p/b+\text{dc}}$	—	$\frac{\sqrt{D'}}{\sqrt{D}} I_{p/b}$	$I_{p/b+\text{dc}}$	—	$DI_{p/b+dc}$	$D'I_{p/b+dc}$
SEPIC	$\sqrt{D}\, I_{p/b+\text{dc}}$	$\sqrt{D'}\, I_{p/b+\text{dc}}$	$I_{p/b}$	$\frac{\sqrt{D'}}{\sqrt{D}} I_{p/b}$	I_{DC}	$\frac{\sqrt{D'}}{\sqrt{D}} I_{p/b}$	$DI_{p/b+dc}$	$D'I_{p/b+dc}$
Ćuk	$\sqrt{D}\, I_{p/b+\text{dc}}$	$\sqrt{D'}\, I_{p/b+\text{dc}}$	$I_{p/b}, I_{\text{DC}}$	—	—	$\frac{\sqrt{D'}}{\sqrt{D}} I_{p/b}$	$DI_{p/b+dc}$	$D'I_{p/b+dc}$

Loss Calculations

The transistor and diode conduction losses can be calculated using an approximation with a series connection of the dc voltage drop representing the on-state voltage drop (v_{on}) and the on-state resistance (r_{on}), as illustrated in (S1).

$$P_c = v_{on} I_{avg} + r_{on} I_{rms}^2 \tag{S1}$$

where v_{on} is the on-state collector-emitter voltage (v_{ce}), drain-source voltage (v_{ds}), or forward voltage (v_f), in the case of IGBTs, MOSFETs, or diodes, respectively. The switching loss is characterized by the switching-loss energy associated with each switching event and is typically assumed to be proportional to the blocking voltage and the conducting current at the instant of switching event. Equation (S2) characterizes the switching loss associated with one half bridge during a switching cycle.

$$P_{sw} = \underbrace{f_{SW} \frac{(E_{onT} + E_{offT} + E_{rrD})}{V_R I_R}}_{k_{sw}} V_{op} I_{op} \tag{S2}$$

where E_{onT}, E_{offT}, and E_{rr} represent the energy loss during transistor turn on, transistor turn off, and diode reverse-recovery event, respectively. The switching energy loss values are provided in the manufacturer's data sheet at reference current (I_R) and voltage (V_R) operating conditions. Hence, the switching energies are normalized at V_R, I_R to derive the switching losses under the operating conditions imposed by the circuit operation V_{op}, I_{op}.

Converter Parameter Details for Efficiency Calculations

Table S1 lists the converter parameters along with selected device parameters for the design example under consideration, with a power level of $P_{pv} = 1.3$ per unit (p.u.), $P_{batt} = 0.3$ p.u., and $P_{ac} = 1$ p.u., as discussed in the "Results and Discussion" section. The results obtained from the simulations and the analytical equations are listed. Due to the similarity between three-winding triple-active bridge (3-W TAB) and five-winding (5-W) TAB designs, the 5-W TAB is excluded from the table.

Table S1. Converter design details for efficiency calculations

	Simulation Results	Analytical results	Loss Parameters
DC-Stacked With Boost dc–dc (Per Converter)			
Photovoltaic (PV) dc–dc Converter Quantity: One			
rms(I_T) avg(I_T) peak(I_T)	3.07 kA 1.94 kA 4.9 kA	3.08 kA 1.95 kA 4.88 kA	$v_{ce} = 0.6$ V, $r_{dson} = 0.22$ mΩ; $E_{on} = 0.9$ J, $E_{off} = 1.5$ J at $V_R = 600$ V, $I_R = 4.8$ kA [52]
rms(I_D) avg(I_D) peak(I_D)	3.76 kA 2.91 kA 4.9 kA	3.78 kA 2.92 kA 4.88 kA	1.5 in $v_f = 1.32$ V, $r_{don} = 0.268$ mΩ; $E_{rr} = 0.1$ J at $V_R = 400$ V, $I_R = 1.5$ kA, $di/dt = 100$ A/μs [53]
Battery dc–dc Converter Quantity: One			
rms(I_T) avg(I_T) peak(I_T) rms(I_D) avg(I_D) peak(I_D)	0.84 kA 0.68 kA 1.07 kA 0.61 kA 0.36 kA 1.07 kA	0.84 kA 0.68 kA 1.07 kA 0.61 kA 0.36 kA 1.07 kA	[T:] $v_{ce} = 0.6$ V, $r_{dson} = 0.41$ mΩ; $E_{on} = 0.33$ J, $E_{off} = 0.4$ J at $V_R = 600$ V, $I_R = 1.8$ kA [D:] $v_f = 0.6$ V, $r_{don} = 0.3$ mΩ; $E_{rr} = 0.15$ J at $V_R = 600$ V, $I_R = 1.8$ kA [54]
DC–ac Converter Quantity: Six			
rms(I_T) avg(I_T) peak(I_T) rms(I_D) avg(I_D) peak(I_D)	1.56 kA 0.9 kA 3.45 kA 0.58 kA 0.16 kA 3.45 kA	1.57 kA 0.9 kA 3.34 kA 0.58 kA 0.16 kA 3.34 kA	[T:] $v_{ce} = 0.6$ V, $r_{dson} = 0.31$ mΩ; $E_{on} = 0.65$ J, $E_{off} = 0.8$ J at $V_R = 600$ V, $I_R = 3.2$ kA [D:] $v_f = 0.7$ V, $r_{don} = 0.26$ mΩ; $E_{rr} = 0.21$ J at $V_R = 600$ V, $I_R = 3.2$ kA [55]
Cascaded Bridge With Boost dc–dc and Full-Bridge dc–ac (Per Module)			
PV dc–dc Converter Quantity: Three			
rms(I_T) avg(I_T) peak(I_T)	0.58 kA 0.37 kA 0.94 kA	0.59 kA 0.37 kA 0.93 kA	$v_{ce} = 0.7$ V, $r_{dson} = 2.2$ mΩ; $E_{on} = 35$ mJ, $E_{off} = 80$ mJ at $V_R = 600$ V, $I_R = 0.8$ kA [56]
rms(I_D) avg(I_D) peak(I_D)	0.71 kA 0.55 kA 0.94 kA	0.72 kA 0.56 kA 0.93 kA	$v_f = 1.53$ V, $r_{don} = 0.55$ mΩ; $E_{rr} = 80$ mJ at $V_R = 400$ V, $I_R = 1$ kA, $di/dt = 100$ A/μs [57]

(*Continued*)

Table S1. Converter design details for efficiency calculations (*Continued*)

	Simulation Results	Analytical results	Loss Parameters
Battery dc–dc Converter Quantity: Three			
rms(I_T)	0.16 kA	0.16 kA	[T:] v_{ce} = 0.6 V, r_{dson} = 4.7 mΩ; E_{on} = 25 mJ, E_{off} =15 mJ at V_R = 600 V, I_R = 0.3 kA [D:] v_f = 0.7 V, r_{don} = 2.2 mΩ; E_{rr} =15 mJ at V_R = 600 V, I_R = 0.3 kA [58]
avg(I_T)	0.13 kA	0.13 kA	
peak(I_T)	0.21 kA	0.2 kA	
rms(I_D)	0.12 kA	0.12 kA	
avg(I_D)	69 A	69 A	
peak(I_D)	0.21 kA	0.2 kA	
DC–ac Converter Quantity: 12			
rms(I_T)	0.49 kA	0.49 kA	[T:] v_{ce} = 0.5 V, r_{dson} =1.2 mΩ; E_{on} = 50 mJ, E_{off} = 90 mJ at V_R = 600 V, I_R = 0.6 kA [D:] v_f = 0.85 V, r_{don} =1 mΩ; E_{rr} = 52 mJ at V_R = 600 V, I_R = 0.6 kA [59]
avg(I_T)	0.26 kA	0.28 kA	
peak(I_T)	1.1 kA	1.1 kA	
rms(I_D)	0.21 kA	0.21 kA	
avg(I_D)	62 A	63 kA	
peak(I_D)	1.1 kA	1.1 kA	
3-W TAB (Per Module)			
PV dc–dc Converter Quantity: 12			
rms(I_T)	0.75 kA	0.74 kA	[T:] v_{ce} = 0.7 V, r_{dson} = 2.2 mΩ; [D:] v_f =1.53 V, r_{don} = 0.55 mΩ; [56]
avg(I_T)	0.49 kA	0.49 kA	
peak(I_T)	1.3 kA	1.2 kA	
rms(I_D)	0.14 kA	0.14 kA	
avg(I_D)	27 A	27 A	
peak(I_D)	1.3 kA	1.2 kA	
Battery dc–dc Converter Quantity: 12			
rms(I_T)	11 A	13 A	[T:] v_{ce} = 0.6 V, r_{dson} = 4.7 mΩ; [D:] v_f = 0.7 V, r_{don} = 2.2 mΩ; [58]
avg(I_T)	0.9 A	1.2 A	
peak(I_T)	0.2 kA	0.2 kA	
rms(I_D)	0.14 kA	0.14 kA	
avg(I_D)	99 A	97 A	
peak(I_D)	0.2 kA	0.2 kA	
AC–dc Converter (Bridge 2) Quantity: 12			
rms(I_T)	52 A	59 A	[T:] v_{ce} = 0.5 V, r_{dson} =1.2 mΩ; [D:] v_f = 0.85 V, r_{don} =1 mΩ; [59]
avg(I_T)	8 A	9 A	
peak(I_T)	0.51 kA	0.53 kA	
rms(I_D)	0.33 kA	0.34 kA	
avg(I_D)	0.22 kA	0.23 kA	
peak(I_D)	0.51 kA	0.53 kA	
DC–ac Converter (Bridge 3) Quantity: 12			
rms(I_T)	0.49 kA	0.49 kA	[T:] v_{ce} = 0.5 V, r_{dson} =1.2 mΩ; E_{on} = 50 mJ, E_{off} = 90 mJ at V_R = 600 V, I_R = 0.6 kA [D:] v_f = 0.85 V, r_{don} =1 mΩ; E_{rr} = 52 mJ at V_R = 600 V, I_R = 0.6 kA [59]
avg(I_T)	0.28 kA	0.28 kA	
peak(I_T)	1.1 kA	1.1 kA	
rms(I_D)	0.21 kA	0.21 kA	
avg(I_D)	63 A	63 A	

rms: root mean square; avg: average; 3-W TAB: three-winding triple-active bridge.

FB configuration. It is noted that the voltage scaling at the PV or BSs considers the assumptions discussed in the "Block Diagram of PV+BS Power Plants" section. The PV and the BSs can interface to the modular dc–ac converters by employing any of the nonisolated dc–dc topologies discussed in the "DC–dc Converter" section. The "Results and Discussion" section presents a design example that compares the dc-stacked architectures with the cascaded bridge architecture.

Battery/PV Energy Storage Ratings

It may be observed that the modular dc–ac converters in Figure 5 have to be sized to filter single-phase ac power requirements. This is in contrast to dc-stacked topologies, which only need to filter high switching-frequency components. Equation (12) characterizes the capacitor size at the module level, which is now a function of the ac current value, power cycle frequency, and allowed ripple at the dc link ($r_{V_{dc}}$).

$$C_{link} = \frac{2}{\pi} I_{dc} \frac{T_{ac}}{4} \frac{1}{r_{V_{dc}}} \tag{12}$$

where the factor of four in the denominator accounts for a second-harmonic ripple from the FB dc–ac converter, and $(2/\pi)I_{dc}$ represents the average value of the mean current flowing into the dc–ac converter. In the case of a cascaded boost converter at the dc link, $I_{dc} = (2/\pi)I_{dc}(1 - D)$. The switching frequency is considered high in comparison to the ac power frequency, and hence, the ripple due to the switching action is ignored. Similarly, (13) characterizes the net size of a series filter inductance to limit the ripple current from the dc source ($r_{I_{dc}}$).

$$L_s = \frac{2}{\pi} r_{V_{dc}} \frac{T_{ac}}{4} \frac{1}{r_{I_{dc}}} \tag{13}$$

where the factor of $2/\pi$ accounts for the average value of the ripple voltage across the inductor. In summary, energy storage elements will be bulkier in the case of the cascaded bridge architecture as compared to dc-stacked topologies due to the design architecture. Together with the dc-link capacitor, the filtering elements at the dc source will be sized to limit the single-phase ac ripple from the dc–ac inverter, as illustrated in (13).

Efficiency Calculations

The analytical equations presented in the "Efficiency Calculations" section can be extended and utilized for loss calculations in the dc–dc and dc–ac converters for CBCs (7)–(10). The "Results and Discussion" section presents comparative results for the design example under discussion.

Triple-Active Bridge With a Three-Winding High-Frequency Transformer Topology

This section examines a modular triple-active bridge (TAB) converter that connects the dc sources to the ac grid via a dc–ac–ac converter and a high-frequency transformer, as illustrated in Figure 6. Several TABs connect in series to form a modular converter capable of connecting several dc systems to the utility-scale ac grid. The PV systems and the BSs interface to the converter via a high-frequency transformer [28], [29].

In contrast to dc-stacked topologies or a CBC, a three-winding (3-W) TAB features a high-frequency transformer as part of the design architecture and provides galvanic isolation between the PV systems, BSs, and the utility-scale ac grid at the module level. As the common point of coupling between the PV, BS, and the ac grid converters is ac, this topology is an ac-coupled configuration in Figure 1(b). The next few sections characterize the ratings of the semiconductor components and energy storage elements within the modular TAB converters.

VA Ratings of Semiconductor Components

This section presents a systematic approach for the derivation of the VA ratings for the cascaded 3-W TAB topology in a step-by-step manner, as detailed further. Figure 7 illustrates a single 3-W TAB module fed from a PV system and a BS. Here, the two dc systems are integrated into a single-phase

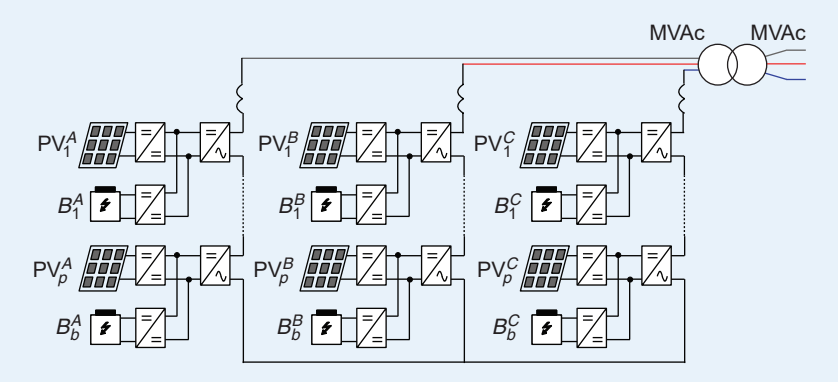

FIGURE 5. The converter topology of a three-phase cascaded half- (or full-) bridge converter with both BSs and PV systems connected to modular dc–ac converters.

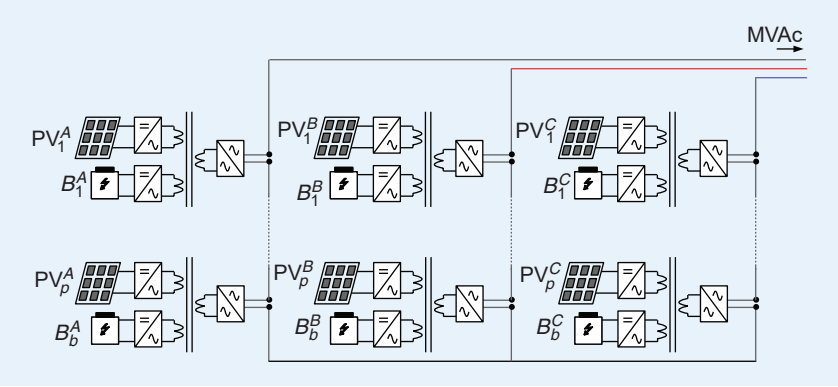

FIGURE 6. The converter topology of a three-phase cascaded TAB converter with both BSs and PV systems connected to modular dc–ac–ac converters via a 3-W transformer.

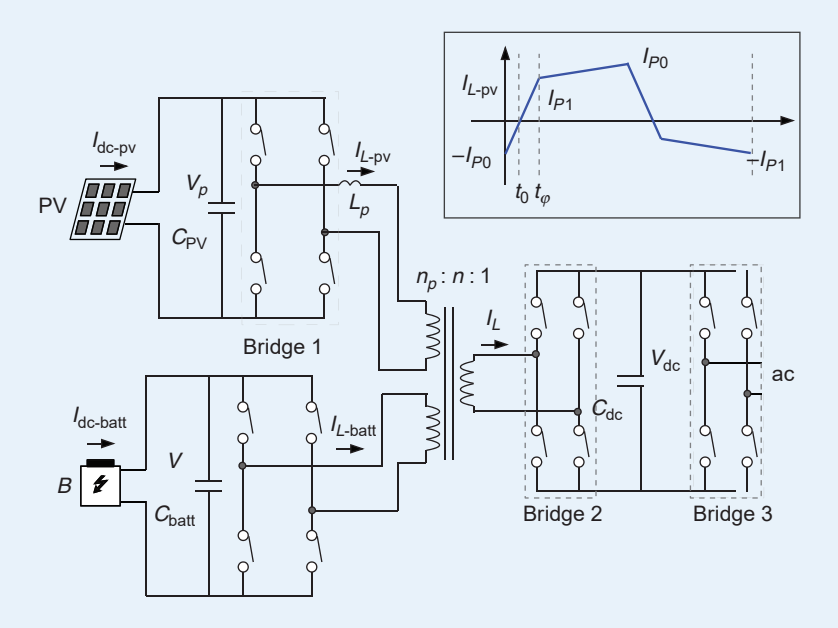

FIGURE 7. Circuit schematic of a single module of TAB converter with both BSs and PV systems connected to modular dc–ac–ac converters via a 3-W transformer.

ac output via a 3-W high-frequency transformer, with a turns ratio of $n_p:n_b:1$ where n_p and n_b represent the turns ratio of the PV and battery converters, respectively.

To minimize the reactive power between the dc and ac sides, the input voltage must be approximately equal to the output voltage after accounting for the turns ratio of the transformer. In other words, $V_p/n_p \approx V_b/n_b \approx V_{\rm dc}$ [30]. Equation set (14) characterizes the per-switch VA rating for bridge 1, as annotated in Figure 7.

$$\text{Bridge 1:}\quad \begin{aligned} V^{1-\text{SW}} &= \begin{cases} V_p = n_p \times V_{\rm dc}, & \text{PV} \\ V_b = n_b \times V_{\rm dc}, & \text{BS} \end{cases} \\ I^{1-\text{SW}} &= \begin{cases} \dfrac{I_{L-\text{pv}}}{\sqrt{2}} = \dfrac{I_L}{\sqrt{2}\,n_p}, & \text{PV} \\ \dfrac{I_{L-\text{batt}}}{\sqrt{2}} = \dfrac{I_L}{\sqrt{2}\,n_b}, & \text{BS} \end{cases} \\ n^{\text{SW}} &= 4\times 3\times p = 12p \\ \text{VA}^{\text{SW}} &= \begin{cases} 2\sqrt{2}\,P_{\rm pv} \times r_{\rm pv}, & \text{PV} \\ 2\sqrt{2}\,P_{\rm batt} \times r_{\rm batt}, & \text{BS} \end{cases} \end{aligned} \tag{14}$$

where $p = b$ represents the number of TAB modules, and I_L represents the RMS value of the net inductor current on the secondary side, which is shared between the two dc systems during the power-transfer process, and the ratio of $I_L - x/I_{\text{DC}-x} = r_x \approx 1.1 - 1.3$ results in an optimized design with minimized VA requirements ($x = pv, batt$). The analysis assumes a phase shift of up to 0.2 per unit (p.u.) to minimize reactive power flow [30], [31]. Similarly, equation sets (15) and (16) characterize the per-switch VA rating for bridges 2 and 3, as annotated in the figure.

$$\text{Bridge 2:}\quad \begin{aligned} V^{1-\text{SW}} &= V_{\rm dc} \\ I^{1-\text{SW}} &= \frac{I_L}{\sqrt{2}} \\ n^{\text{SW}} &= 4\times 3\times p = 12p \\ \text{VA}^{\text{SW}} &= 2\sqrt{2}\,P_{\rm inv} \times r_{\rm inv} \end{aligned} \tag{15}$$

where again the ratio of $I_L/I_{\rm dc} = r_{\rm inv} \approx 1.1 - 1.3$ results in an optimized design with minimized VA requirements.

$$\text{Bridge 3:}\quad \begin{aligned} V^{1-\text{SW}} &= V_{\rm dc} = \frac{1}{p}\frac{V_{\rm ac}}{2d_m} \\ I^{1-\text{SW}} &= \frac{I_{\rm ac}}{\sqrt{2}} \\ n^{\text{SW}} &= 4\times 3\times p = 12p \\ VA^{\text{SW}} &= \frac{\sqrt{2}\,P_{\rm inv}}{d_m} \end{aligned} \tag{16}$$

It may be observed that the ratio between the module's dc-link voltage and the ac grid voltage features the number of modules $p = b$ and the ac-modulation strategy factor d_m. The total VA rating of the overall converter is characterized in (17).

$$\text{VA}^{\text{SW}} = \sqrt{2}\,P_{\rm inv}\left[2r \times (ILR + 0.5 + 1) + \frac{1}{d_m}\right] \tag{17}$$

where the ratio of $I_L - x/I_{\text{dc}-x} = r_x \approx 1.2$ results in an optimized design with minimized VA requirements ($x = pv, batt, inv$). It may be observed that in comparison to dc-stacked topologies and a nonisolated CBC, a 3-W TAB is expected to have a higher switch VA rating. The "Results and Discussion" section presents a design example that compares the several architectures.

Battery/PV/Intermediate Energy Storage Ratings

Similar to a cascaded bridge modular converter, the dc–ac converters of the 3-W TAB modular converter have to be sized to filter single-phase ac power. Although the same equations remain valid [reiterated in (18) and (19)], the capacitance can be distributed between the dc input and ac output for filtering.

$$\frac{C_{\rm dc}}{\dfrac{C_{\rm batt}}{C_{\rm PV}}} = \frac{2}{\pi} I_{\rm dc} \frac{T_{\rm ac}}{4} \frac{1}{r_{V_{\rm dc}}} \tag{18}$$

$$\frac{L_{\rm batt}}{L_{\rm PV}} = \frac{r_{V_{\rm batt/PV}} \times T_{\rm ac}}{2\pi r_{I_{\rm batt/PV}}} \tag{19}$$

where the definition of the variables remain the same.

Efficiency Calculations

Table 3 derives the current expressions critical for loss calculations in a 3-W TAB. The notations I_{x0}, I_{x1} represent the current values when the transformer leakage inductance is referred to the PV, battery, and ac side bridge where $x = P, B,$ ac (I_{P0}, I_{P1} are annotated in Figure 7). Duty ratios d_0, d_ϕ represent the duty ratios of the diode conduction interval referred to the primary side and the phase shift, respectively. Here, the distribution of currents between the transistors and the diodes for the RMS and average calculations assumes that the power is transferred from the PV panel to the battery and the ac grid, where f_b, $f_{\rm ac}$ represent the fraction of PV power transfer to the battery and the ac grid, respectively. Similar expressions can be derived for other power-transfer cases. For the power loss calculations in the output ac bridge (referred to as *bridge 3*), the loss expressions (8)–(10) discussed in the "Efficiency Calculations" section hold true. The "Results and Discussion" section presents comparative results for a design example under discussion.

TAB With a Five-Winding High-Frequency Transformer Topology

To overcome the disadvantage of processing single-phase ac power processing requirements in modular topologies such as CBC and TAB converter, the three ac legs can be integrated using a high-frequency transformer [31]. The circuit schematic of the converter is illustrated in Figure 8. The high-frequency transformer interfaces the PV and the BSs with the three-ac phases to eliminate the need for low-frequency power processing. Similar to 3-W TAB converter, this topology is an ac-coupled configuration in Figure 1(b).

The five-winding (5-W) TAB converter is expected to be more power dense in contrast to the 3-W TAB

converter, with control complexity as a tradeoff. The next few sections detail quantitative and qualitative results.

VA Ratings of Semiconductor Components

VA ratings of the 5-W TAB converter are expected to be comparable to the 3-W TAB converter of the "Triple-Active Bridge With a Three-Winding High-Frequency Transformer Topology" section. Equation sets (20)–(22) characterize net VA ratings for the three bridges wherein the current magnitudes will include three-phase power calculations.

$$\text{Bridge 1:}\quad \begin{aligned} V^{1-\text{SW}} &= \begin{cases} V_p = n_p \times V_{\text{dc}}, & \text{PV} \\ V_b = n_b \times V_{\text{dc}}, & \text{BS} \end{cases} \\ I^{1-\text{SW}} &= \begin{cases} \dfrac{I_{L-\text{pv}}}{\sqrt{2}}, & \text{PV} \\ \dfrac{I_{L-\text{batt}}}{\sqrt{2}}, & \text{BS} \end{cases} \\ n^{\text{SW}} &= 4 \times p \\ \text{VA}^{\text{SW}} &= \begin{cases} 2\sqrt{2}\, P_{\text{pv}} \times r_{\text{pv}}, & \text{PV} \\ 2\sqrt{2}\, P_{\text{batt}} \times r_{\text{batt}}, & \text{BS} \end{cases} \end{aligned} \tag{20}$$

$$\text{Bridge 2:}\quad \begin{aligned} V^{1-\text{SW}} &= V_{\text{dc}} \\ I^{1-\text{SW}} &= \frac{I_L}{\sqrt{2}} \\ n^{\text{SW}} &= 4 \times 3 \times p = 12p \\ \text{VA}^{\text{SW}} &= 2\sqrt{2}\, P_{\text{inv}} \times r_{\text{inv}} \end{aligned} \tag{21}$$

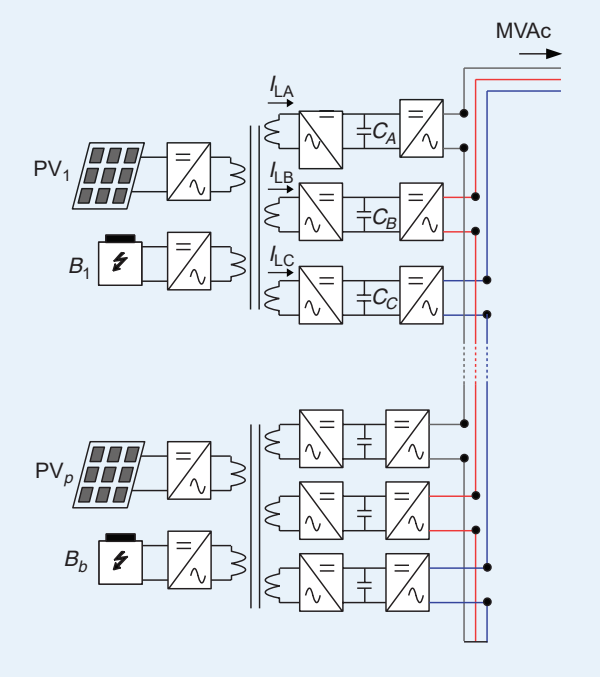

FIGURE 8. The converter topology of a three-phase cascaded TAB converter with both BSs and PV systems connected to modular dc–ac–ac converters via a 5-W transformer. Note that the three ac phases are integrated together with the same dc systems.

Table 3. RMS and average current expressions for TAB converters useful for loss calculations

	Component	I_{RMS}	I_{avg}
PV	Transistors	$\sqrt{\frac{(I_{P0}^2 + I_{P1}^2 + I_{P0}I_{P1})}{3}(0.5 - d_\phi) + \frac{I_{P1}^2}{3}(d_\phi - d_0)}$	$I_{P0}(0.25 - 0.5d_\phi) + I_{P1}(0.25 - 0.5d_0)$
	Diodes	$I_{P0}\sqrt{\frac{d_0}{3}}$	$0.5I_{P0}d_0$
	Inductor LP	$\sqrt{\frac{(I_{P0}^2+I_{P1}^2+I_{P0}I_{P1})}{3}(1-2d_\phi)+\frac{(I_{P0}^2+I_{P1}^2-I_{P0}I_{P1})}{3}2d_\phi}$	-
	where, $d_0 = \frac{I_{P0}L_S f_S}{\left(V_p + \frac{V_{\text{dc}}}{n_p}\right)}$, $d_\phi = \frac{\phi}{2\pi}$, $I_{P0} = \frac{2\phi V_{\text{dc}} n_p - \pi(V_{\text{dc}} n_p - V_p)}{4\pi f_S L_p}$ and $I_{P1} = \frac{2\phi V_p + \pi(V_{\text{dc}} n_p - V_p)}{4\pi f_S L_p}$		
Battery	Diodes	$\sqrt{\frac{(I_{B0}^2 + I_{B1}^2 + I_{B0}I_{B1})}{3}(0.5 - d_\phi) + \frac{I_{B1}^2}{3}(d_\phi - d_0)}$	$I_{B0}(0.25 + 0.5d_0 - 0.5d_\phi) + I_{B1}(0.25 - 0.5d_\phi)$
	Transistors	$I_{B0}\sqrt{\frac{d_\phi - d_0}{3}}$	$0.5I_{B0}(d_\phi - d_0)$
	where $L_b = \frac{L_p n_b^2}{n_p^2}$, $I_{B0} = f_b \frac{\frac{2\phi V_p n_b}{n_p} - \pi\left(\frac{V_p n_b}{n_p} - V_b\right)}{4\pi f_S L_b}$ and $I_{B1} = f_b \frac{2\phi V_b + \pi\left(\frac{V_p n_b}{n_p} - V_b\right)}{4\pi f_S L_b}$		
AC	Diodes	$\sqrt{\frac{(I_{\text{ac0}}^2 + I_{\text{ac1}}^2 + I_{\text{ac0}}I_{\text{ac1}})}{3}(0.5 - d_\phi) + \frac{I_{\text{ac1}}^2}{3}(d_\phi - d_0)}$	$I_{\text{ac0}}(0.25 + 0.5d_0 - 0.5d_\phi) + I_{\text{ac1}}(0.25 - 0.5d_\phi)$
	Transistors	$I_{\text{ac0}}\sqrt{\frac{d_\phi - d_0}{3}}$	$0.5I_{\text{ac0}}(d_\phi - d_0)$
	where $L_{ac} = \frac{L_p}{n_p^2}$, $I_{\text{ac0}} = f_{\text{ac}} \frac{\frac{2\phi V_p}{n_p} - \pi\left(\frac{V_p}{n_p} - V_{\text{dc}}\right)}{4\pi f_S L_{\text{ac}}}$ and $I_{\text{ac1}} = f_{\text{ac}} \frac{2\phi V_{\text{dc}} + \pi\left(\frac{V_p}{n_p} - V_{\text{dc}}\right)}{4\pi f_S L_{\text{ac}}}$		

$$\text{Bridge 3:}\quad \begin{aligned} V^{1-\text{SW}} &= V_{\text{dc}} = \frac{1}{p}\frac{V_{\text{ac}}}{d_m} \\ I^{1-\text{SW}} &= \frac{I_{\text{ac}}}{\sqrt{2}} \\ n^{\text{SW}} &= 2\times 3\times p = 6p \\ \text{VA}^{\text{SW}} &= \frac{\sqrt{2}\,P_{\text{inv}}}{d_m} \end{aligned}. \tag{22}$$

It may be noted that although expressions (20)–(22) are comparable to those of the 3-W TAB modules, the dc–ac converters for the PV and BS process three-phase ac power. In other words, in contrast to the 3-W TAB, the 5-W TAB features a single dc–ac converter per dc source.

Further, considering the ac–dc–ac converter, i.e., bridges 2 and 3 in the figure, each of the three cascaded converters process single-phase ac power directly to the output, resulting in minimal capacitance values at the intermediate link (C_A, C_B, and C_C). Hence, the net converter currents (I_{LA}, I_{LB}, and I_{LB}) feature a second-harmonic ripple, resulting in higher RMS current values. This can be identified in the net VA rating calculations of (23).

$$\text{VA}^{\text{SW}} = 2\sqrt{2}\,P\left[r\times(ILR+z) + r_{\text{inv}}^{2\omega_p} + \frac{1}{d_m}\right] \tag{23}$$

where the ratio of $I_L - x/I_{\text{DC}-x} = r_x \approx 1.2$ for the PV and battery converters. Note that the factor $r_{\text{inv}}^{2\omega_p}$ will be much higher than a 3-W TAB because the current waveforms will feature a second-harmonic ripple. The "Results and Discussion" section demonstrates the performance of this architecture using a design example.

Battery/PV Energy Storage Ratings

In contrast to a 3-W TAB converter, the energy storage elements of the 5-W TAB converter process only high-frequency current and voltage ripples. The sizing equations for the capacitive and inductive energy storage that reduce the impact of the switching action at the dc and ac side are characterized in (24) and (25), and (26), respectively.

$$C_{\text{Batt}-\text{PV}} = I_{\text{dc}} \times \frac{T_S}{4}\frac{1}{r_{V_{\text{dc}}}} \tag{24}$$

$$L_{\text{Batt}-\text{PV}} = \frac{r_{V_{\text{dc}}}}{4}\frac{T_S}{4}\frac{1}{r_{I_{\text{dc}}}} \tag{25}$$

$$C_{\text{dc}} = \frac{\left(\frac{\hat{I}_{\text{ac}} + I_{\text{dc}}}{3}\right)\times \hat{d}_0\, T_S}{r_{V_{\text{dc}}}} \tag{26}$$

where $\hat{d}_0$ represents the maximum value of the zero state of ac bridge 3 when the peak value of the ac phase current and rectified inductor current flows into the capacitor. Similar to dc-stacked topologies, the size of the energy storage elements is a function of the modulation strategy because the dominant ripple is due to the switching action. It may be noted that while under ideal scenarios although the energy storage elements will be sized to filter high-frequency switching ripples, energy storage elements will need to filter any low-frequency ripples that are imposed due to practical challenges in implementing the control approach.

Efficiency Calculations

Although the analytical equations presented in the "Efficiency Calculations" section can be utilized for loss calculations in the 5-W TAB, it may be noted that the PV and battery bridges are integrated for the three ac phases. The "Results and Discussion" section presents comparative results for the design example under discussion.

Control Strategies for Hybrid PV+BS Plants

Modular power electronic converters feature a hierarchical control strategy. Figure 9 illustrates a simplified block diagram for a hybrid PV+BS power plant, which consists of a central controller at the grid level and local controllers for module-level controls. The central controller receives power dispatch commands from the grid-side system operator, which includes reference active power (P_g^{ref}) and reference reactive power (Q_g^{ref}), if reactive power control is permitted. The central controller consists of a phase-locked loop (PLL) unit, maintains the power dispatched from the hybrid plant, and provides energy balancing between several converters/modules. Further, the central controller determines the reference power commands for the modular PV and BS, $P_{k,\text{pv}}^{\text{ref}}$ and $P_{k,\text{batt}}^{\text{ref}}$, respectively, where k refers to the kth module. The remaining section discusses the several control approaches within the central controller and for the local controllers suitable for hybrid PV+BS plants. Note that superscript m refers to the measured quantities in the following discussion.

Central Controller

The ac grid-side voltages (v_g^m) are typically processed by a PLL to determine the peak value of the grid voltage ($\hat{V}_g$) and the frequency (f). Consequently, $\hat{V}_g$ and f are utilized to determine the reference active ($P_{\text{ac}}^{\text{ref}}$) and reactive ($Q_{\text{ac}}^{\text{ref}}$) power values, respectively, typically using synchronverters or virtual synchronous generators (VSGs) [32], [33].

The VSG control concept exploits the idea of operating an inverter to mimic a synchronous generator to emulate its inertial characteristics. Typical VSG methods include voltage and frequency filtering, which are obtained from the PLL using a deadband and a proportional controller. The deadband reduces noisy voltage or frequency-support needs to prevent false VSG activation. The proportional controller is designed based on the megawatt/hertz capability of the plant. As these methods include derivative terms and their measurement through PLLs, their implementation uses slower controllers. Recent advanced VSG schemes illustrate improvements in performance in hybrid plants by eliminating PLL and derivative terms [34]. Alternatively, although VSGs inherit the advantages of droop-control methods and provide inertia support, droop-control methods can be considered where no

inertia emulation and a fast response is required [35], [36].

Local Controllers

Based on grid demand, the power availability in PV systems ($P_{k,\mathrm{pv}}$), and the state of charge (SOC) of the BS ($P_{k,\mathrm{batt}}$), the central controller creates the reference power dispatch commands for local controllers of the PV, BS, and inverter systems. The local controllers are responsible for PV/MPPT, BS/SOC, and inverter dc voltage control. Although the control variable for dc-stacked and CBC architectures are duty-ratio variables, the 3-W and 5-W TAB architectures require phase-shift modulation. The following sections discuss control methods for several cases.

The VSG control concept exploits the idea of operating an inverter to mimic a synchronous generator to emulate its inertial characteristics.

Inverter dq Current Controls and Their Alternatives

Synchronous reference frame control, also called *dq control*, transforms grid currents and voltages into a reference frame that rotates synchronously with the grid voltage, e.g., $abc \rightarrow dq$, using PLL techniques. Consequently, as the control variables become dc values, control and filtering is simplified. As illustrated in the figure, the grid-side converter control strategy typically consists of two hierarchical loops. The inner-current loop regulates the grid current, while the outer-voltage loop regulates the dc voltage based on power demand. Hence, the loops are designed for power quality and power flow, respectively. These control loops typically feature proportional–integral (PI) controllers as they have a satisfactory behavior when regulating dc variables [37]. Advanced controllers feature cross coupling or voltage feedforward terms to improve the performance of PI controllers [38], [39].

Due to poor compensation of low-order harmonics with PI control techniques, advanced techniques such as proportional–resonance (PR) controllers, hysteresis and deadbeat controllers are gaining popularity. The implementation of PR controllers is simpler in a stationary reference frame, e.g., $abc \rightarrow \alpha\beta$, or a natural frame of reference and phase-angle information are not necessities [40]. A hysteresis controller introduces variable switching-frequency operation, which is not suitable for grid-tied applications. Several methods have been proposed in the literature, employing an adaptive band to obtain a fixed switching frequency. Complexity of the hysteresis controller is high for current regulation [9], [41]. Alternatively, deadbeat controllers are simpler and attempt to mitigate errors in the control variables within one sample delay. To compensate for this delay, an observer can be introduced into the structure of the controller, with the aim to modify the current reference to compensate for the delay [42], [43]. Nevertheless, all of these inverter control architectures are suitable for the four power electronic architectures under consideration as they are designed for the dc–ac inverter connected to the grid.

DC-Stacked and CBC Architectures

Figure 9 also illustrates the control structure of a local PV controller suitable for dc-stacked and CBC architectures. The MPPT algorithm identifies the maximum power that can be generated by the PV and controls the voltage at the terminals of the PV module $v_{k,p}$. Based on the PV power reference received from the central controller $P^{\mathrm{ref}}_{k,\mathrm{pv}}$, a voltage controller based on PI control creates a current reference $I^{\mathrm{ref}}_{k,\mathrm{pv}}$ command. Consequently, the PI current controller generates the duty ratio for the PV dc–dc converter [33]. In a BS, the local SOC controller determines the SOC of the batteries and controls the power of the battery module. Based on the BS power reference received from the central controller $P^{\mathrm{ref}}_{k,\mathrm{batt}}$, a power controller based on PI control creates a current reference $I^{\mathrm{ref}}_{k,\mathrm{batt}}$ command. Consequently, the PI current controller generates the duty ratio for the PV dc–dc converter [33].

3-W and 5-W TAB Architectures

The voltage-transfer ratio between the input and output in TAB topologies is a critical design factor that has a direct effect on the reactive power flow within the topology. In other words, if $V_p/n_p \neq V_b/n_b \neq V_{\mathrm{dc}}$, high circulating currents can have a significant effect on converter performance [30], [44]. Consequently, the complexities in control strategies for these topologies are higher than traditional dc-stacked and CBC topologies.

With the control architecture in Figure 9, the inverter dc voltage is regulated by the central controller references and is fixed. Consequently, the reference active power command ($P^{\mathrm{ref}}_{k,\mathrm{pv}}$) and the PV module voltage ($v_{k,p}$) obtained from the central controller and the MPPT algorithm is utilized using a PI controller to generate the phase shift for the output ac bridge. A similar control strategy can be implemented on the BSs. As $V_p/n_p \approx V_b/n_b \approx V_{\mathrm{dc}}$ may not hold true, the converter would not operate at the optimized efficiency operating condition. The "Results and Discussion" section quantifies this using a case scenario based on specifications of the design example under consideration. In [45], the authors suggest regulating the PV panel voltage to maintain converter performance. Alternatively, current-fed dual-active bridge dc–dc converters are gaining popularity, where the duty ratio and the phase shift are regulated to maintain a high efficiency operation [44]. An alternate

strategy to Figure 9, which is more suitable for TAB architectures to maintain converter performance, is based on regulating the dc inverter voltage by the PV system [31], [46], [47], [48]. One such implementation is illustrated in Figure 10, where the MPPT controller is employed to regulate the PV output voltage, which provides a constant dc voltage to the inverter. Further, the inverter follows the dc voltage and grid references to provide the desired power at the regulated voltage. The battery bridge phase shift is regulated based on the PV/dc voltages and reference power commands. Although converter efficiency can be optimized with this approach by minimizing the circulating currents, the total per-unit ratings of the converter could be higher than both the dc-stacked and CBC converter topologies to support the grid voltage when the PV operating voltage is low. As noted in the "TAB With

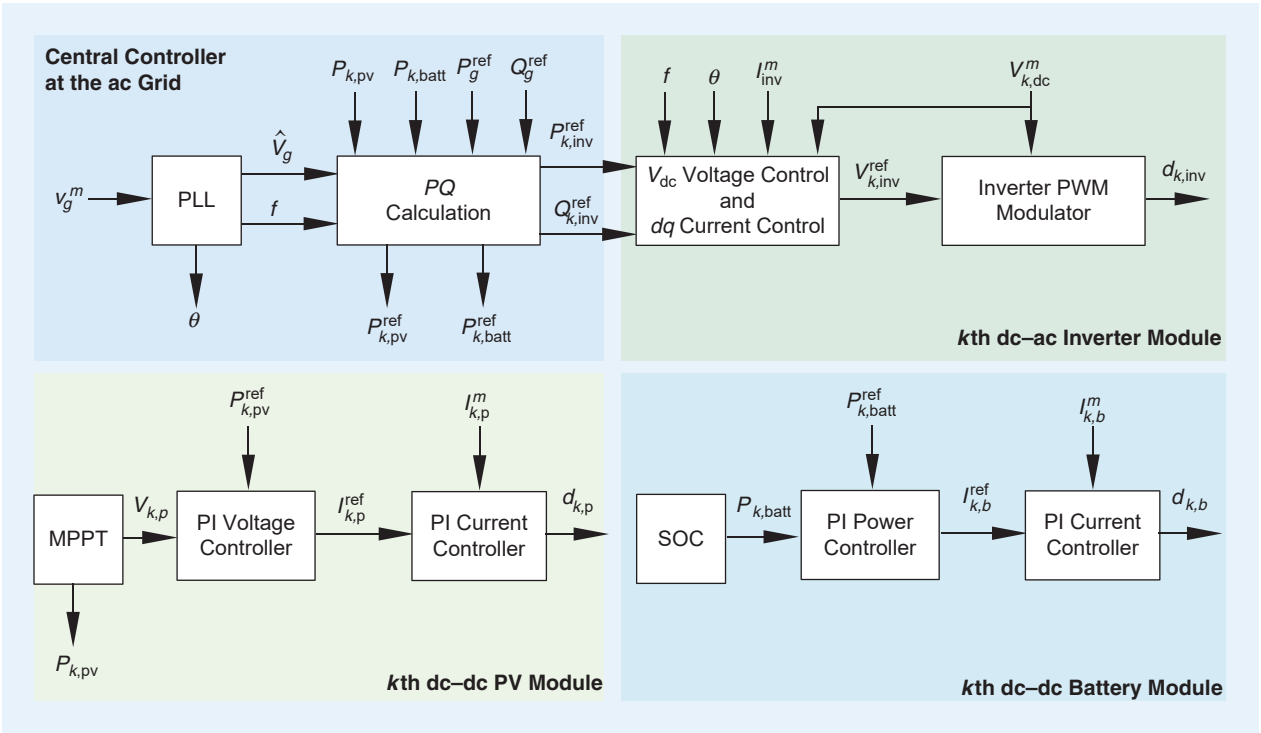

FIGURE 9. A block diagram of the hierarchical control approach for a hybrid PV+BS plant. PLL: phase-locked loop; SOC: state of charge; PI: proportional integral.

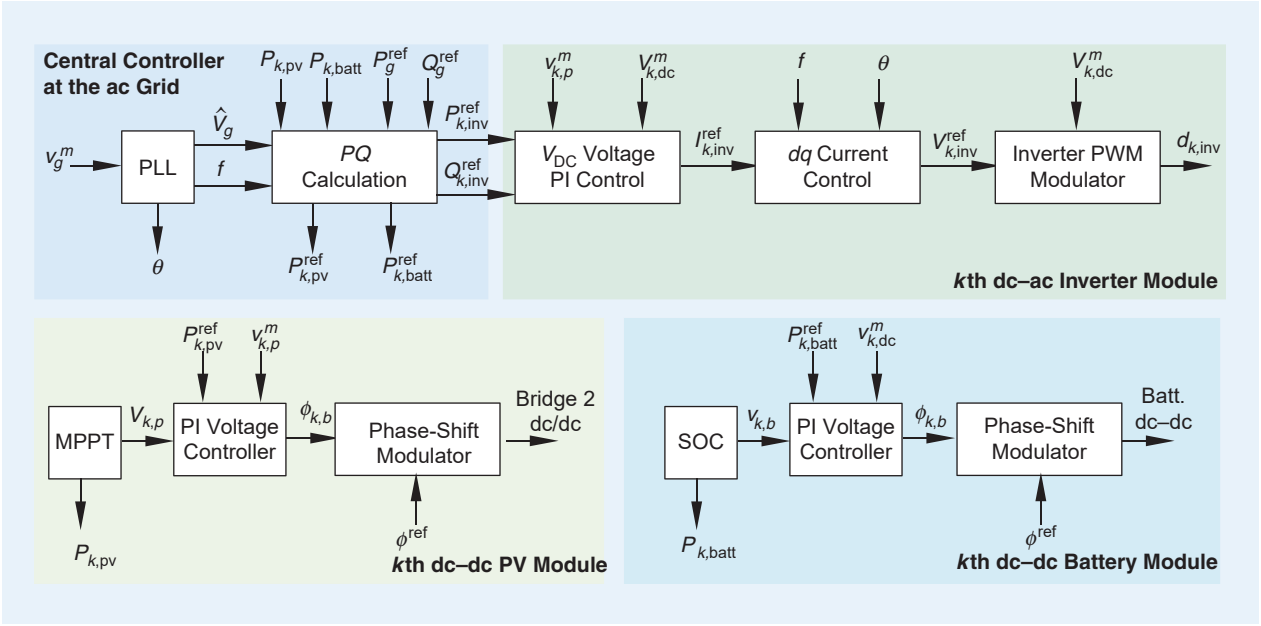

FIGURE 10. A block diagram of the hierarchical control approach for a hybrid PV+BS plant suitable for TAB topologies. Batt.: battery.

a Five-Winding High-Frequency Transformer Topology" section, a 5-W TAB topology necessitates a per-phase phase shift on the ac side to minimize the dc–ac converter capacitor value and reaps the benefits of a three-phase integrated transformer-winding configuration [31].

Double-Star Configuration

Cascaded bridge architectures may be viewed as single-star configurations, which comprise three arms for each of the three ac phases. Although this article focuses on cascaded bridge architectures for modular power conversion, the modular multilevel converter (MMC) configuration provides an alternative for integration of hybrid PV+BS systems to the grid. In contrast to cascaded bridge architectures, the MMC architecture is a double-star configuration featuring six arms. The neutral points of the two-star networks formed by the three arms provide an accessible dc port output. Hence, MMC architectures enable bulk-transmission renewable power by utilizing high-voltage dc (HVdc) transmission infrastructure, along with other grid-support functions [18], [33], [49].

The module designs examined in the "Cascaded Bridge Architectures" section, including FB modules, 3-W, and 5-W transformer TAB modules can be connected in series to form six arms for an MMC configuration. These architectures will be suitable for HVdc transmission from hybrid PV+BS power plants. The analytical results discussed in the article can be extended for such double-star configurations.

Results and Discussion

This section presents quantified and qualitative results of the power converter architectures in terms of VA ratings, energy storage requirements, efficiency estimations, and control complexity for a design example. Table 4 details specifications of the parameter design values suitable for a utility-scale hybrid PV and battery energy storage power plant. As noted in the "Block Diagram of PV+BS Power Plants" section, the ILR and the battery plant power ratings are assumed to be 1.3 and 0.5 p.u., respectively, which are typical in today's plants.

Table 5 lists specifications of the selected benchmark configurations. With a safety margin of 1.2 and a FB converter approach, both the dc-stacked and modular converter architectures feature eight converters and 14 modules, respectively. As the net theoretical per-unitized VA and energy storage ratings will not be affected by the transformer turns ratio, for simplicity, it is assumed to be one-for-all configurations. In practical industrial solutions, other turns ratios could be used for optimization purposes.

Table 6 details ratings of the power semiconductor switches and the energy storage elements for the benchmark cases under consideration. The circuit architectures have been developed in the piecewise linear electrical circuit simulation environment to verify analytical calculations. As noted in the analytical models, TAB modular converter configurations feature a higher per-unitized rating for the power semiconductor devices in comparison to the dc-stacked and cascaded bridge topologies. Further, as noted previously, the 5-W TAB has a slightly higher VA rating in comparison to the 3-W TAB architecture due to the second-harmonic current ripple in the ac/dc/ac bridges. However, in contrast to other modular topologies, the 5-W TAB features a low energy storage requirement due to three-phase transformer integration at the module level. It may also be noted that the higher RMS current ratings in TAB converters also result in higher per-unitized ratings for high-frequency transformers.

Using the efficiency calculation analytical models detailed in the "DC-Stacked Architectures" and "Cascaded Bridge Architectures" sections, and the time-domain simulations, Figures 11–15 present and compare the performance of the four converter approaches in terms of efficiency and loss distribution. Figure 11 compares the efficiency of the various topologies as a function of the switching frequency with a power level of $P_{pv} = 1.3$ p.u., $P_{batt} = 0.3$ p.u., and $P_{ac} = 1$ p.u. The details of the part numbers and the loss parameter values employed for efficiency calculations are summarized in

Table 4. Parameter design values for the design example under consideration

Parameter	Value
Power	18 MVA
Frequency	60 Hz
AC source voltage	13.8-kV RMS
PV:battery:inverter power ratio	1.3:0.5:1
DC battery voltage	400–650V
PV panel voltage	200–600V

Table 5. Specifications of the selected configurations for the several power converter architectures

Topology	DC Stacked	Cascaded Bridge	3-W TAB	5-W TAB
IGBT voltage	1.2 kV (nominal)			
Safety factor	1.2			
DC voltage	1,000 V (nominal)			
Converters	8	—	—	—
Modules	—	14	14	14
LF-TF turns-ratio	13.8/0.55	1:1	—	—
HF-TF turns-ratio	—	—	1:1:1	1:1:1:1:1

LF-TF: low-frequency transformer; HF-TF: high-frequency transformer.

Table 6. Ratings of the power semiconductor devices and the energy storage elements for the design example under consideration

Parameters		DC Stacked	Cascaded Bridge	3-W TAB	5-W TAB
PV converter	Switch VA	3.05 p.u.	3.05 p.u.	4.28 p.u.	4.4 p.u.
	Filtering ES	15.6 m p.u.	0.05 p.u.	0.05 p.u.	2 m p.u.
Battery converter	Switch VA	1.08 p.u.	1.08 p.u.	1.65 p.u.	1.7 p.u.
	Filtering ES	5.25 m p.u.	0.02 p.u.	0.02 p.u.	1 m p.u.
Grid inverter	Switch VA	4.8 p.u.	4.8 p.u.	8.29 p.u.	10.7p.u.
	Filtering ES	17.8 m p.u.	1.63 p.u.	1.59 p.u.	0.15 p.u.
Low-frequency transformer		1 p.u.	1 p.u.	—	—
High-frequency transformer		—	—	1.2 p.u.	1.5 p.u.
Total VA (p.u.)		8.93 p.u.	8.93 p.u.	14.21 p.u.	16.8 p.u.
Total ES (p.u.)		0.04 p.u.	1.7 p.u.	1.67 p.u.	0.15 p.u.

Base power = 18 MVA; base frequency = 60 Hz; base energy = 0.3 MJ; ES: energy storage.

Table S1 in "Loss Calculations." The validity of the analytical models is verified using simulations, where accuracy in the current calculations is reported to be $< 1\%$. The efficiency calculations include transformer losses. The low-frequency line transformer for dc-stacked and CBC topologies and high-frequency module transformers for TAB topologies are assumed to be 99.2 and 99.5%, respectively, [18], [50], [51]. As the PV, battery, and one of the ac-side bridges can be designed to operate under zero-voltage switching, 3-W and 5-W TAB converters feature weaker dependence on the switching frequency in comparison to dc-stacked and CBC topologies at the rated power.

Figures 12 and 13 illustrate loss distribution with a switching frequency of 2 and 20 kHz, respectively. The solid, stacked bars and dashed, stacked bars indicate the per-unitized conduction and switching losses, respectively. As evident in Table 6, 3-W and 5-W TAB topologies have a higher switch VA rating (the additional FB is designed as bridge 2 or B2 in the discussion). Consequently, the net conduction losses in these topologies are higher than in dc-stacked and CBC topologies. In contrast, due to zero-voltage switching (ZVS) operation, TAB topologies have net lower switching losses. Moreover, CBC topologies have lower switching losses compared to a dc-stacked topology due to a lack of modularity and loss parameters of the commercially available devices for higher voltage and current requirements. When comparing 3-W and 5-W TAB converters, due to three-phase integrated PV and battery converter systems, higher current-rated devices are selected, which can be designed with lower on-state resistance. Hence, a 5-W TAB design fairs slightly better than a 3-W TAB one. With the design specifications and design selections, a CBC is clearly the most efficient with lower switching-frequency designs, while a 5-W TAB

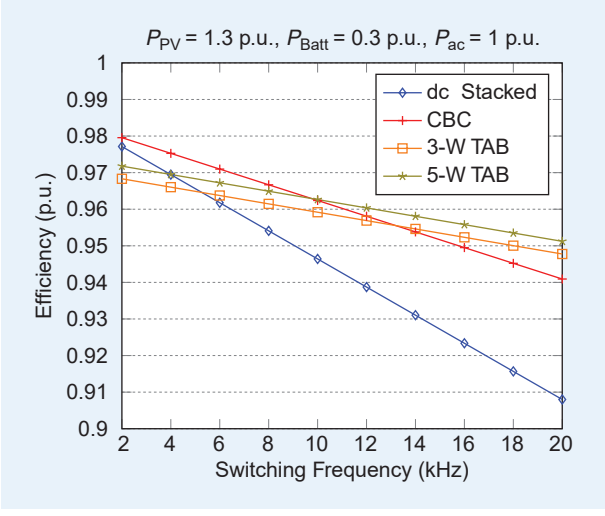

FIGURE 11. Efficiency of the compared topologies as a function of the switching frequency with a power level of $P_{pv} = 1.3$ p.u., $P_{batt} = 0.3$ p.u., and $P_{ac} = 1$ p.u.

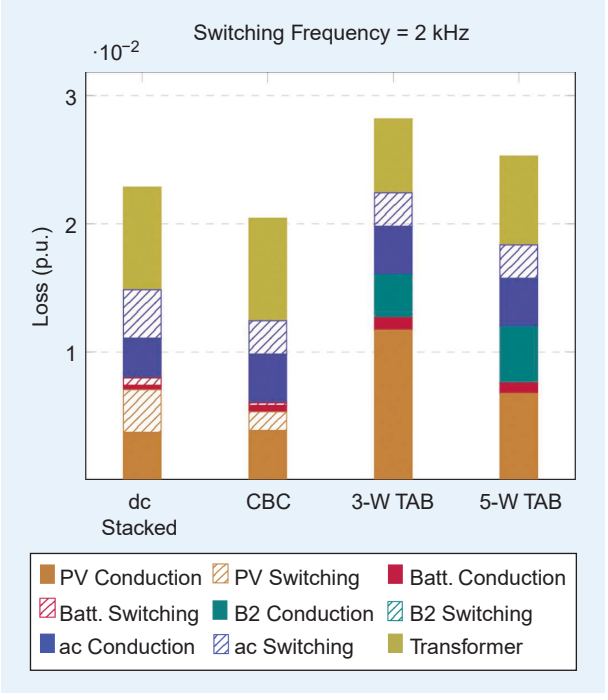

FIGURE 12. Loss distribution with a switching frequency of 2 kHz with a power level of $P_{pv} = 1.3$ p.u., $P_{batt} = 0.3$ p.u., and $P_{ac} = 1$ p.u. Batt.: battery.

is the most efficient in high switching-frequency designs. Switching losses at the dc–ac inverter dominate, with a switching frequency of 20 kHz in all of the topologies.

Figures 14 and 15 quantify the effect of difference in control methods for TAB topologies. Here, with a power level of $P_{pv} = 0.5$ p.u., $P_{batt} = 0$ p.u., and $P_{ac} = 0.5$ p.u., a low-PV power output scenario is considered. Although the high-frequency transformer turns ratio is optimized for a 600-V PV operation and a 1-kV dc inverter voltage operation ($n_p = 0.6$), during low power output from the PV panel, the PV panel voltage is operating at 525 V. In the case of dc bus voltage regulation at the ac inverter control loop, the dc voltage is maintained at 1 kV. On the other hand, if the dc inverter's voltage is regulated by the PV panel voltage, the dc voltage is regulated to 875 V to minimize circulating currents. Figure 14 illustrates the current waveform at the PV side of the high-frequency transformer. It is noted that the RMS value of the current increases by 5% in the case of $V_{dc} = 1$ kV. Figure 15 shows the loss distribution, where the net losses are increased by 10.2 and 9.8% in the case of 3-W and 5-W TABs, respectively. Hence, the tradeoff in adding control complexity with efficiency in the case of TAB topologies is readily observed.

Table 7 provides a summary of the qualitative characteristics of the candidate topologies under discussion.

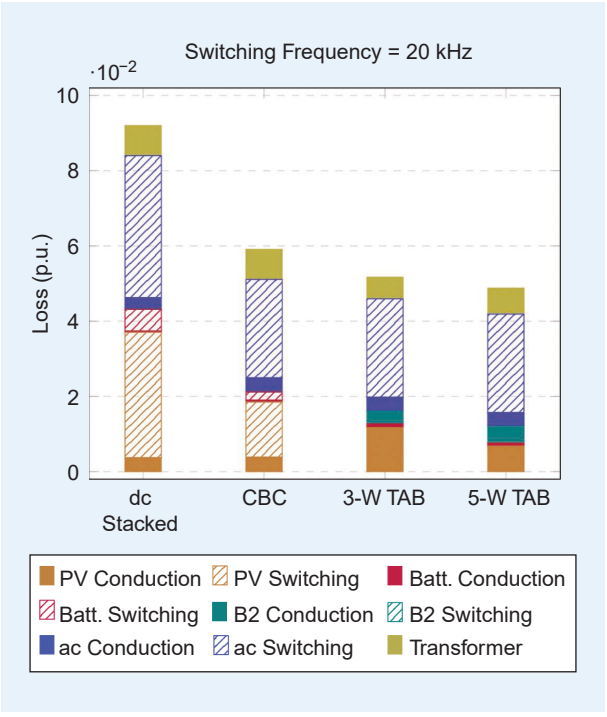

FIGURE 13. Loss distribution with a switching frequency of 20 kHz with a power level of $P_{pv} = 1.3$ p.u., $P_{batt} = 0.3$ p.u., and $P_{ac} = 1$ p.u. Batt.: battery.

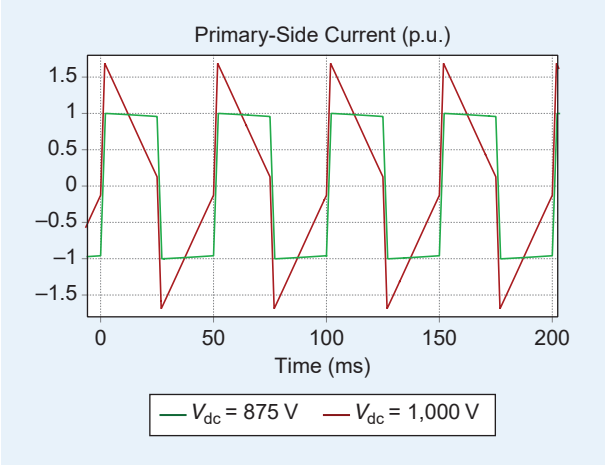

FIGURE 14. Current waveforms on the primary-side high-frequency transformer in a 3-W TAB with a power level of $P_{pv} = 0.5$ p.u., $P_{batt} = 0$ p.u., and $P_{ac} = 0.5$ p.u.; a PV voltage of 525 V; and dc voltages of 875 V (green line) and 1 kV (red line).

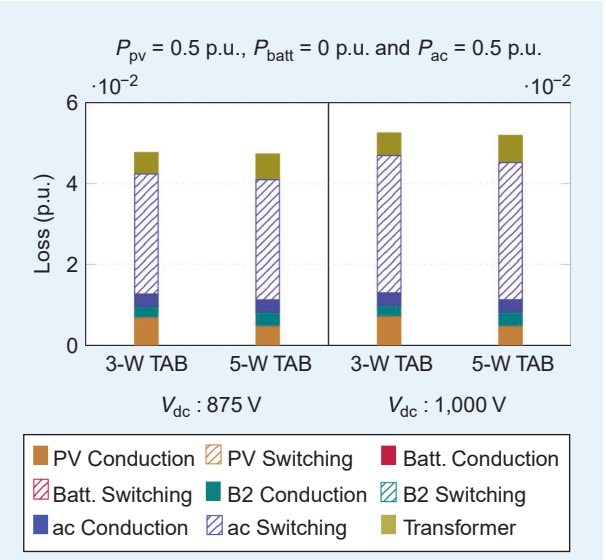

FIGURE 15. Loss distribution with a switching frequency of 20 kHz with a power level of $P_{pv} = 0.5$ p.u., $P_{batt} = 0$ p.u., and $P_{ac} = 0.5$ p.u. for $V_{dc} = 875$ V and $V_{dc} = 1$ kV.

Table 7. Summary of converter qualitative characteristics for the candidate topologies

Topology	DC Stacked	Cascaded Bridge	3-W TAB	5-W TAB
Efficiency	Second	First	Third	Third
Power Density	Third	Second	Second	First
Control Complexity	First	First	Second	Third
Modularity	Second	First	First	First
Maturity Level	First	Second	Third	Third

Although TAB topologies can be optimized at high-frequency switching, dc-stacked and CBC topologies utilize lower switching-frequency operation. As noted in Figure 11, CBC and TAB topologies have the highest efficiency in their design space of frequency selection. Overall, CBC topologies have the highest efficiency, with a low switching-frequency design. Further, as concluded in Table 6, a 5-W TAB is expected to have the highest power density due to its low energy storage requirements. As a tradeoff for minimized, intermediate energy storage, the 5-W TAB will require a higher degree of control complexity to manage the second-harmonic power ripple at the ac–dc–ac converter bridges to minimize the size of the intermediate energy storage element. Further, TAB topologies require extensive optimization to maintain ZVS operation over a wide operating range to maintain high efficiency. Finally, modular topologies benefit from ease of integration and superior fault tolerance due to a modular design, which is also indicated in the table.

Conclusion

This article provided a comparative examination of power electronic conversion architectures that are suitable for utility-scale hybrid PV and battery energy storage power plants. In particular, the article presented the characteristics of several power conversion architectures from the point of view of power semiconductor requirements, reactive component requirements, efficiency, modularity, control complexity, and so on. Based on the provided analysis, a cascaded bridge dc–ac converter is expected to be most attractive in terms of efficiency. On the other hand, three-phase integrated TAB converters are superior in terms of overall power density, with control complexity as a tradeoff in comparison to other approaches. The article gave detailed analytical models to present the comparative evaluation in terms of the alternatives that are suitable for hybrid PV+BS power plants. The results from this article are geared toward supporting the current and future planned specific case and optimization studies of hybrid PV and battery storage power plants.

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