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# Threshold voltage control with high-temperature gate-oxide annealing in ultrawide bandgap AlGaN-channel MOSHFETs

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We report threshold voltage ($V_{TH}$) control in ultrawide bandgap $Al_{0.4}Ga_{0.6}N$-channel metal oxide semiconductor heterostructure field-effect transistors using a high-temperature (300 °C) anneal of the high-$k$ $ZrO_2$ gate-insulator. Annealing switched the polarity of the fixed charges at the $ZrO_2$/AlGaN interface from $+5.5 \times 10^{13}$ cm$^{-2}$ to $-4.2 \times 10^{13}$ cm$^{-2}$, pinning $V_{TH}$ at $\sim(-12$ V), reducing gate leakage by $\sim 10^3$, and improving subthreshold swing 2× (116 mV decade$^{-1}$). It also enabled the gate to repeatedly withstand voltages from −40 to +18 V, allowing the channel to be overdriven doubling the peak currents to ~0.5 A mm$^{-1}$. © 2022 The Japan Society of Applied Physics

Supplementary material for this article is available online

III-Nitride HEMTs have attracted attention due to their high-power handling capabilities for compact consumer electronics.[1–4] Chargers with III-Nitride HEMTs designed for phones, tablets, laptops, etc. are half the size of conventional chargers, while offering fast charging capabilities. These devices are also becoming a major part of electric vehicle (EV) controls in modern transportation. Recently, many hybrid and EV automakers are investing in III-Nitride technology to enable higher power conversion efficiency, reduced system cost and weight compared to their traditional silicon counterparts.[5,6] The simultaneous combination of high frequency, high-power density and high-temperature operation capabilities of III-Nitride electronics enables this performance improvement.

For continued scaling to smaller footprints in power electronics, ultrawide bandgap (UWBG) $Al_xGa_{1-x}N$ ($x > 0.3$, $E_G > 3.4$ eV) electronics are needed. This improvement is predicated on the scaling of the breakdown field with alloy composition.[7,8] Thus $Al_xGa_{1-x}N$ ($x > 0.4$) channel high electron mobility field-effect transistors (HFETs) are promising candidates for compact next-generation power electronics.[9–12] However, in addition to the breakdown field, good gate control and low gate leakage are also key requirements.[13,14] Recently using gate dielectrics, both depletion mode (D-mode)[15] and enhancement mode (E-mode)[16] metal oxide semiconductor heterostructure field-effect transistors (MOSHFETs) have been demonstrated.

Including a dielectric such as $SiO_2$ between the gate metal and barrier/channel region results in the reduction of gate leakage in metal oxide semiconductor HFET's (MOSHFET) in both voltage directions.[17] However, this comes at the expense of higher negative threshold voltage ($V_{TH}$), requiring higher operating gate voltages that can potentially lead to higher gate leakage, negating the very benefit the dielectric was supposed to provide. This can be solved using high-$k$ dielectrics which are often deposited using atomic layer deposition (ALD) due to the ease and precision of the thickness control.[18,19] These ALD dielectrics can suppress gate leakage while maintaining a large gate capacitance in thick enough layers to increase the gate operating voltage with only a modest shift in $V_{TH}$.[19] However, in these ALD dielectrics, the $V_{TH}$ shift is governed not only by the geometrical capacitance, but to a large extent by the fixed charges at the dielectric/AlGaN interface, $n_{ox,intf}$, the distributed fixed charges through the bulk of the dielectric, $n_{ox,bulk}$, and the interfacial trapped charges.[20] These charges present additional variables that must be controlled to achieve the desired $V_{TH}$ with low gate leakage, which is the subject of this paper.

Post-deposition annealing of ALD dielectrics can influence the crystal quality and reduce fixed charges and the trap density at the oxide/semiconductor interface.[21,22] However, selecting the optimal annealing temperature is a very crucial issue. If the temperature is too low, there is no significant influence on $n_{ox,intf}$ and $n_{ox,bulk}$. If the temperature is too high, recrystallization of the ideally amorphous dielectric, can lead to higher leakage currents through the grain boundaries.[23] J. Liu et al. reported that, for $ZrO_2$ the onset of crystallization starts around 210 °C and above 350 °C it completely changes to a crystal structure.[21] The anneal temperature for the ideal optical density was found to be around ~300 °C. Thus, for our study reported here, we selected a 300°C post-deposition anneals of the gate dielectric ($ZrO_2$) to maximize its influence on the bulk/interface charges and the interface trap density without changing the crystalline structure.

To quantify the influence of $n_{ox,intf}$ and $n_{ox,bulk}$ on $V_{TH}$, in MOSHFETs we use.[20,24]

$$V_{th} = \Phi_b - \Phi_f - \Delta E_c - \frac{qt_{ox}^2}{2\varepsilon_{ox}} n_{ox,bulk} - \frac{qt_{ox}}{\varepsilon_{ox}} n_{ox,intf} - q\left(\frac{t_{ox}}{\varepsilon_{ox}} + \frac{t_b}{\varepsilon_b}\right), \quad (1)$$

where $\Phi_b$ is the metal barrier height, $\Delta E_c$ is the conduction band discontinuity, $\Phi_f$ is the energy difference between conduction band and Fermi energy, $t$ is thickness, $\varepsilon$ is permittivity and the subscripts b and ox refer to AlGaN barrier and oxide ($ZrO_2$). $n_{ox,bulk}$ represents the bulk oxide charge (per unit volume), and $n_{ox,intf}$ represents the oxide/barrier interface charge density. Equation (1) underscores the abovementioned fact that $n_{ox,bulk}$ and $n_{ox,intf}$ are two key $V_{TH}$ control parameters in MOSHFETs especially in thicker oxides. High-$k$ ALD oxides have already shown superior device performance in UWBG MOSHFETs.[25,26] In this report we present an oxide thickness ($t_{ox}$) dependent study of $V_{TH}$ values for MOSHFETs with annealed and unannealed

high-$k$ ALD $ZrO_2$ gate-insulator to separate the contributions from $n_{ox,bulk}$ and $n_{ox,intf}$.

Figure 1(a) shows the schematic epilayer structure and device geometry for this work. The structure was grown over a 3 $\mu$m thick high quality AlN/Sapphire template using metalorganic chemical vapor deposition. A reverse graded back barrier AlN-$Al_{0.4}Ga_{0.6}N$ of 85 nm was grown to ensure pseudomorphic registry and screen defects generated from the growth interface.[16] It was followed by 180 nm undoped $Al_{0.4}Ga_{0.6}N$-channel layer, 0.3 nm thick AlN spacer layer and 15 nm n-$Al_{0.6}Ga_{0.4}N$ barrier layer. UWBG $Al_xGa_{1-x}N$ ($x > 0.4$) has low electron affinity ($\chi_S$) that results in high Schottky barrier height ($\Phi_B = \Phi_m - \chi_S$) that in turn results in high contact resistance. To facilitate ohmic contact formation we dope the barrier for reducing the tunneling barrier width for electrons.[17] The donor concentration in the barrier layer, $N_d$ is extracted from the linear $1/C^2$ versus $V$ characteristics that was found to be $\sim 5 \times 10^{18}$ cm$^{-3}$. A 15 nm reverse composition graded $Al_xGa_{1-x}N$ ($x = 0.6$ to 0.3) was grown on top of the n-$Al_{0.6}Ga_{0.4}N$ to further facilitate ohmic contact formation by lowering the effective Schottky barrier height from 2.7 eV for $Al_{0.6}Ga_{0.4}N$ to 0.62 eV for $Al_{0.3}Ga_{0.7}N$.[16] The sheet resistance ($R_{sh}$) of the as grown 2″ wafer was measured by the Lehighton contactless sheet resistance mapping system to be ~2300 Ω sq$^{-1}$ (see supplementary Fig. S1, available online at stacks.iop.org/APEX/15/104001/mmedia). From mercury probe capacitance–voltage ($C$–$V$) measurement system the depletion voltage was estimated as ~−11 V (see Fig. S2).

The device processing started with mesa isolation using $Cl_2$-based inductively coupled plasma reactive ion etching. Ohmic contacts were defined by photolithography with subsequent metallization of Zr/Al/Mo/Au (15/100/40/30 nm) using E-beam metal deposition.[27,28] The contacts were annealed at 950 °C for 30 s under $N_2$ environment by rapid thermal annealing. The contact and sheet resistances were measured using transmission line model (TLM) test patterns. The ohmic contact resistance ($R_c$) and the sheet resistance ($R_{sh}$) were found to be 2.1 ohm mm and 2280 Ω sq$^{-1}$ respectively. $R_{sh}$ was consistent with the values measured on the wafer using the Eddy current method.

The sample was then diced into four pieces: three pieces were used for fabricating $ZrO_2$ MOSHFETs with 10, 20 and 30 nm of oxide thicknesses and the remaining piece was used for the control HFET (no oxide under the gate). The $ZrO_2$ film was deposited using a thermal ALD process at 200 °C, with trimethylaluminum (TMA), tetrakis (dimethylamido) zirconium (IV) (TDMAZ) and deionized water as the precursors.[25] The TDMAZ precursor was also heated to 75 °C in order to achieve a linear growth rate of 0.7 Å/cycle. The deposition was initiated with 15 water pulses prior to the typical AB pulsing sequence to deposit the gate dielectric to ensure saturation of hydroxyl groups at the AlGaN surface required for conformal ALD nucleation. $ZrO_2$ was then removed from the ohmic contact area so probe pad can be connected to the ohmic contacts. The details of the ALD deposition process can be found in Ref. 25. The Ni/Au (100/200 nm) gate metal was then patterned by photolithography and deposited by E-beam evaporation using a liftoff process. Transistors with a source-drain spacing of 6 $\mu$m and gate length of 1.8 $\mu$m were fabricated. Gated TLM structure with gate length 100 $\mu$m was also fabricated for $C$–$V$ measurement. Similar to the earlier reports on post-deposition annealing of $ZrO_2$,[11,21–23] our MOSHFET devices were taken through a two-step post-deposition annealing procedure on a hotplate in $O_2$ ambient atmosphere. For high-$k$ dielectrics, as compared to other annealing environments such as $N_2$, the $O_2$ annealing has shown a great impact on the positive shift of the threshold voltage. As suggested earlier, this may be due to the passivation of oxygen vacancies at the oxide/semiconductor interface.[29] The $O_2$ annealed devices are also expected to be less prone to drain current degradation because oxygen creates stronger bonding when passivating dangling bonds due to oxygen vacancies. When available, our data on $O_2$-annealed MOSHFET reliability will be published elsewhere. The annealing was performed at 250 °C first and then at 300 °C for 30 min at each temperature. The first annealing temperature was chosen as slightly higher

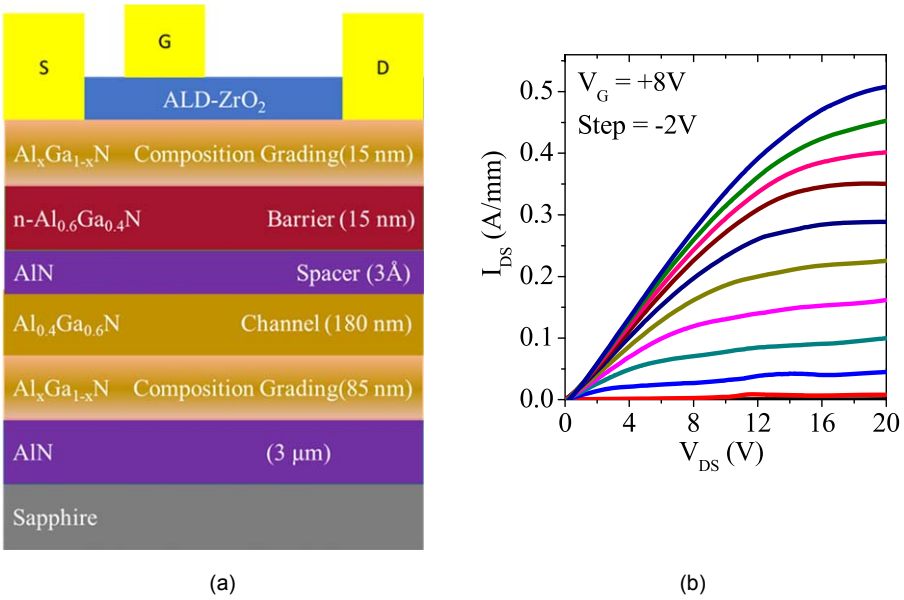


**Fig. 1.** (Color online) (a) Schematic layout of $ZrO_2$ MOSHFET (b) output characteristics of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ MOSHFET with 10 nm $ZrO_2$ after annealing.

than the deposition temperature (200 °C). The devices were characterized both before and after the annealing step. At 250 °C annealing no significant change in device characteristics was noticed; then the temperature was raised to 300 °C. Thus, the reported results all correspond to the 300 °C anneal.

The DC output and transfer characteristics were measured using a parameter analyzer Agilent 4155 C and the *C–V* measurements were done using HP 4284 A LCR meter. Figure 2(a) shows that, at gate voltage $V_G = +1$ V annealing reduces the capacitance value from ∼(3–4) × $10^{-7}$ to ∼(1.8–2.2) × $10^{-7}$ F $cm^{-2}$. The 2DEG charge density ($n_s$) was extracted using the *C–V* measurement on a 100 $\mu$m wide gated TLM structures. Figure 2(b) reflects the corresponding reduction in $n_s$. The on-state sheet electron density $n_s$ was estimated to be ∼1–4 × $10^{13}$ $cm^{-2}$ for the various devices of this study (see Table I).

From *C–V* characteristics we estimate the $ZrO_2$ dielectric constant using the following formula:

$$1/C_G = 1/C_{ox} + 1/C_b,$$

where $C_G$ is the measured gate capacitance, values for the unannealed and annealed conditions are 2.45 × $10^{-7}$ and 1.83 × $10^{-7}$ F $cm^{-2}$, respectively. $C_b$ is the barrier capacitance which is obtained from the HFET *C–V* characteristics without the $ZrO_2$ (2.58 × $10^{-7}$ F $cm^{-2}$). Given the 20 nm thickness, the dielectric constant is extracted from $C_{ox} = \varepsilon_r \varepsilon_0 / t_{ox}$ to be $\varepsilon_r = 115.92$ and 14.6 for as deposited and annealed $ZrO_2$.

A typical output characteristic is shown in Fig. 1(b), where good saturation behavior is seen with current densities ∼0.5 A $mm^{-1}$ in the 1.8 $\mu$m gate length devices. Typical output characteristics for HFET and MOSHFET devices with 20 and 30 nm $t_{ox}$ are presented in the Supplementary Information section (Fig. S3).

Figure 3 shows the double sweep transfer characteristics of the 1.8 $\mu$m gate length devices with at a drain bias $V_{DS} = +10$ V. It shows hysteresis in both cases of before and after annealing. Annealing does not completely remove the hysteresis but a reduction in hysteresis was observed. Due to their extremely low gate leakage, MOSHFET devices can operate at much higher positive gate voltages as compared to HFETs, which lose the gate control at $V_G \geqslant 2$ V due to high gate conduction. For the 30 nm thick dielectric MOSHFET, at $V_G = +14$ V the channel current 0.5 A $mm^{-1}$ was achieved, which is twice as high as that of HFET (Table I). Further increase in the gate forward bias does not lead to the current increase due to limited 2DEG channel capacity and real-space charge transfer from 2DEG to the dielectric-barrier interface.[30] As seen from Fig. 3(a), the unannealed MOSHFET devices show a very large threshold shift compared to an HFET. $V_{TH}$, which was defined as the gate voltage $V_{GS}$ at which channel current $I_{DS} = 1$ $\mu$A, or 20 $\mu$A $mm^{-1}$, had a large negative shift immediately after deposition (Table I), increasing monotonically with $t_{ox}$. $V_{TH}$ reaches as high as −33.7 V for 30 nm thick $ZrO_2$ making devices unusable in practical applications. The leakage current in

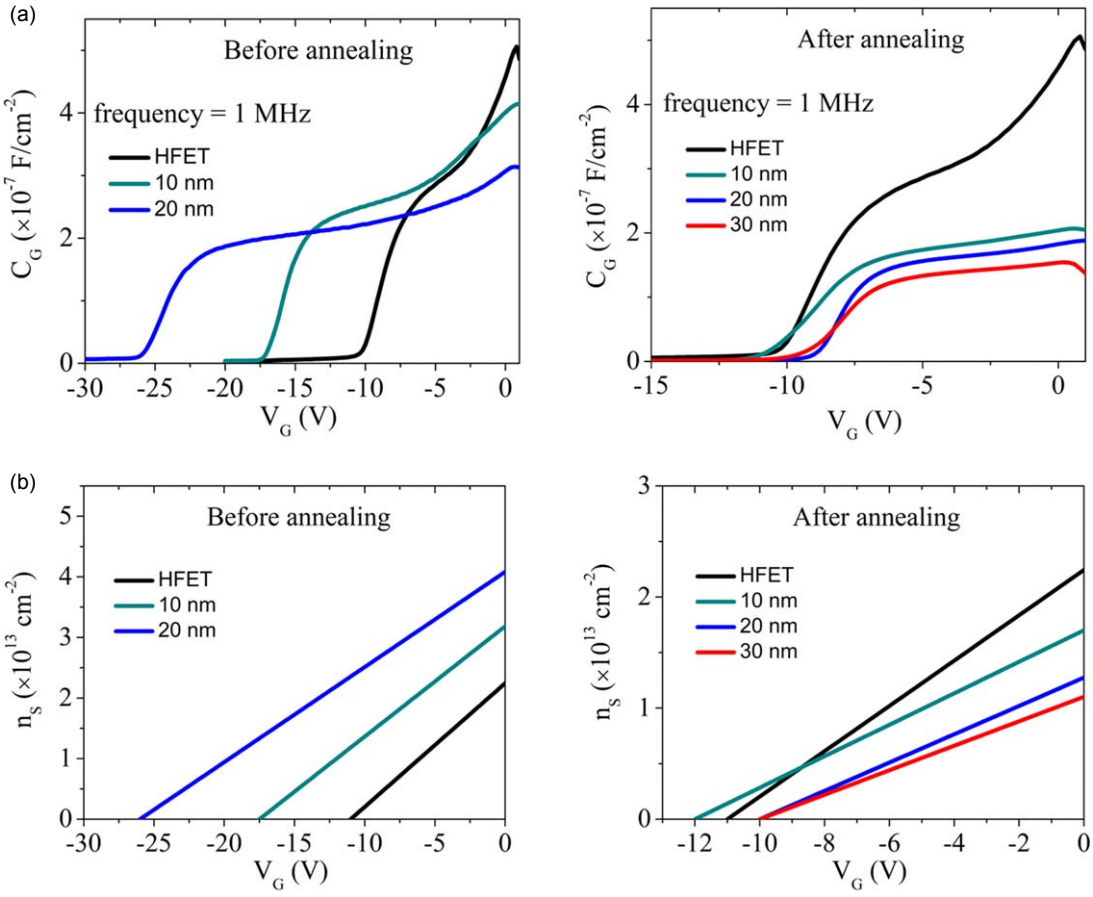


**Fig. 2.** (Color online) (a) *C–V* characteristics of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ HFET and MOSHFETs before and after annealing (b) 2DEG carrier density as a function of gate voltage of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ HFET and MOSHFETs before and after annealing.

**Table I.** Summary of MOSHFET device characteristics with different $ZrO_2$ thickness before and after the 300 °C anneal.

| | HFET | 10 nm | | 20 nm | | 30 nm | |
|---|---|---|---|---|---|---|---|
| | | Before | After | Before | After | Before | After |
| $I_D$ (A mm$^{-1}$) | 0.24 at $V_G = +2$ V | 0.55 at $V_G = +8$ V | 0.509 at $V_G = +8$ V | 0.558 at $V_G = +12$ V | 0.515 at $V_G = +12$ V | 0.595 at $V_G = +15$ V | 0.504 at $V_G = +18$ V |
| $I_G$ (A) | $5 \times 10^{-6}$ at $V_G = -20$ V | $6 \times 10^{-11}$ at $V_G = -20$ V | $8 \times 10^{-9}$ at $V_G = -20$ V | $1.1 \times 10^{-9}$ at $V_G = -20$ V | $4 \times 10^{-11}$ at $V_G = -20$ V | $1.7 \times 10^{-9}$ at $V_G = -40$ V | $1.5 \times 10^{-9}$ at $V_G = -40$ V |
| Off-state current (A) from transfer curve | $2 \times 10^{-6}$ | $4 \times 10^{-9}$ | $6 \times 10^{-9}$ | $5 \times 10^{-7}$ | $2 \times 10^{-11}$ | $2 \times 10^{-7}$ | $6 \times 10^{-10}$ |
| $V_T$ (V) | −10.8 | −20.8 | −13.1 | −25.5 | −12.1 | −33.7 | −12.2 |
| SS (mv decade$^{-1}$) | 378 | 252 | 210 | 575 | 105 | 255 | 116 |
| $N_s$ (cm$^{-2}$) | $2.2 \times 10^{13}$ | $3.2 \times 10^{13}$ | $1.7 \times 10^{13}$ | $4.08 \times 10^{13}$ | $1.3 \times 10^{13}$ | $4 \times 10^{13}$ | $1.1 \times 10^{13}$ |

the off-state for MOSHFETs (for all $t_{ox}$) is reduced by more than two orders as compared to the control HFET.

Post-deposition annealing showed drastic improvement in the $V_{TH}$ in all MOSHFETs where the biggest $V_{TH}$ shift occurs in 30 nm $ZrO_2$ from −33.7 to −12.2 V. Interestingly, after the anneal, $V_{TH}$ only showed a weak $t_{ox}$ dependence, suggesting that the interfacial charge $n_{ox,intf}$ has been significantly changed. The significantly lower negative $V_{TH}$ translated to a reduction in the on-state 2DEG $n_s$ from $\sim 2$–$3 \times 10^{13}$ to $\sim 1 \times 10^{13}$ cm$^{-2}$, in rough proportion to the $V_{TH}$ shift. The off-state current, determined primarily by gate leakage,[31] decreased further for the thicker oxides to $\ll$1 nA, $\sim 10^3$ reduction from that for the HFET. The off-state current for the thinnest 10 nm oxide increased slightly, although it remained in the nA range. We ascribe this unusual outlier to a dramatic change in the $ZrO_2$/AlGaN interface, $n_{ox,intf}$, which we will discuss further when quantifying the various charges responsible for the $V_{TH}$ shifts. As expected, the 2-terminal gate-source leakage characteristics showed a behavior similar to that of the off-state leakage current (Fig. S4).

The subthreshold swing (SS) for MOSHFETs (all $t_{ox}$) improved significantly after annealing to a value as low as 105 mV decade$^{-1}$ for the device with 20 nm thick $ZrO_2$. The improvement in SS is primarily due to the reduction in gate leakage described above, with high gate leakage masking the channel current at the lowest levels. We believe, the ALD oxide annealing lowers the interface trap density leading to reduced hysteresis and improved SS values.[32]

To separate the influence of $n_{ox,bulk}$ and $n_{ox,intf}$, $V_{TH}$ of unannealed and annealed MOSHFETs are plotted as a function of $t_{ox}$ in Fig. 4(a). In Eq. (1) $V_{TH}$ is described by a quadratic polynomial of $t_{ox}$ where the linear term gives $n_{ox,intf}$ while the quadratic term gives $n_{ox,bulk}$. A second order polynomial fit to the experimental $V_{TH}$ versus $t_{ox}$ gave excellent agreement with the equation. The $n_{ox,bulk} = +2.5 \times 10^{19}$ cm$^{-3}$ in unannealed MOSHFETs decreases only slightly to $+1.7 \times 10^{19}$ cm$^{-3}$ after annealing. In contrast, annealing flipped the polarity of the large $n_{ox,intf} = +5.5 \times 10^{13}$ cm$^{-2}$ to $n_{ox,intf} = -4.2 \times 10^{13}$ cm$^{-2}$, a very large change of $\sim(-10^{14}$ cm$^{-2})$. In bulk oxide, most positive negative dipoles cancel each other, thus interface charges constitute the main charge related to the dielectric layer.[33] We speculate that, annealing switches the polarity of the dipoles thus the net charge density at the interface becomes $-4.2 \times 10^{13}$ cm$^{-2}$ after annealing as opposed to $+5.5 \times 10^{13}$ cm$^{-2}$ in the case of the unannealed condition. Figure 4(b) shows the band diagram with the locations of these charges in the structure. This large negative $n_{ox,intf}$ induced by post-deposition annealing at 300 °C is responsible for partially depleting the channel 2DEG, reducing $n_s$, and making $V_{TH}$ less negative. This reduced $n_s$, we believe is also responsible for the ∼20% decrease in the peak drain current that was observed after the 300 °C annealing. However, this is much lower than the 2–3× decrease in $n_s$, indicating that because of the annealing, the channel mobility may have increased ∼2×. In the past, we studied the electron mobility of ultrawide bandgap HFETs and MOS-HFETs with different high-k dielectric layers.[26] Although the mobility temperature dependencies differed for HFET and MOSHFETs, the typical mobility range was the same for both device types. In this work, we used two-step PDA, which we believe is the main difference leading to mobility enhancement. The physical mechanism for mobility increase is the improved morphology of the dielectric and barrier layers and dielectric-barrier-channel interfaces, which, in turn, reduces interface scattering of the 2DGE electrons.

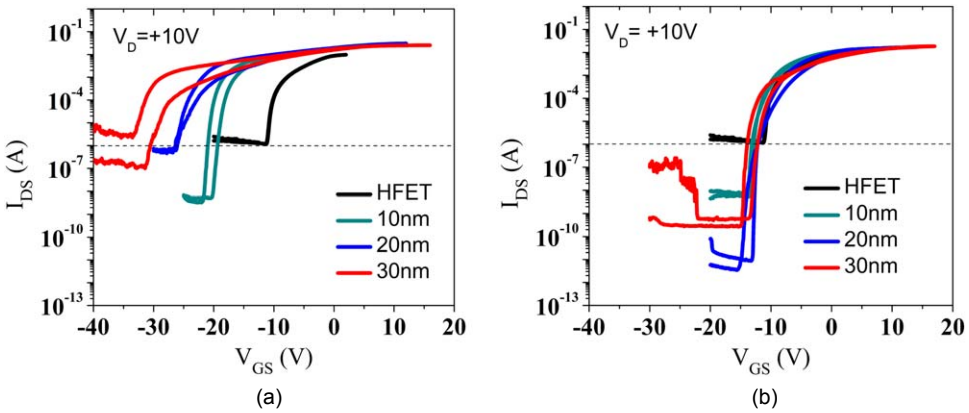


**Fig. 3.** (Color online) Double sweep transfer (IDS-VGS) characteristics of HFET and high-$k$ $ZrO_2$ MOSHFETs before (a) and after (b) 300 °C annealing.

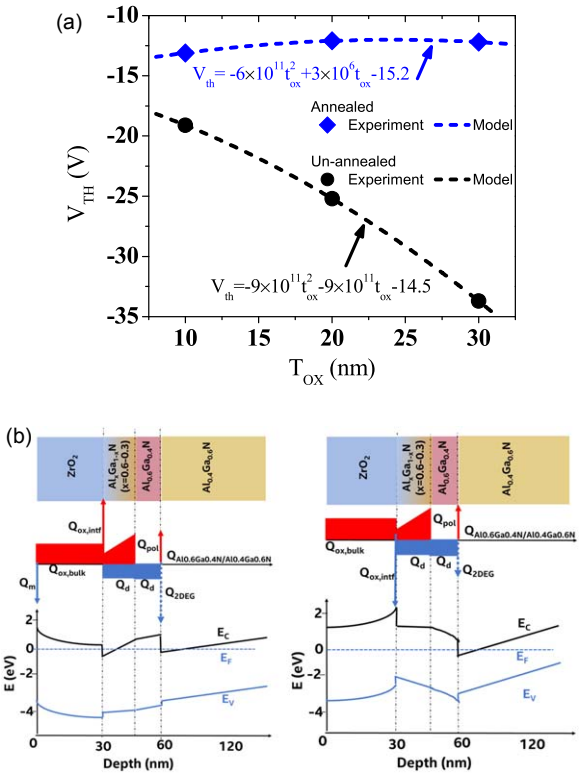


**Fig. 4.** (Color online) (a) $V_{TH}$ of unannealed and annealed MOSHFETs with $ZrO_2$ thickness of 10, 20 and 30 nm. The dots show experimental value and dashed lines show fitting to analytical model. (b) Band diagram of $Al_{0.6}Ga_{0.4}N/Al_{0.4}Ga_{0.6}N$ MOSHFET showing the location and polarity of bulk and interface charges before (left) and after (right) annealing. $Q_d$, $Q_m$, $Q_{pol}$ represent the doping charge, metal charge and polarization charge, respectively, while others have their typical meaning.

In summary, we demonstrate a 2× improvement in channel current using post-deposition annealing of the ALD $ZrO_2$ gate dielectric in UWBG AlGaN-channel MOSHFETs. The annealing mostly eliminated negative threshold voltage shift caused by the dielectric layer and enabled operation at high forward gate bias, up to +18 V compared to +2 V for the Schottky gate HFET, as a result doubling the HFET maximum channel current. Our anneal process also reduced the off-state leakage, improved the SS, while bringing $V_{TH}$ into a range useful for practical applications. We show the improvement to be primarily due to a large change in fixed charge density at the $ZrO_2$/AlGaN interface induced by the annealing. The resulting $n_{ox,intf} = -4.2 \times 10^{13}$ cm$^{-2}$ partially depleted the channel 2DEG to bring $V_{TH}$ under control, while maintaining the current handling and the extremely low gate leakage currents. This paper shows the viability of $ZrO_2$ gate dielectrics for UWBG AlGaN-channel MOSHFETs for high-power applications.

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