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Low temperature, highly stable ZnO thin-film transistors

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ABSTRACT

A low-temperature and straightforward fabrication process for ZnO thin-film transistors (TFTs) with near-zero aging and negligible instability enabled by using an ultrathin oxide as a top-passivation layer is demonstrated. The process features bottom-gate top-contacts ZnO TFTs with ultrathin HfO_2 or Al_2O_3 as passivation layers on top of the TFT followed by post-fabrication annealing (PFA). Devices with ultra-thin capping films of Al_2O_3 followed by a 150 °C PFA show threshold voltage shift (ΔV_{TH}) of <1% after bias stress and negligible shift after aging. The devices show saturation threshold voltage ($V_{TH\text{-}SAT}$) of 2.70 V, saturation mobilities larger than 10 cm^2/V·s, and current I_{ON}/I_{OFF} ratios $>10^6$. On the contrary, devices without nanofilm show similar performance to those with Al_2O_3 but show more considerable instability to aging and bias stress ($\Delta V_{TH} > 5\%$). Also, devices with HfO_2 as a capping layer shows severe instability ($\Delta V_{TH} > 40\%$). A degradation mechanism to explain the improved aging and reliability performance is also discussed.

1. Introduction

Thin Film transistors based on oxides show superiority concerning silicon transistors in processing temperature, transparency, and compatibility with roll-to-roll and large-area fabrication processes. These advantages have generated much attention in the transparent and flexible electronics field to develop various applications. In general, the primary heralded alternative to conventional amorphous silicon TFT technology is the metal-oxide semiconductors, and some of the most promising oxides include ZnO, [1] InZnO, [2,3] ZnSnO, [4,5] and InGaZnO. [6,7] However, metal-oxide TFTs still show instabilities, such as instability induced by ambient, positive and negative bias, temperature, and light. This instability is usually due to carrier concentration changes in the metal-oxide from the adsorption and further chemical reaction with moisture (H_2O) and oxygen (O_2) from the ambient [8–11] or during the TFT fabrication. [9,12–15] Furthermore, the electric field applied during typical TFT operation might accelerate the adsorption, migration, and diffusion of O_2 and H_2O, enhancing the TFT instability. [7,16]

The demonstration of low-temperature and stable oxide-based thin-film transistors without further increasing the fabrication complexity is highly desirable. Relatively simple approaches such as depositing a protective layer on the metal-oxide-semiconductor surface exposed to the atmosphere have been evaluated, such as inorganic passivation/protection (SiO_2, SiN_x). Still, these films' deposition degrades the semiconductor due to the harsh processing environments and required temperatures [17–22]. Regularly, the reduction of degradation occurs using extended high-temperature post-deposition annealing. [19,23] Nevertheless, the annealing limits the technology's application to rigid substrates and limits oxide semiconductors' to high temperatures. Organic films have also been used to improve metal-oxide stability, but the uniformity and homogeneity of these organic films are challenging to control, resulting in instability in device performance. [16,24–27]

In this work, ultrathin inorganic (HfO_2, Al_2O_3) nanofilms (referred to as NF in the manuscript) deposited on top of fully fabricated nanocrystalline-ZnO based TFTs are investigated, and the resulting performance and reliability systematically evaluated to enable thin-film transistors with $\Delta V_{TH} < 1\%$ after bias stress, negligible aging, $V_{TH\text{-}SAT}$ of 2.7 V, saturation mobilities larger than ten cm^2/V·s, and current I_{ON}/I_{OFF} ratios $>10^6$. The conduction band offset (CBO) is about ~2.2 eV [28,29] and ~ 3.0 eV [28,30] for HfO_2/ZnO and Al_2O_3/ZnO, respectively. The band gap for ZnO, HfO_2, and Al_2O_3 are 3.2, 5.6, and 7.0 eV, respectively [31–33]. In addition, the electron and hole effective masses are close to the following values: (a) ZnO are $m_e^* = 0.3\ m_0$ and $m_h^* = 0.59\ m_0$; (b) Al_2O_3 are $m_e^* = 0.4\ m_0$, and $mh^* = 6.0\ m_0$ [34]; and (c) HfO_2 are $me^* = 0.11\ m_0$ and $mh^* = 0.58\ m_0$ [35,36], however, they

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could be as heavier as me* = 1.91 m_0 and mh* = 9.9 m_0 in a cubic cell [37]. All these values are referenced concerning the electron-free mass, m_0.

2. Materials and methods

The fabrication of the thin-film transistors occurred with conventional photolithography. Fig. 1a shows the TFTs' plan view image, while Fig. 1b shows a 3D representation. The substrate is glass coated with 100 nm of Indium-tin-oxide (ITO) with resistivity $<6.8 \times 10^{-4}$ Ω•cm. Before the dielectric deposition, the ITO surface is treated with oxygen-based reactive-ion-etching (RIE) to eliminate any contamination. Immediately after the RIE treatment, 15 nm of Al_2O_3 are atomic layer deposited (ALD) with a substrate temperature of 100 °C. Trimethylaluminum and water are the precursors. Next, ZnO (50 nm) is pulsed laser deposited. The substrate temperature and O_2 partial pressure are 100 °C, and 2.67 Pa, respectively. The ablation occurred with a calibrated energy density of 1 J/cm^2. Source and drain electrodes are then defined by thermal evaporation of aluminum (100 nm) and patterned. Finally, each transistor's ZnO channel is isolated from neighbor devices using a wet etching process (Fig. 1b). TFTs are referred to as "as-fabricated" up to this step. Finally, the sample is divided into four pieces for the NF deposition with either none, HfO_2 (10 nm, 100 °C), or Al_2O_3 (10 nm, 100 °C). Fig. 1c shows a cross-section of the TFTs with the nanofilm.

The nanofilms are atomic layer deposited. Before the deposition process, the chamber pressure was controlled to 67 Pa using a constant N_2 flow. Water vapor serves as the oxygen source, whereas trimethylaluminum (TMA, 97% purity) and tetrakisdimethylamido hafnium (TDMAHf, 99.99% purity) are the metal-organic precursors for aluminum and hafnium, respectively. The pulse times were 15, 15, 50 ms for water, TMAH, and TDMAHf precursors, respectively. The purge time is 60 s for metal-organic precursors and 20 s for water. A total of 110 cycles results in 10 nm of both inorganic films. Following the nanofilm deposition step, the samples were annealed in a 90/10% N_2/O_2 atmosphere at 150 °C and 250 °C for 1 h.

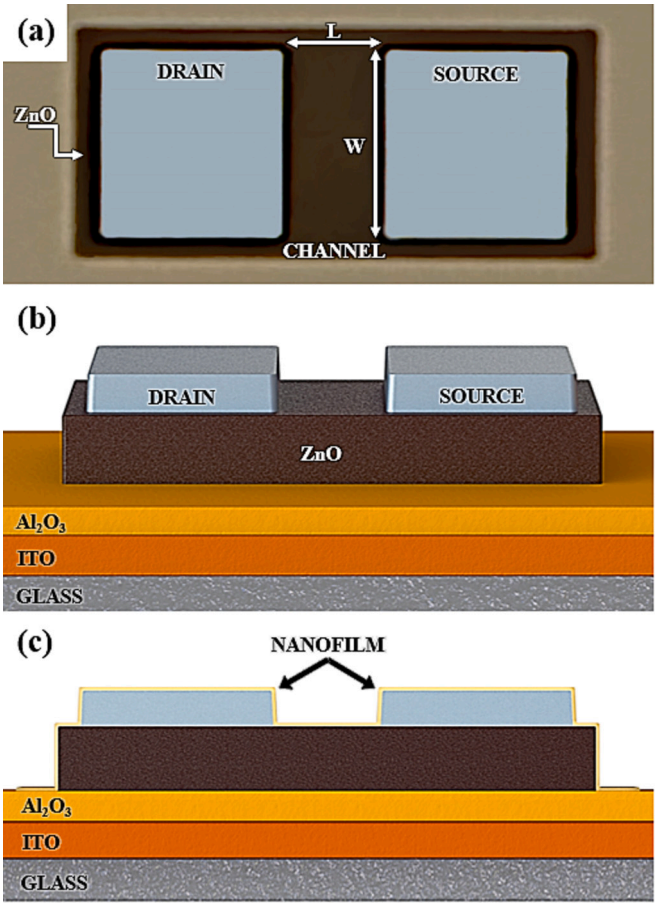

Fig. 1. (a) Microscope top view image and (b) 3D illustration of the fabricated TFTs without nanofilm. (c) Cross-section illustration of the TFTs with top nanofilm. The top nanofilm encapsulates ZnO, source, and drain.

The devices' characterization occurred at room temperature (RT), dark, and air environment using a Keithley 4200-SCS semiconductor parameter analyzer. The reliability analyses were performed applying 5 V to the gate (V_{GS}) and drain (V_{DS}) simultaneously for 600 s. The stress was interrupted with interspersed I_{DS}-V_{GS} data characteristics collected from $V_{GS} = -1.5$ to 5 V and $V_{DS} = 5$ V, along with a pre-stress I_{DS}-V_{GS} collected just before bias stressing. To further study the barrier properties, aging was induced by further annealing the samples at 100 °C for 1 h in 90/10% N_2/O_2. The study of the nanofilms' structure occurred using grazing angle X-ray (GIXRD) with a monochromatic copper source (Cu Kα1 1.54056 Å) and an incidence angle of 0.5°.

3. Results and discussion

The as-fabricated ZnO TFTs without nanofilm nor PFA are used as the reference devices for the results and discussion. The I_{DS}-V_{DS} for these devices ($W/L = 100/40$) is shown in Fig. 2a and the normalized (W/L) transfer characteristics in Fig. 2b. The transfer characteristics are precisely the same indicating negligible parasitic effects. The current ratio (I_{ON}/I_{OFF}) is more significant than 10^8, with leakage current in the range of 10^{-13} A.

The saturation threshold voltage ($V_{TH\text{-}SAT}$) and the saturation mobility (μ_{SAT}) are calculated by linear fitting the $I_{DS}^{0.5}$ vs. V_{GS} plot for $V_{DS} > V_{GS} - V_{TH\text{-}SAT}$. [38] The right axis in Fig. 2b shows the linear fit using Eq. 1. The extracted $V_{TH\text{-}SAT}$ and μ_{SAT} are 2.7 ± 0.1 V and 13.3 ± 0.4 cm^2/V·s, respectively. The subthreshold swing obtained using eq. 2 is 204 ± 12 mV/DEC.

$$I_{DS} = \frac{\mu_{SAT} C_{OX} W}{2L}(V_{GS} - V_{TH-SAT})^2 \quad (1)$$

$$SS = \frac{dV_{GS}}{d(\log I_{DS})}\bigg|_{Max} \quad (2)$$

Fig. 3a compares as-fabricated (open squares) transfer characteristics to devices with the nanofilms before PFA. Neither $V_{TH\text{-}SAT}$ nor μ_{SAT} are significantly affected by the NF; however, both I_{OFF} and the SS increase for TFTs with NF. In our device configuration, due to the full depletion of electrons in the channel, the I_{OFF} is defined by the ultra-thin ZnO (i.e., ZnO thickness). Thus, I_{OFF} can potentially be affected by conduction near the top of ZnO. Therefore, the ΔI_{OFF} and ΔSS can be correlated to changes in the density of trap states, not solely at the bottom-channel interface but also positive charges at the top (TP), close to the S/D. The increase in I_{OFF} indicates the formation of a top conductive channel because of the NF deposition, which affects the performance of as-fabricated TFTs. It is important to note that the NF deposition is at low temperature and might have a more fixed positive charge, thereby inducing the top channel as reflected in the higher I_{OFF} in Fig. 3a. [19]

The structural properties of the NF are in Fig. 3 (e - g). The as-fabricated ZnO is polycrystalline and has a wurtzite structure with a (0002) preferential orientation (JCPDS # 36–1451), as in Fig. 3e. On the other hand, Al_2O_3 and HfO_2 show amorphous and polycrystalline structures, respectively. HfO_2 has a broad peak around 32.7° corresponding to the (111) monoclinic unit cell (JCPDS # 06–0318).

3.1. Device behavior after post-fabrication anneal (90/10 N_2/O_2)

As discussed in the experimental section, a post-fabrication anneal (PFA) is performed at either 150 or 250 °C for 1 h. in 90/10 N_2/O_2 ambient to reduce any defects introduced during the NF deposition.

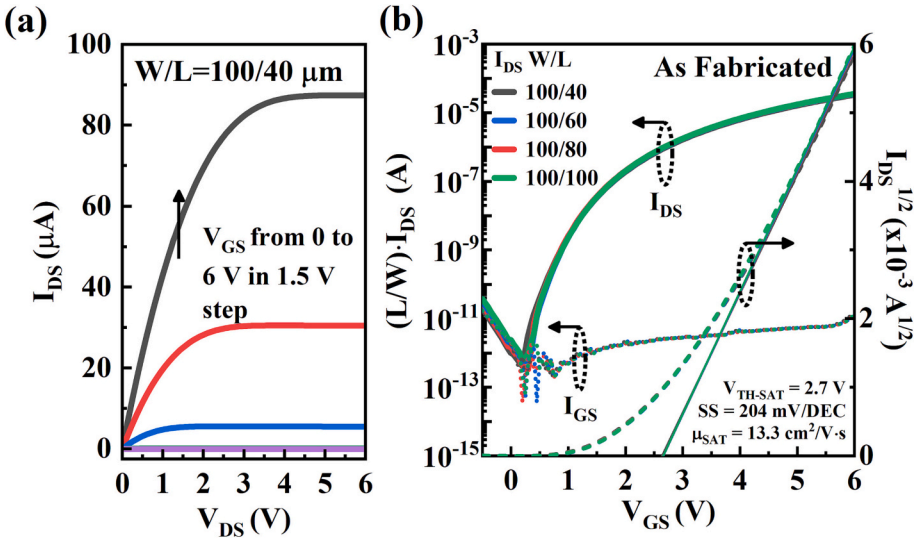

Fig. 2. Electrical performance of the reference ZnO TFT (without-top nanofilm and no-post-fabrication anneal). (a) I_{DS} vs. V_{DS} Output characteristics of a $W = 100$ and $L = 40$ μm. (b) Representative transfer characteristics of 4 different ZnO TFTs geometries. Dotted lines represent gate current (I_{GS}).

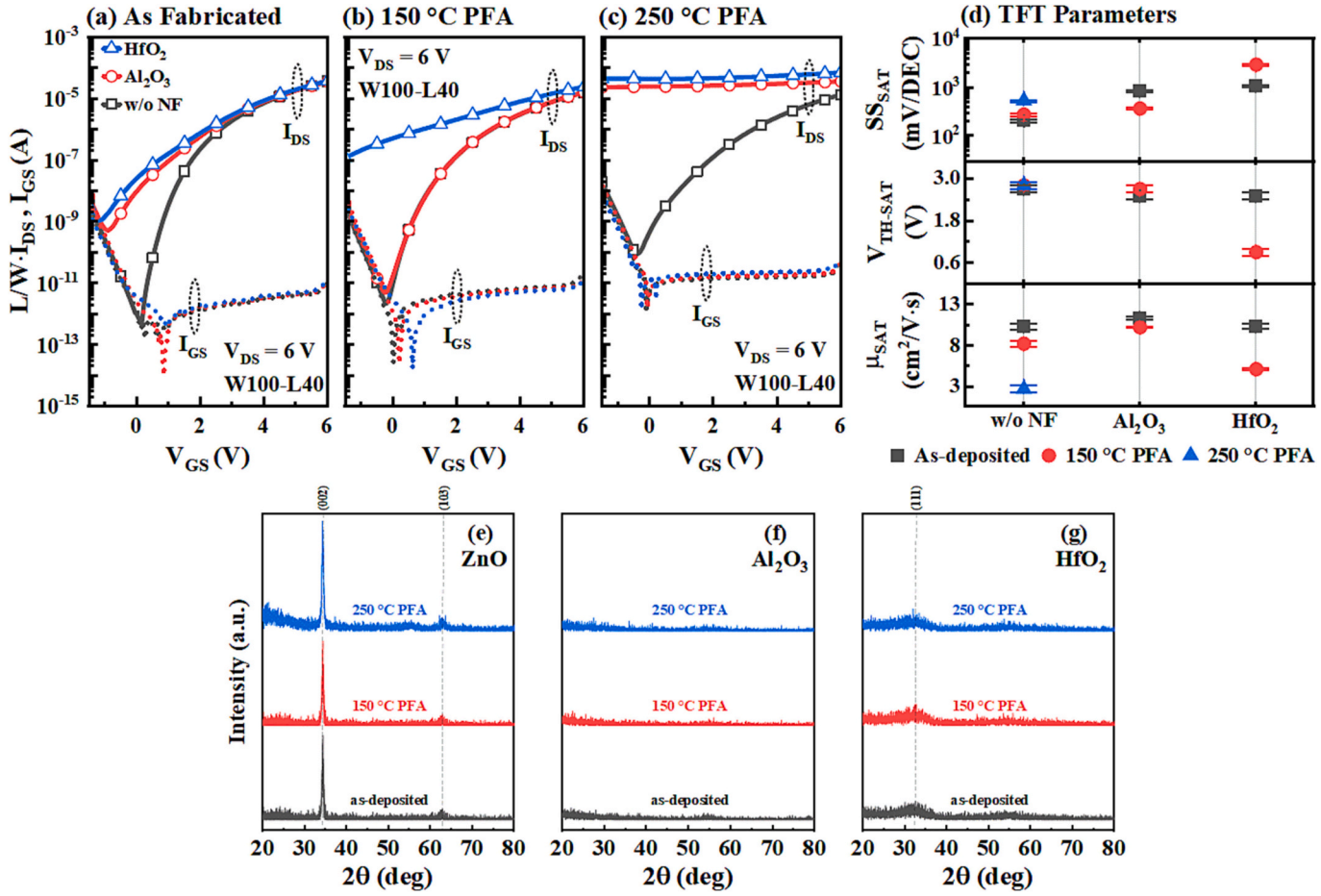

Fig. 3. I_{DS} vs. V_{GS} transfer characteristic under different top nanofilm conditions (no-bias stress): (a) as fabricated, (b) 150 °C, and (c) 250 °C post-fabrication anneal (PFA). (d) V_{TH-SAT}, μ_{SAT}, and SS_{SAT} parameters as a function of the nanofilm condition for different PFA (Each point is the average of 45 devices, Standard deviation is also shown in the figure). The degradation of the TFT performance with 250 °C PFA is probably due to both interfaces' deterioration. (e) to (g) XRD results for ZnO, Al_2O_3, and HfO_2 with and without PFA.

Fig. 3 (b) and (c) show the I_{DS}-V_{GS} characteristics for devices after 150 °C and 250 °C PFA, respectively. The extracted TFT parameters for samples with PFA are shown in Table 1.

The V_{TH-SAT} increases from 2.7 to 2.8 V for devices without the NF and 150 °C PFA. Also, there is no significant change in threshold voltage after 250 °C PFA, when compared to 150 °C. I_{OFF} slightly increases with

Table 1
Relation of device performance as a function of top nanofilm and post-annealing condition.

Parameter	No Post Deposition Anneal			150 °C PFA			250 °C PFA		
	w/o NF	Al_2O_3	HfO_2	w/o NF	Al_2O_3	HfO_2	w/o NF	Al_2O_3	HfO_2
$V_{TH\text{-}SAT}$ (V)	2.7 ± 0.1	2.5 ± 0.1	2.5 ± 0.1	2.8 ± 0.1	2.7 ± 0.1	0.9 ± 0.1	2.8 ± 0.1	–	–
[1] V_{TE} (V)	2.2 ± 0.1	2.1 ± 0.1	2.1 ± 0.1	2.7 ± 0.1	2.6 ± 0.2	2.1 ± 0.1	3.6 ± 0.1	–	–
μ_{SAT} (cm^2/V•s)	13.3 ± 0.4	11.3 ± 0.2	10.3 ± 0.3	8.2 ± 0.4	10.2 ± 0.1	5.1 ± 0.1	2.7 ± 0.4	–	–
μ_{FE} (cm^2/V•s)	17.4 ± 0.4	15.5 ± 0.7	14.3 ± 0.6	11.6 ± 0.7	13.9 ± 0.2	12.1 ± 0.2	4.1 ± 0.1	–	–
SS_{SAT} (mV/DEC)	204 ± 12	828 ± 40	1060 ± 46	271 ± 16	361 ± 17	2883 ± 98	520 ± 28	–	–
SS_{LIN} (mV/DEC)	181 ± 7	1052 ± 21	1330 ± 22	254 ± 16	319 ± 18	2975 ± 51	570 ± 27	–	–
$R_{SH\text{-}ON}$ (Ω/□)	4.4×10^4	4.9×10^4	4.7×10^4	7.0×10^4	6.0×10^4	6.1×10^4	2.1×10^5	–	–
$R_{SH\text{-}OFF}$ (Ω/□)	4.3×10^{12}	4.2×10^7	1.8×10^7	2.8×10^{10}	4.7×10^9	1.9×10^6	1.3×10^9	–	–

[1] V_{TE} is the threshold voltage extracted from the extrapolation of the linear portion of the I_{DS}-V_{GS}, from maximum slope to zero current for small V_{DS} voltages (V_{DS} = 0.1 V).

annealing temperature, and SS_{SAT} increases 32.8% and 154.9% after 150 and 250 °C PFA, respectively. The increase in *SS* indicates the filling of trap states near the bottom of the ZnO. These trap states can be a result of the formation of oxygen vacancies, [39–41] hydrogen [42,43], carbon [44,45], or roughness induced defects due to substrate instabilities [38] at the bottom-channel. This increase in the density of interface traps causes an increase of the Coulomb scattering, which causes a decrease in electron mobility, as observed in Fig. 3d.

Devices with Al_2O_3 NF followed by 150 °C PFA show two orders of magnitude decrease in I_{OFF}, a reduction of 56% in *SS*, and an 8% increase in $V_{TH\text{-}SAT}$ compared to the reference samples. This result indicates that the anneal reduced positively fixed, thereby mitigating the top conductive channel. [46]

For devices with HfO_2 NF, the I_{OFF} increases two orders of magnitude, and *SS* increases 172%, after 150 °C PFA compared with the reference samples but shows a negative $V_{TH\text{-}SAT}$ shift of ~2 V. This denotes the addition of positive oxide charge. Impurities likely cause this additional charge from the low-temperature deposition process.

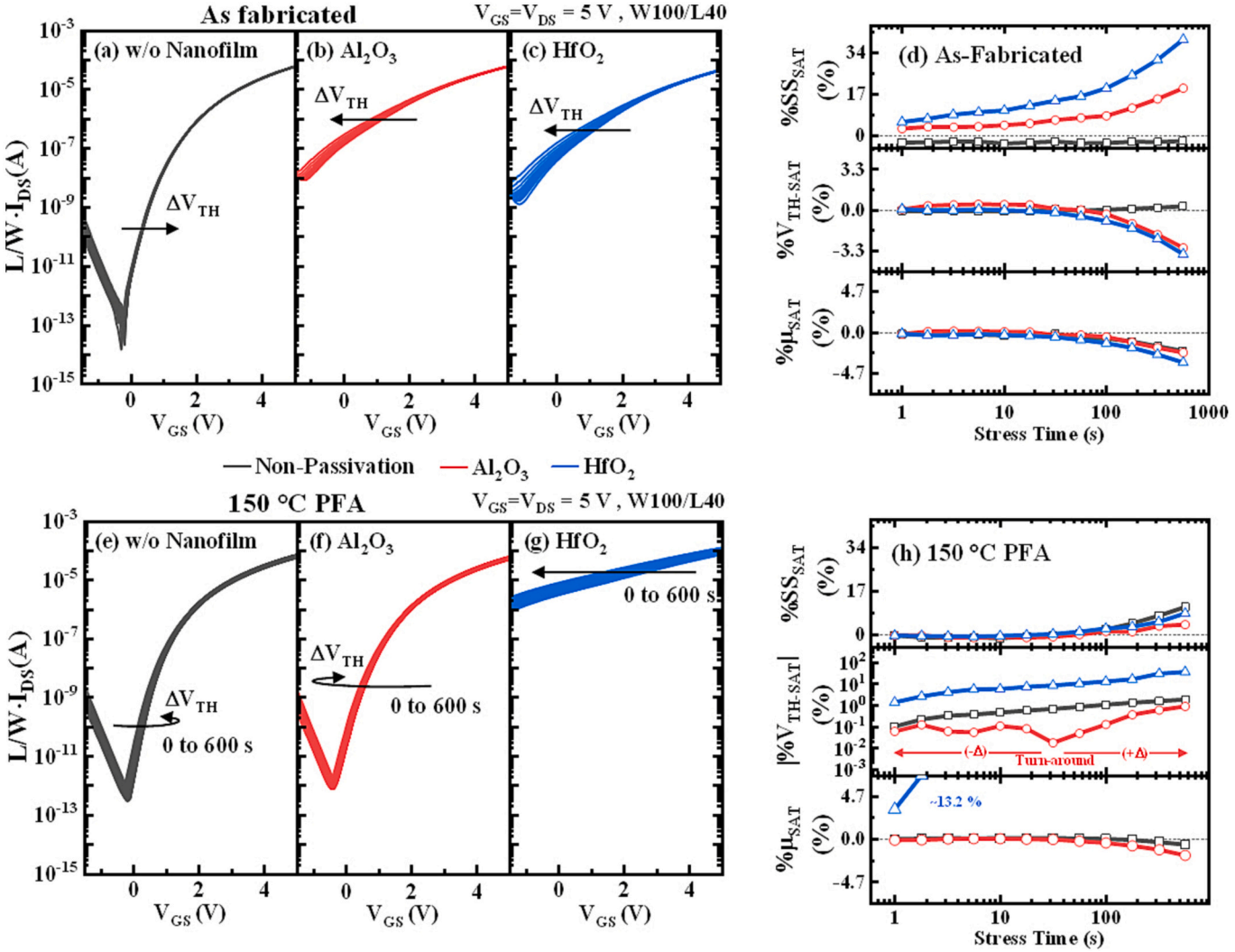

Fig. 4. Typical transfer characteristics for bias stress ($\underline{V_G} = \underline{V_D} = \underline{5}$ V). (a) to (c) are for the as-fabricated devices; (e) to (g) are for 150 °C PFA; (d) and (h) shows the time evolution of the percentage changes in $V_{TH\text{-}SAT}$, μ_{SAT}, and SS_{SAT} parameters for as fabricated and after 150 °C PFA, respectively.

Contrary to Al_2O_3, these impurities can readily diffuse in HfO_2 NFs due to its nanocrystalline character. [47,48] These positively charged contaminants are likely located in close proximity to the NF/ZnO interface resulting in the formation of a top conductive layer [39,49–52] and increasing the carrier concentration in ZnO, resulting in negative ΔV_{TH}. It is important to note that there is no degradation in the drain saturation current in the 4–6 V range (Fig. 3 a-b). The fact that the drain current is not reduced, even with the increase in *SS* and I_{OFF}, demonstrates top channel conduction and requires a more negative gate voltage to turn the TFT off. [46] If there are generated defects acting as interfacial traps that increased *SS* and I_{OFF}, then there would have been a noticeable decrease in the drain saturation current, as typically seen in the literature. [53,54] Devices with Al_2O_3- and HfO_2- nanofilms show severe degradation after 250 °C PFA. This degradation could be due to the diffusion of atoms at the interface semiconductor/dielectric, leading to oxygen vacancies and hydrogen or carbon diffusion. [39,42,51,55,56]

3.2. Device stability under a positive bias stress

The 250 °C PFA is detrimental to all the devices regardless of NF; thus, they were not further analyzed. However, the sample with 150 °C PFA and Al_2O_3 NF show substantial improvement from its as fabricated counterpart. Next, bias stress studies are used to study the NF's impact on device stability and reliability for not annealed and 150 °C PFA devices. The figure of merit for the analyses is the percentage threshold voltage shift ($\%V_{TH\text{-}SAT}$) measured concerning the initial or $t = 0$ s value. Similar calculations were used for $\%SS$ and $\%\mu_{SAT}$. Fig. 4 (a) to (c) shows the representative transfer characteristics, while Fig. 4d shows the change of the figure of merits with stress time for the as-fabricated samples.

3.2.1. Bias stress in unannealed devices

The positive $\%V_{TH\text{-}SAT}$ of the reference sample (Fig. 4a) indicates that negative charge trapping occurs in the bottom-channel with minimum or negligible impact due to the top channel. States responsible for trapping can be either interface states, oxide/ dielectric states, or both. The $\%SS$ is not affected in TFTs without NF; therefore, the dominant $\%V_{TH\text{-}SAT}$ mechanism in these devices is due to oxide trapped states. This mechanism is also present in TFTs with NFs, given that all devices have the same MOS structure. However, the magnitude and direction of $\%SS$ and $\%V_{TH\text{-}SAT}$ are different, suggesting that the NF, and ultimately the top channel, play an essential role in the degradation mechanism. [39]

The $\%V_{TH\text{-}SAT}$ is negative in TFTs with Al_2O_3- (Fig. 4b) and HfO_2- (Fig. 4c) nanofilm, indicating an increase in positive charge concentration. The change of I_{OFF} also suggests a more conductive channel, while the ΔSS hints that the charge is near the interface under these bias stress conditions. This charge might be due to generated defects at the top-channel and near the drain with the prolonged bias stress. [57] Because $|\%V_{TH\text{-}SAT}|$ in HfO_2 is bigger than Al_2O_3, the charge trapping density is more significant in HfO_2. This concentration difference can be related to the nanocrystalline and amorphous character of HfO_2 and Al_2O_3, respectively (Fig. 3).

3.2.2. Bias stress after 150 °C post-fabrication anneal

Representative transfer characteristics after stress for the TFTs after 150 °C PFA are in Fig. 4 (e) to (g). The quantification of changes in device performance is in Fig. 4h. For non-passivated devices, the $\%V_{TH\text{-}SAT}$ is positive for the initial 100 s, suggesting that the instability is due to negative-charge accumulation in the bottom A_2O_3/ZnO interface. This behavior is the dominant degradation mechanism of ZnO-based TFTs. [58] However, after 100 s of stress, $\%V_{TH\text{-}SAT}$ becomes negative, suggesting that a more conductive channel is forming. This can be due to the absorption of moisture, nitrogen, and carbon from the atmosphere in the exposed non-passivated top surface. These molecules can induce dangling bonds and vacancies during the prolonged bias stress, which overcomes the negative trapping occurring at the bottom interface.

Devices with HfO_2 (Fig. 4g) nanofilms show a negative $\%V_{TH\text{-}SAT}$, increased $\%SS$ and reduced $\%\mu_{SAT}$. This suggests that the top channel is becoming more conductive, creating additional degradation besides the negative charge trapping at the bottom channel. The polycrystalline character of these films can be beneficial for forming defects because of grain boundaries, resulting in considerable more charge accumulation.

On the contrary, devices with Al_2O_3-NF show the smallest $\%SS_{SAT}$ (+3.9%), $\%V_{TH\text{-}SAT}$ (+0.8%) and $\%\mu_{SAT}$ (−1.75%) (Fig. 4f). These devices show a unique turnaround effect. This behavior could be due to a competing mechanism that results in $\%V_{TH\text{-}SAT}$ neutralization. At the beginning of the stress, the top channel's increased conductivity dominates the degradation, resulting in a negative $\%V_{TH\text{-}SAT}$. The prolonged field applied during the bias stress can increase the concentration of defects at the top channel (dangling bonds and vacancies), but the amorphous character of the Al_2O_3 limits the creation of many new trap states, contrary to what is observed in HfO_2. Simultaneously, the conventional negative charge trapping mechanism occurs at the bottom interface, resulting in positive $\%V_{TH\text{-}SAT}$. The competition of these mechanisms at the top and bottom interfaces results in instability neutralization, as observed in Fig. 4f.

3.3. Device aging in air

The accelerated aging study consists of device annealing (100 °C, 1 h). Fig. 5 shows the TFT performance before and after aging. $V_{TH\text{-}SAT}$ and μ_{SAT} decrease 32.1% and 8.1%, respectively, for devices without NF. *SS* increases by 8.7%. The increase in I_{OFF} and *SS* after aging indicates an increase in trap states in the top channel. The negative change of $V_{TH\text{-}SAT}$ indicates a more conductive channel after aging. As mentioned, the adsorption of moisture and contaminants in the ambient onto the exposed ZnO surface can occur. These contaminants can be positively charged and shift $V_{TH\text{-}SAT}$ negatively by the accumulation of this charge.

Devices with Al_2O_3 NF show no deterioration in TFT performance after aging, as shown in Fig. 5b. Therefore, Al_2O_3 neutralizes the instability induced by prolonged bias stress and forms an excellent barrier against diffusion. This results in highly stable devices with excellent performance for large-area, low temperature, and novel electronic applications.

3.4. Proposed degradation mechanism

Fig. 6 shows the proposed mechanism for the behavior observed. Devices without NF (Fig. 6a) are affected by moisture and probably hydrocarbons in the air. These contaminants can adhere to the exposed ZnO channel's surface and induce the formation of a top-channel. The incorporation of the NF/protection layer blocks these molecules' adsorption onto the ZnO top surface, as shown in Fig. 6b. Nevertheless,

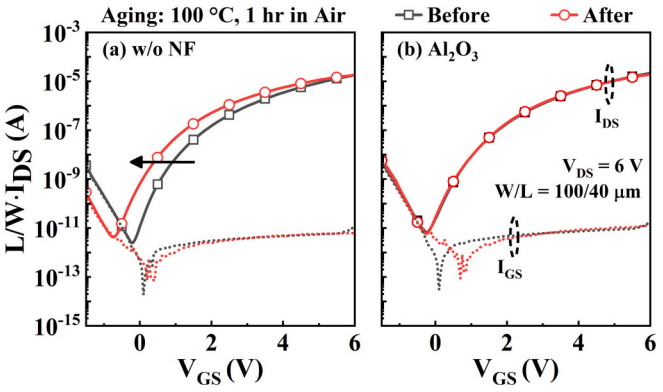

Fig. 5. Aging impact comparison for different samples: (a) Without top nanofilm, and (b) Al_2O_3 nanofilms. The reference used for each condition is the device with 150 °C PFA. Devices with Al_2O_3-NF show zero-aging induced shifting.

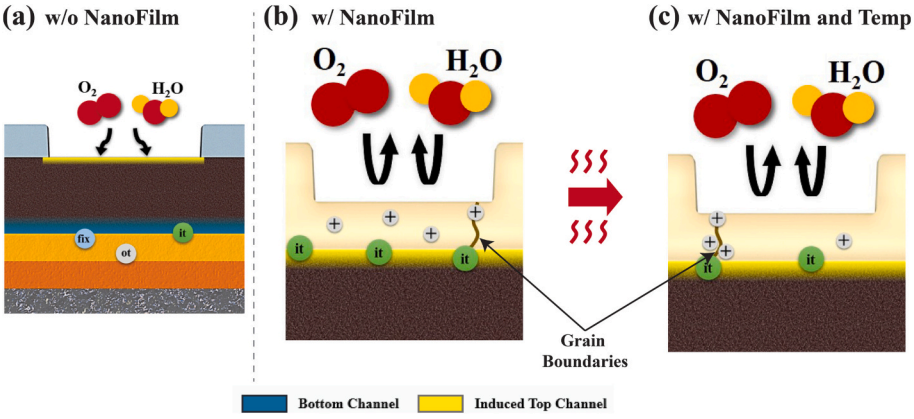

Fig. 6. Proposed instability mechanism for different top surface conditions and annealing/aging. The cross-section for the different conditions analyzed: (a) Without nanofilm; (b) with nanofilm; and (c) with nanofilm plus temperature influence. The top nanofilm (b) blocks the diffusion of molecules (a) in ambient (H_2O, N_2, O_2, etc.). The deposition of the top nanofilm induced the formation of a top channel [yellow in (b)] in addition to the modulated bottom channel [Blue in (a)]. The presence of grain boundaries [in (b) and (c)] enables migration of positive charge near the top interface resulting in devices with larger instability. IT = interface traps; + = oxide traps; V = oxygen vacancies. For Al_2O_3, the (b) and (c) grain boundary mechanism is substantially suppressed due to fewer grain boundaries than HfO_2. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

the addition of these low-temperature high-k dielectrics may inherently introduce a positive charge in the oxide, which causes the development of a conductive layer at the top surface. These positive charges in the NF would attract electrons from the ZnO, effectively creating a top-channel, similar to devices without top NF.

Despite the barrier effectiveness of the NFs used, the concentration of oxide traps can be affected due to temperature (PFA or aging), and it is clearly dependent on the material. The filling of trap states is limited in Al_2O_3 films, probably due to its amorphous structure, while the HfO_2 might increase due to its polycrystalline character. [59–61] The results from the deposition of an inorganic amorphous film demonstrate the balance between defects and vacancies that exist, as shown in this research. The presence of grain boundaries allows more migration of positive charges and lowers the quality of interfaces in close proximity to the top ZnO surface, resulting in devices with more substantial instability.

4. Conclusion

This work provides a novel method to enable a low-temperature and simple fabrication process for ZnO thin-film transistors (TFTs) with negligible aging and reduced instability after electrical stress. Devices with ultra-thin Al_2O_3 films followed by a 150 °C PFA show threshold voltage shift (ΔV_{TH}) of <1% after bias stress and negligible shift after aging for 1000 s with a saturation threshold voltage ($V_{TH\text{-}SAT}$) of 2.7 V, saturation mobilities larger than ten $cm^2/V{\cdot}s$, and current ratios $>10^6$. The results suggest that Al_2O_3 or HfO_2 deposition without PFA increases the conductivity at the top-channel interface, degrading device performance compared to devices without nanofilm. The neutralization of trapped charge occurs by performing a post-fabrication anneal. Annealing the devices at 250 °C severely impacts the TFT performance with and without top nanofilm, while a 150 °C annealing shows substantial improvement, particularly for Al_2O_3 nanofilms. The negligible $\Delta V_{TH\text{-}SAT}$ for Al_2O_3-nanofilms indicates a competing effect with negative trap states at the bottom-channel and positive trap states at the top-channel, resulting in effective charge neutralization increasing the device stability. With low-temperature fabrication, Al_2O_3 nanofilms are an excellent barrier for devices against ambient conditions. Furthermore, for the stress time used in this work, Al_2O_3 nanofilms limited the bias stress instability of devices. This result is remarkable for large-area electronic applications where prolonged or heavy usage could be achieved, even with fabrication that uses low-temperature processing.

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Credit author statement

- Rodolfo A. Rodriguez-Davila: Writing- Original draft preparation, Conceptualization, Methodology, Investigation, Formal Analysis.
- Richard A. Chapman: Data curation, Data Analysis, Investigation, Validation.
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- S. J. Castillo: Investigation, Editing, Supervision, Funding Acquisition.
- Chadwin D. Young: Supervision, Writing - Reviewing & Editing, Funding Acquisition.
- Manuel A. Quevedo-Lopez: Validation, Writing - Reviewing, Editing, Funding Acquisition.

Declaration of Competing Interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

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Data availability

Data will be made available on request.

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Appendix A. Supplementary data

Supplementary material: The PDF contains relevant information for the fabrication process flow, TFT layout and aspect ratios, Comparison of transfer characteristics in linear and saturation regimen. Supplementary data to this article can be found online at [https://doi.

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