Enhancement-Mode AlInN/GaN High-Electron-Mobility Transistors Enabled by Thermally Oxidized Gates

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***Abstract*— Enhancement mode AlInN/gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are fabricated by thermally oxidizing the barrier region under the gate. The oxidation is performed at 850 °C in O_2, and a SiN_x mask is used to achieve selective oxidization of the AlInN layer. For comparison, a standard Schottky gate and atomic layer deposition (ALD) Al_2O_3 metal–insulator–semiconductor (MIS) HEMTs are fabricated from the same structure and show depletion mode behavior as expected. Scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS) mappings are performed to characterize the gate of the oxidized HEMTs, showing complete oxidation of the AlInN barrier. All the devices are tested to determine their transfer and output characteristics. The results show that the thermally oxidized gate produces a positive shift in threshold voltage at ∼4 V and low currents (∼2×10^{-7} mA/mm) at zero gate voltage. The oxidized HEMTs are also subjected to postmetallization annealing (PMA) at 400 °C and 500 °C for 10 min flowing 1000 sccm of N_2, retaining enhancement mode behavior and leading to a further positive shift in threshold voltage.**

***Index Terms*— AlInN, enhancement mode, gallium nitride (GaN), high-electron-mobility transistors (HEMTs), thermal oxidation.**

I. Introduction

GALLIUM nitride (GaN) has promising intrinsic properties such as a high critical electric field, thermal stability, and transport properties, including high electron mobility and saturation velocity [1], [2]. These properties make GaN suitable for power semiconductor devices that require high operating voltages and temperatures. Recently, vertical GaN diodes and metal–oxide–semiconductor field-effect transistors (MOSFETs) have been realized with kilovolt breakdown performance grown on low-defect GaN substrates [3]. While the availability of GaN substrates continues to increase, they are still expensive and have small diameters, and therefore GaN devices with lateral topologies are more commercialized. This includes high-electron-mobility transistors (HEMTs) grown on cheaper and larger nonnative substrates such as Si, SiC, or sapphire. III-nitride HEMTs use a thin AlGaN or AlInN barrier layer on GaN to create a 2-D electron gas (2DEG) with high sheet electron concentration and mobility [4], which is advantageous for high-speed operation [5], [6]. They can also be used for high-power transistor operation using appropriate field termination schemes.

III-nitride HEMTs and metal–insulator–semiconductor (MIS) HEMTs operate normally-ON (or depletion mode), which is not ideal for high-power devices. Instead, normally-OFF (or enhancement mode) behavior is preferred, which allows for simpler gate control circuitry and power control [6]. Many techniques are used to create enhancement mode devices, including fluorine treatments, etching a recess under the gate, and selective regrowth of p-GaN or etching of a p-GaN layer to form a p-n junction under the gate [7], [8], [9], [10], [11], [12]. There are well-known challenges associated with these techniques, and the main drawbacks arise from surface contamination or damage during fabrication. For example, with recessed-gate MIS-HEMTs, etching under the gate introduces damage, which increases leakage currents. The deposited oxides used to suppress this gate leakage require surface pretreatments to remove contaminants such as oxygen, carbon, and silicon, which are present on exposed surfaces. Finally, etch controllability and uniformity are issues in addition to plasma-induced damage that must be addressed during fabrication [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. To avoid these problems, a less-developed approach to achieve enhancement mode operation is utilized by oxidizing the barrier layer under the gate to produce a positive shift in threshold voltage, V_{th}. For both AlGaN/GaN and AlInN/GaN HEMTs, native oxides have been used to form MIS-HEMTs in this manner. For AlGaN, oxidation at elevated temperatures produces thin oxide layers that are insulated with an oxidation rate of ∼1.2 nm/h [24], [25], [26]. Similar thin oxide layers have been used for AlInN barriers created via plasma or thermal oxidation [27], [28], [29]. The thermal oxidation of AlInN displays faster

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oxidation rates, ∼0.5 nm/min at 830 °C in O_2, and the ability to form thick insulating layers [30], [31], which can be leveraged in HEMT fabrication. In addition to more promising oxidation behavior, AlInN/GaN HEMTs also perform better at higher temperatures, can be grown lattice matched to GaN, and have higher sheet carrier densities [32], [33], [34], [35].

In this work, a standard AlInN/AlN/GaN structure is used to create an enhancement-mode HEMT by selective oxidization through the entire thickness of the AlInN barrier layer under the gate. Overall, this oxide serves two purposes. First, the AlInN under the gate is completely converted into an oxide, which depletes the 2DEG. Second, the formed gate oxide acts as an insulating layer to reduce gate leakage of the HEMT. Selective thermal oxidation of AlInN under the gate produces enhancement-mode HEMTs while avoiding surface exposure and contamination at interfaces under the gate [36], [37]. This report discusses the fabrication of enhancement-mode AlInN/GaN MIS-HEMTs with oxidized barrier gates and examines the effects of annealing on enhancement-mode behavior.

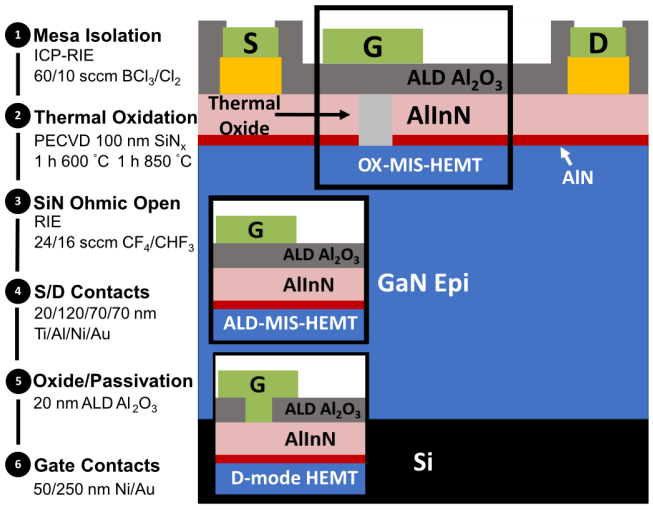

Fig. 1. Schematic cross-section of a thermally oxidized OX-MIS-HEMT with the fabrication steps on the left. The two insets show the gate structure for the ALD-MIS-HEMT and D-mode HEMT that are simultaneously processed for comparison.

II. Experimental Methods

A commercial AlInN/GaN HEMT structure is used, grown by metal-organic chemical vapor deposition (MOCVD) on silicon. It consists of a 700-nm-thick unintentionally doped GaN layer, a ∼1-nm AlN layer, and a 10-nm unintentionally doped $Al_xIn_{1-x}N$ ($x = 0.82$) barrier, which is lattice matched to GaN. An average sheet resistance of 280.49 Ω/sq. is measured across the wafer. The HEMTs are fabricated and characterized using standard fabrication techniques. Three different device topologies are fabricated in parallel. The first is a D-mode HEMT with Schottky gates, the second is an ALD-MIS-HEMT, and the third is a thermally oxidized barrier HEMT or OX-MIS-HEMT. First, a mesa is formed using inductively coupled plasma (ICP) etching to isolate electrical test structures and the various HEMT topologies. Typically, ohmic source and drain contacts are deposited and annealed after mesa etching. However, to prevent degradation of the ohmic contacts due to high temperatures needed during thermal oxidation, the first fabrication step is selective oxidation of the AlInN barrier layer for the OX-MIS-HEMT. Note that while the AlInN layer for the D-mode HEMT and ALD-MIS-HEMT are not oxidized, all the devices are subject to the same thermal budget throughout the processing. After the mesa etch, the sample is cleaned in 10:1 BOE, and a 100-nm-thick SiN_x masking layer is deposited via plasma-enhanced chemical vapor deposition (PECVD). The SiN_x is removed within a 5-μm-long region under the gate of the OX-MIS-HEMT using reactive ion etching (RIE). Selective thermal oxidation in the open SiN_x areas is performed in a dry environment with O_2. The oxidation is performed at two temperatures in a horizontal quartz tube furnace with an oxygen flow of ∼2800 sccm. The sample is oxidized at 600 °C for 1 h, ramped to 850 °C, and oxidizedfor an additional 1 h. This results in a ∼10-nm-thick oxide layer. After oxidation, the SiN_x masking layer is removed across all devices via RIE. During the RIE etch, the oxide layer is exposed and some surface etching of the oxide is observed. Next, the Ti/Al/Ni/Au metal stack is deposited and annealed at 850 °C for 1 min to form the source and drain ohmic contacts for all three topologies. A blanket 20-nm-thick Al_2O_3 layer is grown by atomic layer deposition (ALD) and serves as both a passivation layer and to minimize gate leakage. Via openings are made to the source and drain contacts with a 1-min BOE etch. The ALD oxide is also removed in a 5-μm-long region for the Schottky gate of the D-mode HEMT. The oxide remains unetched for the gate of the ALD-MIS-HEMT. Removal of the ALD Al_2O_3 in the gate region of the OX-MIS-HEMT cannot be done selectively since the thermal oxide also etches when exposed to typical ALD Al_2O_3 etchants. Finally, Ni/Au metal pads are deposited to form 15-μm-long gate contacts and probing pads for the source and drain. A T-shaped gate is formed for the OX-MIS-HEMT, with the center 5 μm of the gate being oxidized and 5 μm on either side of the thermal oxide having ALD Al_2O_3 with AlInN underneath.

Fig. 1 shows a cross-section of the thermally oxidized OX-MIS-HEMT with a fabrication process flow chart. Additionally, gate regions of the normally ON or D-mode-HEMTs (Schottky gate) and ALD-MIS-HEMTs (ALD Al_2O_3 between the gate metal and AlInN) are depicted for comparison (inset of Fig. 1). Table I details the transistor specs for the different devices, such as the source, gate, drain spacing, and channel widths and lengths. After fabrication, the devices are wafer probed and tested on a semiconductor parameter analyzer at room temperature to determine the output and transfer characteristics of the transistors. The oxide is imaged, and the composition is determined using scanning electron microscopy, scanning transmission electron microscopy (STEM), and energy-dispersive X-ray spectroscopy (EDS).

III. Results and Discussion

Fig. 2 shows STEM and EDS images in two locations of the oxidized gate region of the OX-MIS-HEMT. Fig. 2(a) and (b)

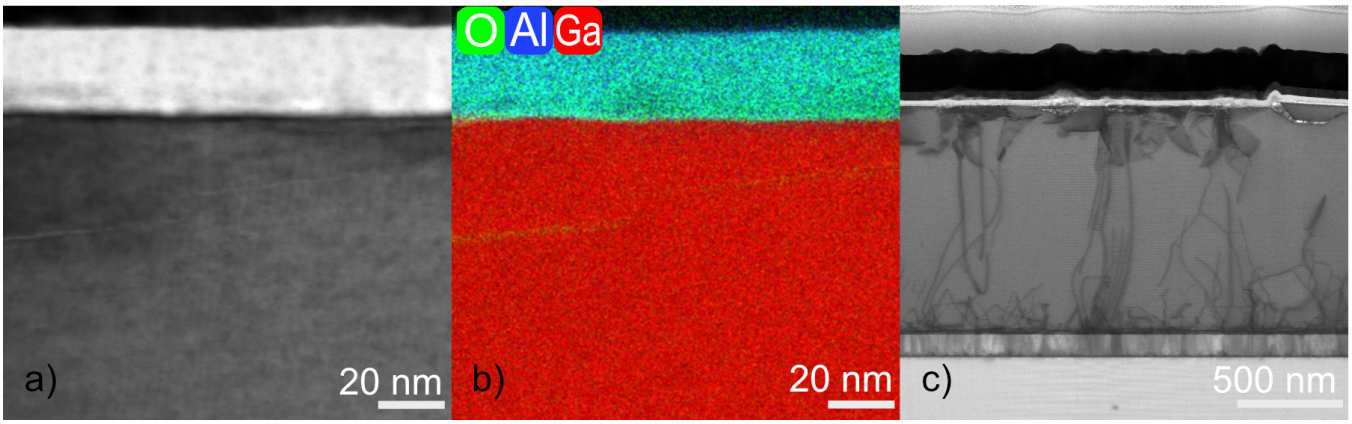

Fig. 2. STEM images and EDS maps of different oxidized regions within and at the edge of the gate for the OX-MIS-HEMT. (a) STEM image of a smooth region with (b) respective EDS map. (c) Zoomed-out STEM image demonstrating oxidation roughness near threading dislocations and a crack at the oxidation edge on the right.

TABLE I
FABRICATED DIMENSIONS OF DIFFERENT HEMTS USED FOR COMPARISON IN THIS STUDY

FET Type	Channel Width (μm)	L_G (μm)	L_{GS} (μm)	L_{GD} (μm)	Opening Length (μm)
D-mode HEMT	200	15	5	10	5
ALD-MIS-HEMT	200	15	5	20	0
OX-MIS-HEMT	200	15	5	10	5

shows a defect-free region where complete oxidation of the AlInN and AlN layer occurs in the oxidized gate region. The interface between the GaN and oxide is smooth, and the thermal Al_2O_3 is indistinguishable from the deposited ALD Al_2O_3. Indium and nitrogen are not detected in the EDS mapping, indicating that it is being removed during oxidation and cleaning. In accumulates on the oxide surface during oxidation [38], and removing SiN_x and surface cleaning for the source and drain contacts lead to complete Indium removal. Fig. 2(c) shows a zoomed-out image with rougher oxide regions formed near threading dislocations and cracking at the edge of the oxide (right-hand side). Overoxidation could be contributing to the roughness and cracking. The role of threading dislocations is unknown, but the collected data suggests that they could promote oxidation of the AlInN layer at different rates, leading to roughness. Previous experiments on the oxidation of buried AlInN layers revealed that little to no lateral oxidation occurs. At most, lateral oxidation occurs at the same rate as vertical oxidation, which would produce 10–20 nm of oxide and is unlikely to be a significant factor in device performance. Additionally, the SiN_x hard mask introduces stress at the edges of the selective oxidation opening. This stress contributes to edge cracking and most likely impacts device performance for the OX-MIS-HEMT by reducing the ON-state current.

Current versus voltage (IV) measurements are performed on the different HEMTs to compare their performance. For each set of IV measurements, an initial measurement is taken (black), followed by five consecutive measurements to stress the devices (blue), and a final measurement 10 min after the last stressed measurement (orange). The voltage ranges were chosen to highlight the turn-on and the ON-state current. Fig. 3(a) and (b) shows the transfer characteristics, or logarithm of the drain current (I_d) versus gate–source voltage (V_{gs}), at a drain bias of 10 V of the standard D-mode-HEMT and ALD-MIS-HEMT, respectively. As expected, the D-mode-HEMT is normally ON and shows a high leakage current, which is typical for HEMTs with Schottky gates [39]. The ALD Al_2O_3 reduces the leakage current by five orders of magnitude and shifts the threshold voltage to even lower voltages for the ALD-MIS-HEMT. The transfer characteristic only slightly changes between the stress and recovery measurements for these devices.

Fig. 3(c) shows the transfer characteristic of the OX-MIS-HEMT, at a drain bias of 10 V, exhibiting many benefits. The IVs are swept from negative to positive voltages. First, these devices have low leakage in the OFF-state, similar to the ALD-MIS-HEMT. The low currents are observed up to −1 V for the stressed device, indicating that the thermally oxidized gate creates an enhancement mode HEMT. They show ON/OFF ratios of $\sim 10^7$, which is greater than the standard HEMT, $\sim 10^5$, and less than the ALD-MIS-HEMT $\sim 10^9$. They exhibit low currents ($\sim 2 \times 10^{-7}$ mA/mm) at zero gate voltage and are in the OFF state.

Of course, some challenges must be overcome, which are typical for new oxide semiconductor devices and discussed below. After stressing, the threshold voltage shifts to positive voltages, indicating interface traps and charges at the oxide–semiconductor interface under the gate. The shift in threshold voltage remains after waiting 10 min, suggesting a burn-in effect. The devices' subthreshold swing is large, with turn-on occurring over many volts, and they are more resistive, resulting in low ON-state currents. When compared to the D-mode HEMT and ALD-MIS-HEMT, the OX-MIS-HEMT has an ON-state current that is lower by over three

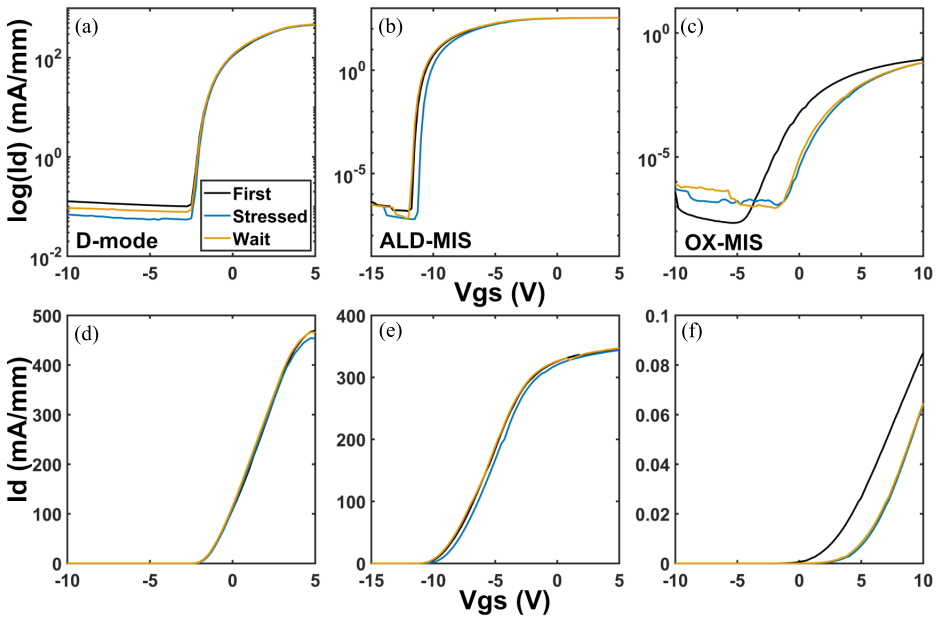

Fig. 3. Transfer characteristics for different fabricated devices after an (black) initial sweep, (blue) stressed after consecutive measurements, and (orange) waiting 10 min after stressing before remeasuring. (a)–(c) Semilog transfer characteristics, drain current versus gate–source voltage (I_d versus V_{gs},) at a drain voltage (V_d) = 10 V for the D-mode HEMT, ALD-MIS-HEMT, and OX-MIS-HEMT, respectively. (d)–(f) Same transfer characteristic, I_d versus V_{gs}, in a linear scale.

orders of magnitude at 10 V. From the STEM images in Fig. 2, cracking at the edges attributed to stress from SiN_x mask is likely the cause of this current lowering. Degradation of the 2DEG in unoxidized regions is not expected since all devices are subjected to the same thermal budget (they are processed on the same sample), while only the OX-MIS-HEMT has a lower ON-state current. Another possibility is that oxidation at the GaN interface reduces the mobility of the channel under the gate region, resulting in higher resistances and, therefore, lower ON-state current. An estimated channel mobility of up to $\sim$1 cm^2/Vs is obtained by using the saturation current from output characteristic measurements, like the analysis done with MOSFETs. In a crack-free device, we expect higher mobilities to be observed since cracking along the channel width reduces the "effective" device size. Additionally, the low mobility may be a result of overoxidation, where increased roughness is expected by oxidizing the GaN. Fig. 3(d)–(f) shows the transfer characteristics on a linear scale for each HEMT, which clearly shows the enhancement mode behavior of the OX-MIS-HEMT compared to the other two devices. The OX-MIS-HEMT has a threshold voltage of $\sim$4 V after being stressed. The threshold voltages are obtained by taking the slope of the linear V_{gs} curve after turn-on and tracking where a corresponding line crosses the x-axis.

Hysteresis measurements for the different HEMTs are conducted to understand charges and trapping at the oxide semiconductor interfaces. Dual-sweep transfer characteristics measured from negative to positive voltages and back are conducted with a drain voltage of 10 V. The D-mode devices show minimal hysteresis. Both the ALD-MIS-HEMT and OX-MIS-HEMT show hysteretic behavior due to charges. Comparing the two transfer curves after stressing shows that the ALD-MIS-HEMT has more hysteresis than the OX-MIS-HEMT

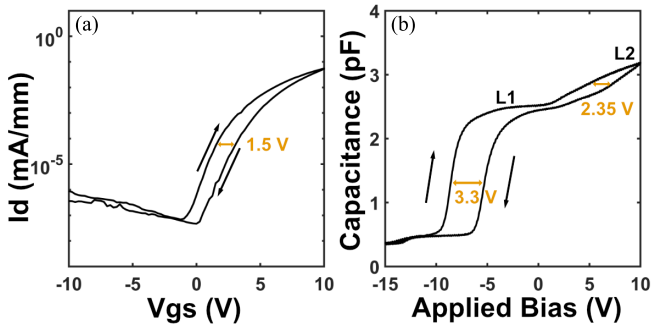

Fig. 4. (a) Dual-sweep transfer characteristic, I_d versus V_{gs}, at $V_d = 10$ V that is swept from -10 to 10 V and back with a $+1.5$ V change in voltage. (b) Capacitance versus voltage measurement from depletion to accumulation showing two capacitance "ledges" (L1 and L2) associated with the gate topology. L1 is a capacitance from the ALD Al_2O_3 while L2 is from the thermal oxide.

and a change in voltage of $+2.5$ and $+1.5$ V is observed, respectively. Fig. 4(a) shows the dual-sweep transfer curve of the OX-MIS-HEMT with the labeled change in voltage. In addition to the transfer curves, capacitance versus voltage (CV) measurements between the source and gate of the OX-MIS-HEMT are performed. Fig. 4(b) shows the CV sweep from depletion to accumulation and back to depletion of the OX-MIS-HEMT. The CV sweeps are taken at 1 MHz with an amplitude of 30 mV. Since the gate design is T-shaped, two capacitance "ledges," L1 and L2, are observed. The first, L1, is attributed to the ALD Al_2O_3/AlInN interface in the regions bordering the left and the right of the oxide gate that are not thermally oxidized. The second, L2, is from the thermally oxidized AlInN/GaN interface. Like the transfer characteristic, more hysteresis is observed for the ALD Al_2O_3/AlInN

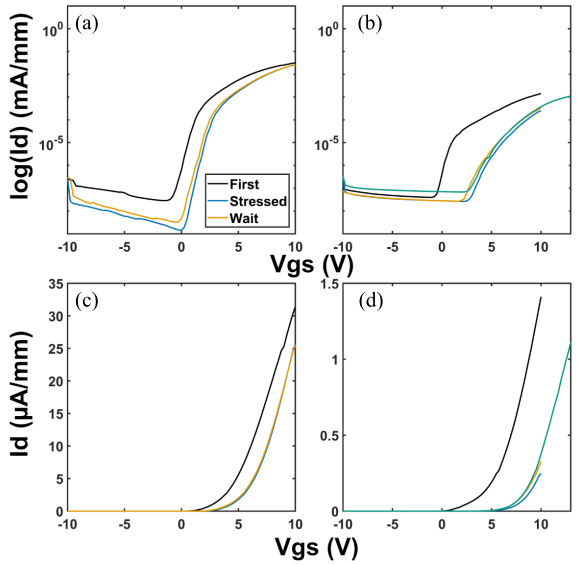

Fig. 5. Transfer characteristics, I_d versus V_{gs}, for the annealed OX-MIS-HEMT at $V_d = 10$ V after an (black) initial sweep, (blue) stressed after consecutive measurements, and (orange) waiting 10 min after stressing before remeasuring. Plots (a) and (b) of semi-log transfer characteristics after annealing the sample at 400 °C and 500 °C for 10 min respectively. Plots (c) and (d) of transfer characteristics on a linear scale. Additionally, the sample annealed at 500 °C is measured past $V_{gs} = 10$ V to reach the maximum ON-state current, (teal) which is shifted after annealing.

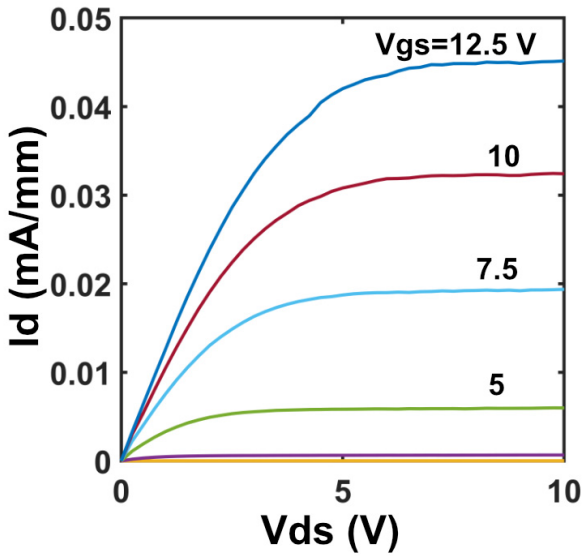

Fig. 6. Output characteristic consisting of drain current versus drain–source voltage (I_d versus V_{ds}) sweeping the gate–source voltage (V_{gs}) from −2.5 to 12.5 V in steps of 2.5 V for an unannealed OX-MIS-HEMT. The output curves with appreciable current are labeled with their respective V_{gs}.

interface with a change in voltage (width) of +3.3 V when compared to the thermal oxide/GaN interface that has a shift of +2.35 V. Hysteresis from the *CV* measurements indicates that there is oxide charge for both oxides with the ALD oxide having more charge. Other reports on *CV* measurements for ALD Al_2O_3 recessed MIS-HEMTs show a voltage shift of ∼0.5 V [20]. Improving interface charges of the thermal oxide is a priority. Considering the thermal oxide has less charge than the ALD Al_2O_3, significant improvement like what has been achieved for the ALD oxide is realistic by fine-tuning the oxidation processing steps.

After processing the OX-MIS-HEMTs, an annealing study is conducted to see the effects of postmetallization annealing (PMA) on the oxide interface. Other studies on ALD-deposited oxides show improvement in interface characteristics after PMA [40]. Fig. 5(a) and (b) shows the transfer characteristic after annealing the OX-MIS-HEMT at 400 °C and 500 °C for 10 min in 1000 sccm of N_2, respectively, using the same stressed measurements described above. With increasing annealing temperature, the threshold voltage shifts to even higher voltages, preserving enhancement mode behavior, and the subthreshold swing improves by two times when compared to the unannealed samples. The improvement in electrical performance indicates that annealing the samples improves the oxide–semiconductor interface. A drawback to annealing the samples is a further reduction in the ON-state current for the devices by ∼2 times for the devices annealed at 400 °C and ∼10 times at 500 °C. Additionally, due to the shift in threshold voltage, the device annealed at 500 °C is also swept to higher gate voltages to observe the plateau in ON-state current, which is observed before stressing the devices.

Fig. 5(c) and (d) shows the linear transfer characteristic for the annealed devices, which show the positive shift in threshold voltage after annealing. Threshold voltages greater than 5 and 8 V are observed for the devices annealed at 400 °C and 500 °C, respectively. The additional shift in threshold voltage is attributed to either the passivation of interface charges or oxide charges from the postanneal step. High threshold voltages are ideal to prevent false gate triggering in high-power applications.

Fig. 6 shows the output characteristic, I_d versus drain–source voltage (V_{ds}), for an unannealed OX-MIS-HEMT with V_{gs} from −2.5 to 12.5 V with voltage steps of 2.5 V. Appreciable currents do not occur until 5-V bias is applied, demonstrating enhancement mode operation. Compared to previous studies with thermally oxidized gates, these devices can be driven at higher gate voltages of up to 15 V before catastrophic breakdown. With a threshold voltage that increases after annealing and the ability to be driven at higher gate voltages, using an oxidized barrier layer has promising features for power devices.

There are certainly improvements that can be made in the device processing that will result in better performance. The nonideal subthreshold swings, low ON-state current, and shifts in threshold voltages are most likely a result of stresses in the SiN_x masking layer and the thermal oxide layer itself. Stress from the ∼100-nm SiN_x layer accounts for cracking observed at the edges of the oxide gate in the STEM images, as delamination and blistering are observed in the microscopic images of SiN_x outside the gate region of the sample after the oxidation step. Maier et al. [34] describe using a 30-nm robust crack and blister-free Si_3N_4 layer as a passivation for the AlInN/GaN HEMTs that are measured at temperatures up to 1000 °C. Replicating this low-stress and temperature-robust

SiN layer as a selective oxidation mask should improve device performance by reducing cracking along the opening for the gate oxide. Additionally, oxidation times were not optimized in this study, and ideally, the oxidation would terminate on the AlN or GaN interface. The oxidation time and temperature are decided based on previous oxidation rate studies of AlInN. This study shows that the oxidation rate decreases with decreasing In content [38]. Therefore, AlN could act as an oxidation termination layer since appreciable oxidation of AlN is typically observed between 800 °C and 1100 °C [41], [42]. Further studies must be conducted to determine if the AlN layer is a viable oxidation termination layer at 850 °C. This requires measuring the oxidation rates of AlN and exploring oxidization conditions to ensure uniform oxidation across the wafer. Finally, to improve the subthreshold swing and low ON-state currents of the OX-MIS-HEMT, smaller gate lengths and short oxidation times could be explored too. This should help reduce the number of interface traps under the gate.

IV. Conclusion

To conclude, complete oxidation of the AlInN under the gate of a standard AlInN/GaN HEMT structure results in enhancement mode operation with 4 V threshold voltages and low OFF-state currents ($\sim 2 \times 10^{-7}$ mA/mm) at zero gate voltage. Additionally, the PMA of the devices results in a positive shift in the threshold voltage beyond zero volts, ensuring enhancement mode behavior. Improving the oxidation process, such as managing stress and optimizing the oxidation conditions, should significantly improve the device's performance. The initial devices show promising results for an alternative way to form an enhancement-mode MIS-HEMT that potentially can compete with state-of-the-art performance and is a promising candidate for power applications.

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