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Investigating Wet Chemical Oxidation Methods to Form SiO_2 Interlayers for Self-Aligned Pt-HfO_2-Si Gate Stacks

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Abstract:

Self-aligned metal-oxide-semiconductor (MOS) capacitors are studied with several low temperature, wet chemical silicon dioxide (SiO_2) interlayers to understand their impact on electrical performance. Self-aligned MOS capacitors are fabricated with a bottom-up patterning technique that uses a poly(methyl methacrylate) brush and dopant-selective KOH etch combined with area-selective atomic layer deposition (AS-ALD) of hafnium dioxide (HfO_2) and Pt. The wet chemical pre-treatments used to form the SiO_2 interlayer include HF-last, 80 °C H_2O, and SC-2. Capacitance-voltage measurements of these area-selective capacitors exhibit a HfO_2 dielectric constant of ~19, irrespective of pre-treatment. After a forming gas anneal, the average interface state density decreased between 1.8 and 7.5 times. The minimum observed D_{it} is 1 x 10^{11} $eV^{-1}cm^{-2}$ for the HF-last treatment. X-ray photoelectron spectroscopy shows an increase in stoichiometric SiO_2 in the interfacial layer after the anneal. Additional carbon is also observed; however, comparison with capacitors fabricated in a non-selective process reveals minimal impact on performance.

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I. INTRODUCTION

Alignment between the edge of a gate stack and the edge of the underlying doped source-drain regions of the silicon (Si) channel is a critical issue for the fabrication of high-performance transistors. Excess overlap results in large fringe capacitance and reduced device speed while too much underlap can result in extra series resistance.[1,2] Achieving proper alignment within an integrated high-k/metal gate stack can require complex integration schemes such as the replacement metal gate technique.[3] Processing and integration becomes even more challenging for gate-all-around transistors with either vertical[4] or lateral[5] silicon nanowires, where numerous process steps are required to align the gate stack over the channel (e.g., selectively etching a gap across the channel and depositing a dummy gate for source/drain doping, then replacing the dummy gate with a high-k gate stack). The ability to form self-aligned device structures, such as MOS capacitors, would simplify fabrication of gate-all-around transistors and benefit a variety of emerging device applications, including vertical nanowire transistors monolithically integrated into the back end of line (BEOL)[6] and flexible electronics that require lower process temperatures and patterning techniques that are more scalable than conventional photolithography.[7]

Atomic layer deposition (ALD) allows for low-temperature and area-selective deposition of thin films closely aligned with patterns on the underlying substrate, largely irrespective of geometry. The most common techniques for area-selective ALD (AS-ALD) involve using self-assembled monolayers (SAMs)[8-15] or other polymeric materials[16-21] to deactivate the surface by preventing the chemisorption of the ALD precursors. These techniques typically require photolithography to apply the masking

material, either to pattern the surface modification layer[13,16-18] or to pattern the deposition of different materials that have intrinsic chemical differences.[10,12,21,22]

Our previous work demonstrated a fabrication process that combines a bottom-up patterning technique with AS-ALD to deposit hafnium dioxide (HfO_2) and platinum (Pt) thin films based on the local carrier concentration of the underlying Si substrate, ultimately forming self-aligned MOS capacitors.[23] The bottom-up patterning techniques is a derivative of selective co-axial lithography via etching of surfaces (SCALES).[24,25] Patterning with SCALES begins with a poly(methyl methacrylate) (PMMA) brush grown from a Si surface via atom-transfer radical polymerization. We selectively remove the polymer film from the lightly doped Si regions by etching with an aqueous potassium hydroxide (KOH) solution. The PMMA film remains attached to the heavily doped Si regions which then serves as a mask for AS-ALD of HfO_2 and Pt. The resulting self-aligned MOS capacitors yielded expected capacitance-voltage behavior.

A thin SiO_2 layer is often required to form a low defect density interlayer between Si and high-k dielectrics,[26,27] as well as to improve ALD nucleation of HfO_2.[28] To form this interlayer, a high-temperature thermal oxidation technique is typically used. However, high temperature thermal oxidation is not possible with the current SCALES process because the polymer cannot withstand high process temperatures. Other chemical oxidation methods have also been studied to improve ALD film nucleation and reduce interface state density, including treatments such as hydrogen peroxide, standard cleans 1 and 2 (SC-1 and SC-2 from RCA clean), nitric acid and heated water (H_2O).[28,29]

In this work, self-aligned (area-selective deposition) Pt-HfO_2-Si MOS capacitors are compared with conventional (non-selective deposition) capacitors to investigate the

impact of a variety wet chemical processes (i.e., HF etch, 80 °C H_2O, and SC-2) for forming the SiO_2 interlayer. Physical characterization methods (i.e., ellipsometric spectroscopy and x-ray photoelectron spectroscopy) are used to understand the relationship between the various SiO_2 interlayer formation techniques and the electrical performance of the capacitors. Capacitance-voltage characteristics exhibit similar performance between area-selective and non-selective capacitors, and average interface state density is reduced to 1.9 x 10^{11} $eV^{-1}cm^{-2}$ after a forming gas anneal (FGA). X-ray photoelectron spectroscopy indicates an increase in the amount of stoichiometric SiO_2 in the interfacial layer after the FGA. Additional carbon is also observed in the area-selective interfacial layer after the FGA which does not significantly impact performance.

II. EXPERIMENTAL METHODS

A. Non-selective capacitor fabrication

For conventional "non-selective" capacitors, Si(100) with a p-type doping level of ~10^{18} cm^{-3} was used. A modified RCA clean was first performed: 1 min in dilute SC-1 (5 DI H_2O:1 H_2O_2:0.25 NH_4OH) at 75 °C, 30 s HF etch, and 10 min in SC-2 (5 DI H_2O:1 H_2O_2:1 HCl) at 75 °C. The fabrication process for the area-selective capacitors requires a less aggressive organic clean than the typical SC-1 treatment to minimize damage to the PMMA mask. For consistency, a modified version of the typical RCA clean was used for both the non-selective and area-selective capacitors. This clean was followed by an HF etch (30 s in 1% HF) to remove the native oxide prior to formation of the SiO_2 interlayer. Three different wet chemical oxidation techniques were investigated as pre-treatments to form the thin SiO_2 interlayer: HF-last treatment (30 s in 1% HF followed by DI H_2O rinse), hot water (30 s in 1% HF then 10 min in ultra-pure DI H_2O at 80 °C), and SC-2

treatment (30 s in 1% HF then 10 min in 5 DI H_2O:1 H_2O_2:1 HCl at 75 °C). These chemical oxides are compared with a high temperature rapid thermal processing (RTP) oxidation (30 s in 1% HF, 3 min in RTP furnace flowing 5 SCCM O_2 at 900 °C, 1% HF etch to reduce thickness).

Immediately following oxidation, the samples were transferred to the ALD chamber (Cambridge Fiji ALD system with argon as a carrier/purging gas and a total chamber pressure of 0.45 Torr) to deposit ~6 nm of thermal HfO_2 at 200 °C using 55 cycles of tetrakis(dimethylamido)hafnium (TDMAHf) and H_2O. The exposure times for TDMAHf and H_2O were 0.25 and 0.06 s, respectively, followed by purge times of 20 and 15 s. Electron-beam evaporation was used to deposit 75 nm of Pt through a shadow mask, forming approximately 85 µm x 85 µm square MOS capacitors. Figure 1a shows the device structure. The final process step was a forming gas anneal (FGA, 5 SCCM, 96% N_2 / 4% H_2) for 30 min at 400 °C, and results are shown for annealed and unannealed capacitors.

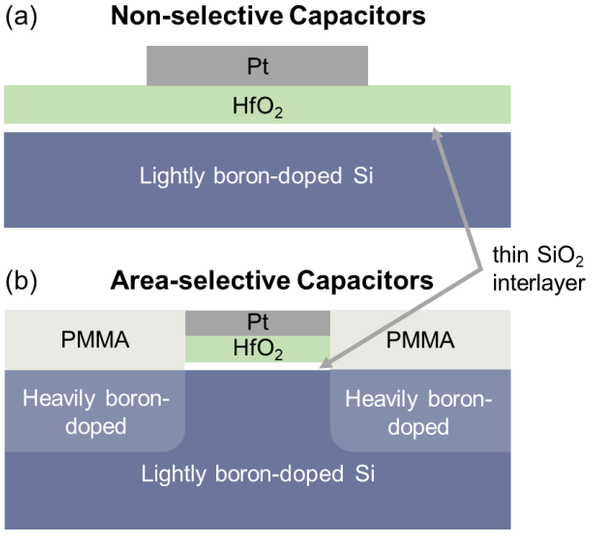

Fig. 1. Schematic diagrams representing the cross-sectional device structure for non-selective capacitors (a) and area-selective capacitors (b).

B. Area-selective capacitor fabrication

To fabricate the self-aligned "area-selective" capacitors, p-type Si(100) was patterned with a thick SiO_2 mask and then doped with boron via solid state diffusion (2 h at 1050 °C, B_2O_3 source) to fabricate heavily boron-doped (~10^{20} cm^{-3}) substrates with lightly boron-doped (~10^{18} cm^{-3}) approximately 100 μm x 100 μm square regions and one additional 4 mm x 12 mm area adjacent to the capacitors for physical characterization. Given the junction depth of about 1 μm, we expect boron to diffuse laterally a similar amount. The final device dimensions are 96 μm x 96 μm. This doping profile enables the use of SCALES and AS-ALD to form the self-aligned structures. With the SCALES process, a poly(methyl methacrylate) (PMMA) brush anchored to the Si surface was synthesized[24] across the entire substrate and selectively removed from the lightly-doped regions via cycles of exposure to potassium hydroxide (KOH) solution (1 mL 45 wt% KOH:3 mL IPA:8.5 mL DI H_2O) to etch the Si and acetone to solvate the PMMA. The substrate was then cleaned with the same modified RCA clean described previously, followed by 1% HF etch and thin SiO_2 oxidation using the same oxidation treatments described in the non-selective capacitor methods. However, the thermal oxidation requires very high temperature which degrades the PMMA film used for patterning, so only the chemical oxide pre-treatments were used to fabricate the area-selective capacitors. After oxidation, samples were transferred to the ALD chamber for selective deposition of HfO_2 and Pt on the exposed lightly doped Si. HfO_2 was deposited with 55 cycles of thermal HfO_2 ALD at 200 °C using the same recipe as the non-selective

capacitors. Following the HfO_2 deposition, Pt was deposited with 300 cycles of thermal Pt ALD at 300 °C using (trimethyl)methylcyclopentadienylplatinum(IV) ($MeCpPtMe_3$) and O_2. The exposure times for $MeCpPtMe_3$ and O_2 were 1 and 10 s, respectively, followed by purge times of 10 s. This fabrication process is described in detail in previous work.[23,24] Figure 1b shows the resulting device structure. The final process step was a FGA (5 SCCM, 96% N_2 / 4% H_2) for 30 min at 400 °C, and results are shown for annealed and unannealed capacitors.

C. Electrical Characterization

Capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were conducted with a Keithley 4200-SCS semiconductor analyzer and Cascade Microtech probe station. Capacitance and conductance were measured at 100 kHz with a voltage sweep from 2 V to -2 V. Capacitance and conductance data was normalized to device area. The conductance method was used to extract interface state density (D_{it}), assuming a small standard deviation in the semiconductor surface potential, using the equation:[30]

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \quad (1)$$

where q is electronic charge, ω is angular frequency, and G_p is the conductance peak after extracting and correcting for series resistance using the relationships defined by Vogel et. al.[31] The measured capacitance (C_m) and conductance (G_m) were corrected using the following relationships:

$$C_c = \frac{C_m}{(1-G_m R_s)^2+\omega^2 {C_m}^2 {R_s}^2} \quad (2)$$

$$G_c = \frac{\omega^2 C_m C_c R_s - G_m}{G_m R_s - 1} \quad (3)$$

where C_c is corrected capacitance, G_c is corrected conductance and R_s is series resistance. Series resistance was extracted by numerically iterating the R_s value in the corrected conductance equation until G_c is minimized throughout accumulation (or approximately equal to tunneling conductance). After G_c is obtained for 5 capacitors from each interlayer type, the average D_{it} value is plotted with error bars indicating the standard deviations.

D. Physical Characterization

Spectroscopic ellipsometry was used to measure film thickness. Spectroscopic ellipsometry was performed with a Woollam M-2000 ellipsometer, and CompleteEase software (J.A. Woollam) was used for all spectra fitting for the SiO_2 and HfO_2 films. X-ray photoelectron spectroscopy (XPS) was used to physically characterize the composition of the SiO_2/HfO_2 thin films. XPS measurements were performed with a Thermo Scientific K-Alpha X-ray photoelectron spectrometer system with a monochromatic Al Kα source using a spot size of 400 μm and pass energy of 50 eV. The Si(2p) peak at 99.4 eV corresponding to elemental Si bonds from the substrate was used as a reference peak, and the spectra were shifted to correct the effects of experimental charging. XPS spectra from the capacitors did not detect the SiO_2 interlayer underneath the HfO_2 layer and Pt electrode due to the limited penetration depth of XPS (~5-10 nm).[32] To overcome this, separate samples with a thinner HfO_2 film and without the Pt film were fabricated for XPS measurements. The substrates were prepared in the same way as the capacitor samples with only 30 cycles of HfO_2 ALD and no Pt deposition, and XPS spectra were obtained immediately after processing. Additionally, the spot size for both the ellipsometric and XPS measurements is larger than the area-selective capacitor device

size, so the measurements were performed on the larger patterned area adjacent to the capacitor devices. We assume the film thickness to be relatively uniform across the growth regions of the patterned substrate.

III. RESULTS AND DISCUSSION

Figure 2 shows representative curves of C-V behavior for non-selective and area-selective capacitors before and after the FGA. The C-V curves exhibit expected behavior for MOS capacitors. A difference in maximum capacitance measured for each pre-treatment is noted in addition to presence of interface states. Small variations in SiO_2 thickness for different oxidation methods are likely responsible for the differences in the measured maximum capacitances. Ellipsometry measurements during fabrication indicate that the HfO_2 film thickness for all of the non-selective capacitors was 6.2 nm with the following SiO_2 interlayer thicknesses from each pre-treatment: 0.7 nm from HF, 1.1 nm from 80 °C H_2O, 1 nm from SC-2, and 1.4 nm from thermal oxidation. Similarly for all of the area-selective capacitors, the HfO_2 film was 6.1 nm thick with slightly thicker SiO_2 interlayer thicknesses: 1.0 nm from HF, 1.5 nm from 80 °C H_2O, and 1.5 nm from SC-2. Ellipsometry measurements show a slightly thicker SiO_2 layer for the area-selective capacitors, corresponding to a 0.3-0.5 nm difference in thickness. The differences in thickness between the selective and non-selective cases may be due to a difference in surface roughness from the KOH etching, which can result in overestimation of film thickness for ellipsometry.[33] And the extra process steps for the area-selective capacitors can cause changes in surface properties that impact oxidation.

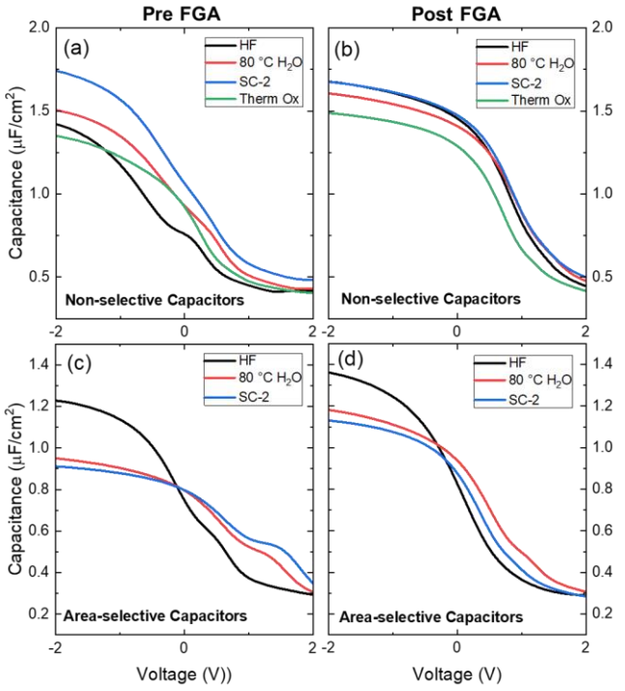

Fig. 2. Capacitance-voltage characteristics of non-selective (a and b) and area-selective (c and d) Pt-HfO_2-Si MOS capacitors before (a and c) and after (b and d) a FGA. Each graph shows a representative C-V curve of one capacitor with each SiO_2 interlayer treatment: HF, 80 °C H_2O, SC-2, and thermal oxide (non-selective only).

Both sample sets show improved performance after the FGA as indicated by the reduced stretch out of the curves. The slight differences in maximum capacitance after the FGA can likely be attributed to a combination of factors including formation of Hf silicate at the interface,[34] increased dielectric constant due to polycrystallization,[35] and diffusion of carbon residue to the surface (*vide infra*). Combining the measured SiO_2 and HfO_2 thicknesses with maximum capacitances between 1.3 and 1.7 μF/cm^2 yields an estimate of a relative dielectric constant of ~20 for the non-selective HfO_2 films, which is expected for ALD HfO_2.[36] Similarly for the area-selective HfO_2 films with maximum

capacitances measured between 0.9 and 1.2 μF/cm^2, a relative dielectric constant of ~19 is estimated, which is very similar to that of the non-selective capacitors.

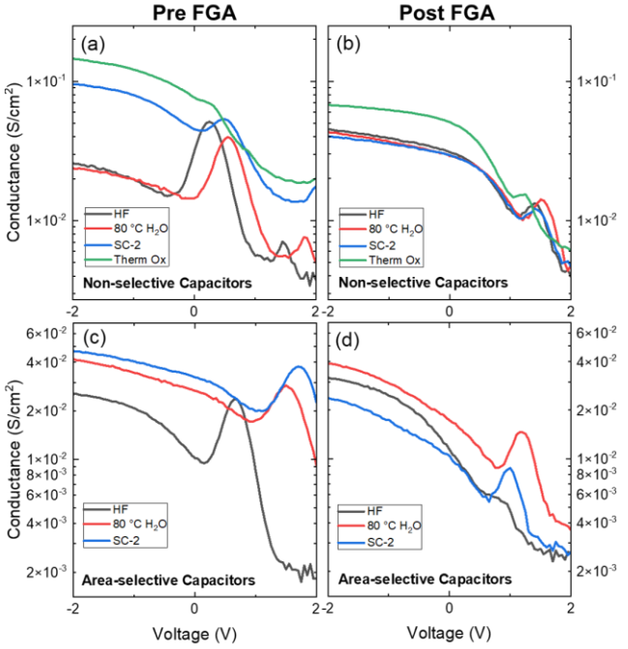

Fig. 3. Conductance-voltage behavior of non-selective (a and b) and area-selective (c and d) Pt-HfO_2-Si MOS capacitors before (a and c) and after (b and d) a FGA. Each graph shows a representative G-V curve of one capacitor with each SiO_2 interlayer treatment: HF, 80 °C H_2O, SC-2, and thermal oxide (non-selective only).

The humps observed in the pre-FGA capacitance curves indicate significant interface state density (D_{it}), so conductance measurements are used to better investigate D_{it}. Figure 3 shows the voltage dependance of measured conductance (G_m) for a device with each oxidation technique for both the non-selective and area-selective capacitors. The peaks seen in the G_m curves are attributed to interface states. D_{it} is extracted for 5 capacitors for each interlayer type before and after FGA as shown in Fig. 4. The interface

state density is observed to decrease significantly with the FGA. The average D_{it} decreases from 8.5 x 10^{11} $eV^{-1}cm^{-2}$ to 1.9 x 10^{11} $eV^{-1}cm^{-2}$ for the non-selective capacitors and from 5.7 x 10^{11} $eV^{-1}cm^{-2}$ to 1.9 x 10^{11} $eV^{-1}cm^{-2}$ for the area-selective capacitors. These post FGA values are similar to what is typically observed for HfO_2/Si gate stacks (~10^{11} $eV^{-1}cm^{-2}$).[37,38] The D_{it} for the wet chemical SiO_2 interlayers is similar to that of the thermal oxide, and there is no significant difference between the non-selective and area-selective samples. The results show that the area-selective process does not have a negative impact on electrical performance relative to the non-selective process, and using any of the wet chemical interlayer techniques results in formation of an interface that functions similarly to the thermal oxide interlayer. However, the standard deviations of the D_{it} are larger for the area-selective processes as compared to the non-selective process. The extra processing steps for the area-selective capacitors (i.e., polymer synthesis and KOH etch) likely roughen the surface and leave carbon residue unevenly distributed across the Si surface. This can result in more extrinsic defects and impurities in some regions of the substrate, leading to more variability in electrical performance.

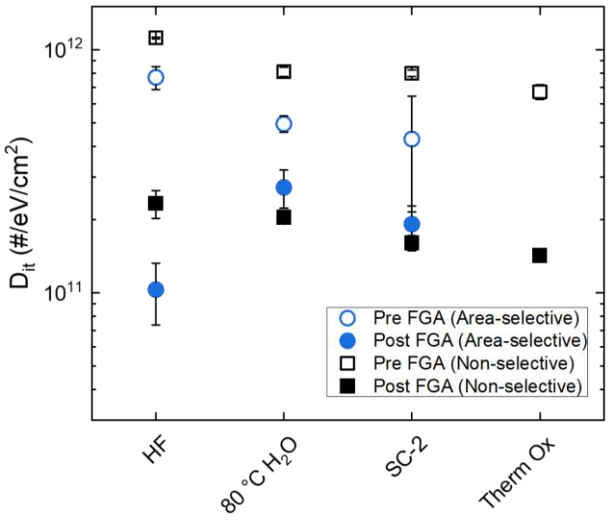

Fig. 4. Estimated D_{it} values for non-selective (black) and area-selective (blue) Pt-HfO_2-Si MOS capacitors before and after the FGA.

XPS is used to physically characterize the oxide-semiconductor interface of the capacitor structure to understand the impact of the processing on the composition of the interlayer. Figure 5 shows XPS spectra of the Si(2p) region obtained from $HfO_2/SiO_2/Si$ substrates that were treated with the same initial processing steps as the capacitors (i.e., modified RCA clean, interlayer oxidation, HfO_2 ALD, and FGA for the non-selective set; PMMA, KOH etch, modified RCA clean, interlayer oxidation, HfO_2 ALD, and FGA for the area-selective set). All substrates show the expected elemental Si doublet peak near 99.4 eV (seen in Fig. 5c for substrates after FGA) due to the bulk Si substrate. The oxidized Si(2p) peak for stoichiometric SiO_2 would be expected near 103.5 eV (referenced to elemental Si at 99.4 eV).[39] Peaks representing lower oxidation states of Si (Si^{1+}, Si^{2+}, Si^{3+}) and Hf silicate compounds have binding energies between 99.4 eV and 103.5 eV.[40-42] With the exception of the pre-anneal HF-treated substrates, all samples have a small peak near 103.5 eV (seen in Fig. 5). These peaks are broader and slightly closer to the elemental Si peak than a stoichiometric SiO_2 peak would be, indicating they are likely a convoluted peak consisting of multiple overlapping peaks attributed to SiO_2, Si suboxides in multiple oxidation states (SiO_x), and Hf silicate compounds.

With the HF pre-treatment, no clear Si(2p) suboxide photoelectron peak is observed before the FGA (but a subtle left-side shoulder of the elemental Si(2p) peak allowed for fitting of a very small suboxide peak for comparison). This suggests very minimal formation of an interlayer during ALD. After the FGA, the appearance of an Si(2p) suboxide peak at 103.0 eV and 102.8 eV for the non-selective deposition substrate

and the area-selective deposition substrate, respectively, indicates formation of an interfacial layer between the Si and HfO_2 film, which is typically seen with annealing of HfO_2 films.[43,44] Excess oxygen in the HfO_2 film in the form of hydroxyl groups can react with Si at the interface to form an interlayer upon thermal treatment.[43] Oxygen impurity in the forming gas is also a possibility, which could allow for diffusion of oxygen through the HfO_2 layer to facilitate SiO_2 growth at the interface.[45]

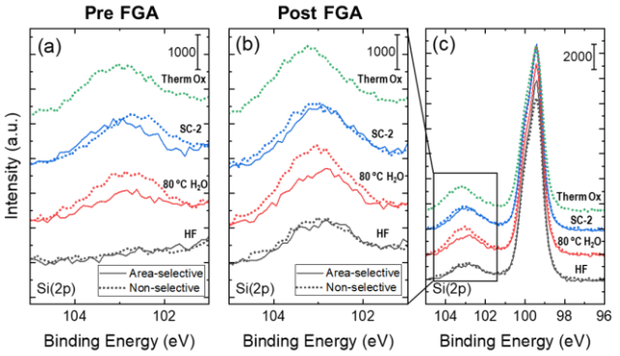

Fig. 5. Si(2p) XPS spectra of non-selective (dotted line) and area-selective (solid line) HfO_2 films on Si with different SiO_2 interfacial layers before (a) and after (b) the FGA; (a) and (b) show a narrower region to see the oxidized Si(2p) peaks in more detail; (c) shows the full Si(2p) spectrum of all substrates after the FGA.

After the FGA, an increase in the peak area of the Si(2p) suboxide photoelectron peak is observed for all interlayer types and most of the peaks blueshift. Figure 6a shows the peak positions of the Si(2p) suboxide peak for each interlayer type before and after annealing. Figure 6b shows the ratio of integrated intensity of the suboxide Si(2p) peak normalized to the integrated intensity of the elemental Si(2p) peak before and after the FGA for each interlayer type. In general, we see the Si(2p) suboxide peak shift to a binding energy 0.2-0.3 eV higher after the FGA. The integrated intensity ratio of the Si

suboxide peak shows a 30-80% increase for the 80 °C H_2O treated substrates, 10-20% increase for the SC-2 treated substrates, and 40% increase for the thermal oxide treated substrate. This increased intensity and shift towards the binding energy of stoichiometric SiO_2 (i.e., 103.5 eV) for most cases suggests formation of higher quality SiO_2 at the interface after the FGA. The level of D_{it} depends on numerous factors, including surface roughness, the stoichiometry and thickness of the interfacial SiO_2 layer, and presence of hydrogen. The differences in the binding energy of the Si(2p) peak does not explain the differences for the D_{it} as a function of interlayer type. However, we do observe a shift post FGA that correlates to the improved electrical performance. Suboxide states of Si induce strain and dangling bonds at the interface, which can trap charges and lead to electronic interface defects.[46] The FGA leading to more stoichiometric SiO_2 at the interface is therefore consistent with a reduced interface state density.

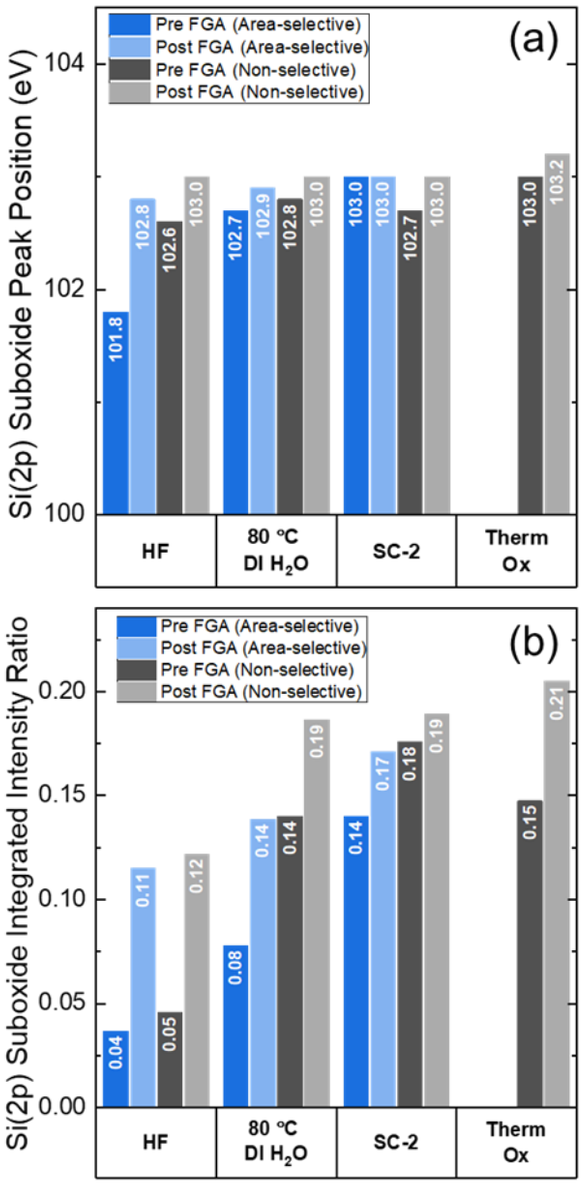

Fig. 6. XPS peak positions of the suboxide Si(2p) peak (a) and ratio of XPS integrated intensity of the suboxide Si(2p) peak to integrated intensity of elemental Si(2p) peak (b) before and after the FGA for area-selective deposition and non-selective deposition $HfO_2/SiO_2/Si$ substrates treated with different SiO_2 interlayer formation techniques.

The Si(2p) suboxide peak from the SC-2 treated area-selective deposition substrate is the only one that does not shift position after the FGA. For the SC-2 pre-

treatment, the Si(2p) spectra from the non-selective deposition substrate indicate a Si suboxide peak shift from 102.7 eV to 103.0 eV after annealing, but the position of the Si suboxide peak from the area-selective deposition substrate remains unchanged at 103.0 eV. The integrated area ratio of the peak did increase, however, suggesting an increase in the amount of interfacial SiO_x consistent with what we observe with the other substrates.

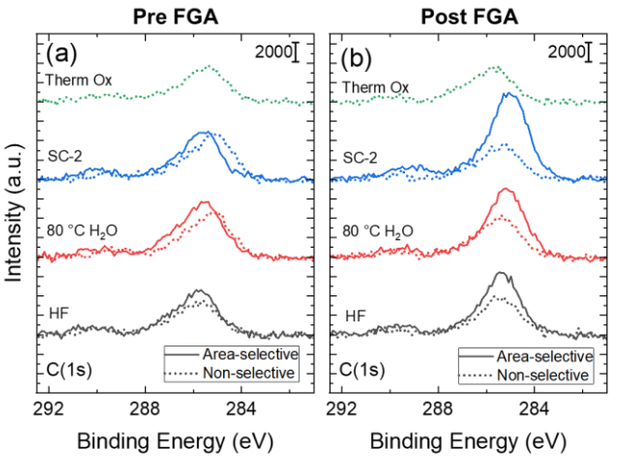

Fig. 7. C(1s) XPS spectra of non-selective (dotted line) and area-selective (solid line) HfO_2 films on Si with different SiO_2 interfacial layers before (a) and after (b) the FGA.

XPS spectra in the C(1s) region for all substrates are shown in Fig. 7. The HfO_2 ALD precursor (TDMAHf) contains methyl carbon groups, so a small amount of carbon is expected in the HfO_2 film in addition to adventitious carbon. Figure 6a shows very similar spectra for all substrates before the FGA, with the small expected C(1s) photoelectron peaks at 285 eV and 289 eV.[47] After annealing however, there is a notable difference between the non-selective and area-selective capacitors. While the C(1s) spectra from the non-selective capacitors show no change in carbon content after annealing, the C(1s) spectra from the area-selective capacitors all show larger carbon

peaks. After the FGA, the atomic percentage of carbon ranges from 6-8% for the non-selective substrates and from 9-12% for the area-selective substrates. This larger atomic percentage of carbon in the area-selective substrates is likely due to carbon residue leftover from the patterned PMMA diffusing up through the HfO_2 film or laterally across the substrate. The average D_{it} of the area-selective and non-selective capacitors is similar, so this extra carbon present on the surface and in the film does not lead to more electrically active defects at the interface. However, the area-selective capacitors do exhibit more variation in performance, indicated by larger standard deviations for D_{it}. The polymer synthesis and KOH etch processing steps for the area-selective deposition substrates can leave more extrinsic defects and impurities in some regions of the substrate, leading to more variability in electrical performance. A more thorough cleaning procedure after patterning the PMMA film should be investigated with future work to minimize the excess carbon observed in the film to ensure more reliable performance between devices.

IV. SUMMARY AND CONCLUSIONS

In summary, Pt-HfO_2-Si MOS capacitors are studied to compare self-aligned area-selective structures with conventional non-selective devices. Various chemical oxidation techniques, including HF-last, 80 °C H_2O, and SC-2 treatment, are used to form an SiO_2 interfacial layer to compare with a high temperature thermal oxidation. The area-selective capacitors perform as well as the non-selective capacitors, and all oxidation treatments exhibit similar electrical performance, with interface state densities near 2 x 10^{11} $eV^{-1}cm^{-2}$ after a FGA. XPS data for the HfO_2-Si interface indicates an increase in

SiO_2 in the interfacial layer after the FGA, which is consistent with the improved interface state density. XPS data also shows presence of extra carbon after annealing the area-selective samples, but this does not significantly impact performance.

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AUTHOR DECLARATIONS

Conflicts of Interest *(required)*

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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FIGURE CAPTIONS

Fig. 1. Schematic diagrams representing the cross-sectional device structure for non-selective capacitors (a) and area-selective capacitors (b).

Fig. 2. Capacitance-voltage characteristics of non-selective (a and b) and area-selective (c and d) Pt-HfO_2-Si MOS capacitors before (a and c) and after (b and d) a FGA. Each graph shows a representative C-V curve of one capacitor with each SiO_2 interlayer treatment: HF, 80 °C H_2O, SC-2, and thermal oxide (non-selective only).

Fig. 3. Conductance-voltage behavior of non-selective (a and b) and area-selective (c and d) Pt-HfO_2-Si MOS capacitors before (a and c) and after (b and d) a FGA. Each graph shows a representative G-V curve of one capacitor with each SiO_2 interlayer treatment: HF, 80 °C H_2O, SC-2, and thermal oxide (non-selective only).

Fig. 4. Estimated D_{it} values for non-selective (black) and area-selective (blue) Pt-HfO_2-Si MOS capacitors before and after the FGA.

Fig. 5. Si(2p) XPS spectra of non-selective (dotted line) and area-selective (solid line) HfO_2 films on Si with different SiO_2 interfacial layers before (a) and after (b) the FGA; (a) and (b) show a narrower region to see the oxidized Si(2p) peaks in more detail; (c) shows the full Si(2p) spectrum of all substrates after the FGA.

Fig. 6. XPS peak positions of the suboxide Si(2p) peak (a) and ratio of XPS integrated intensity of the suboxide Si(2p) peak to integrated intensity of elemental Si(2p) peak (b) before and after the FGA for area-selective deposition and non-selective deposition $HfO_2/SiO_2/Si$ substrates treated with different SiO_2 interlayer formation techniques.

Fig. 7. C(1s) XPS spectra of non-selective (dotted line) and area-selective (solid line) HfO_2 films on Si with different SiO_2 interfacial layers before (a) and after (b) the FGA.

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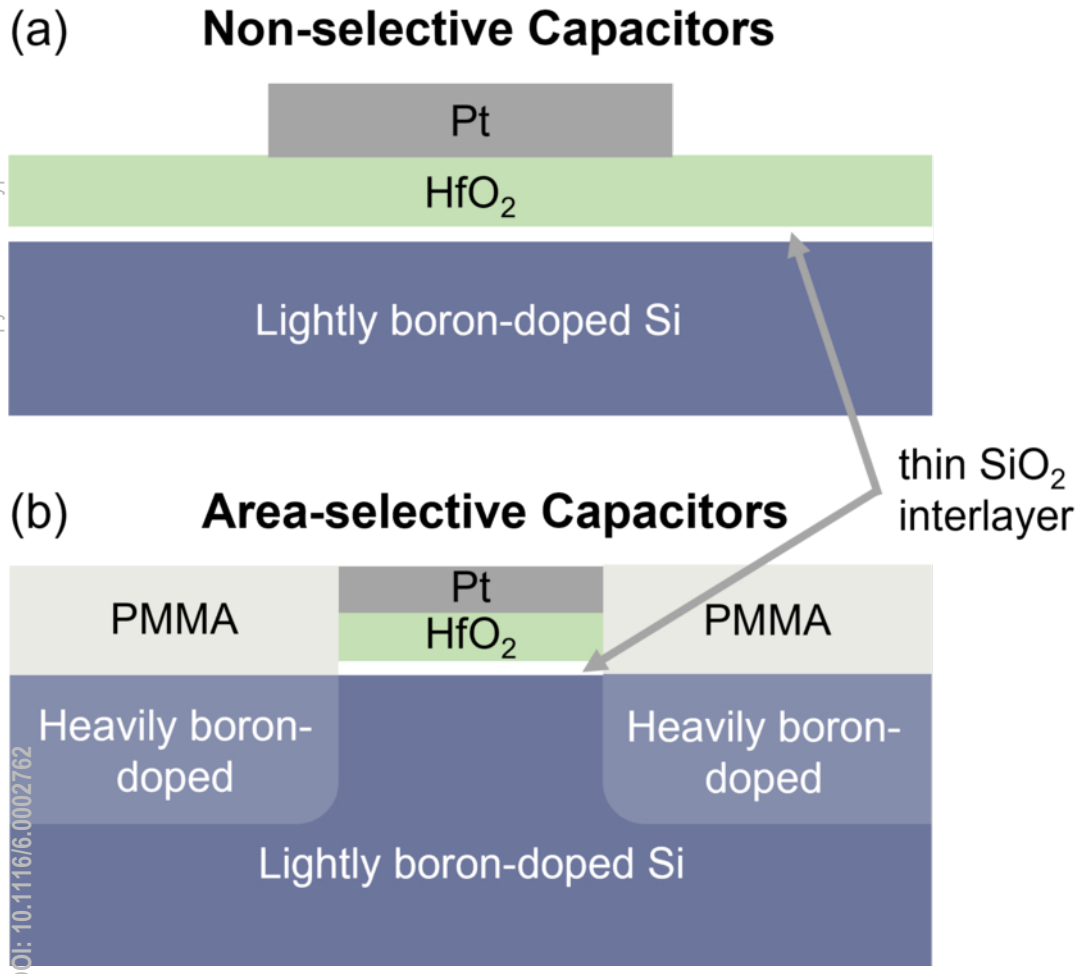

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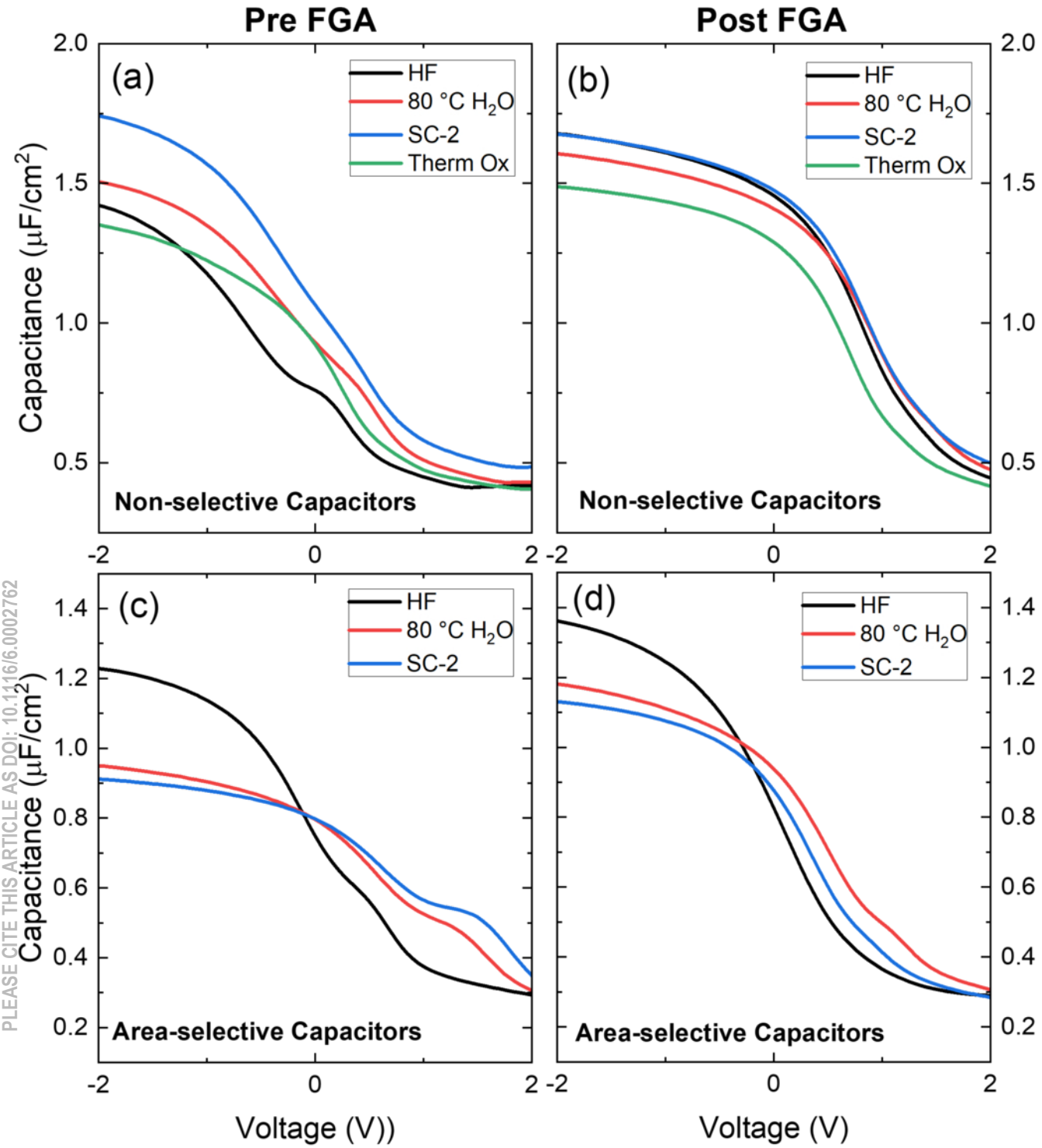

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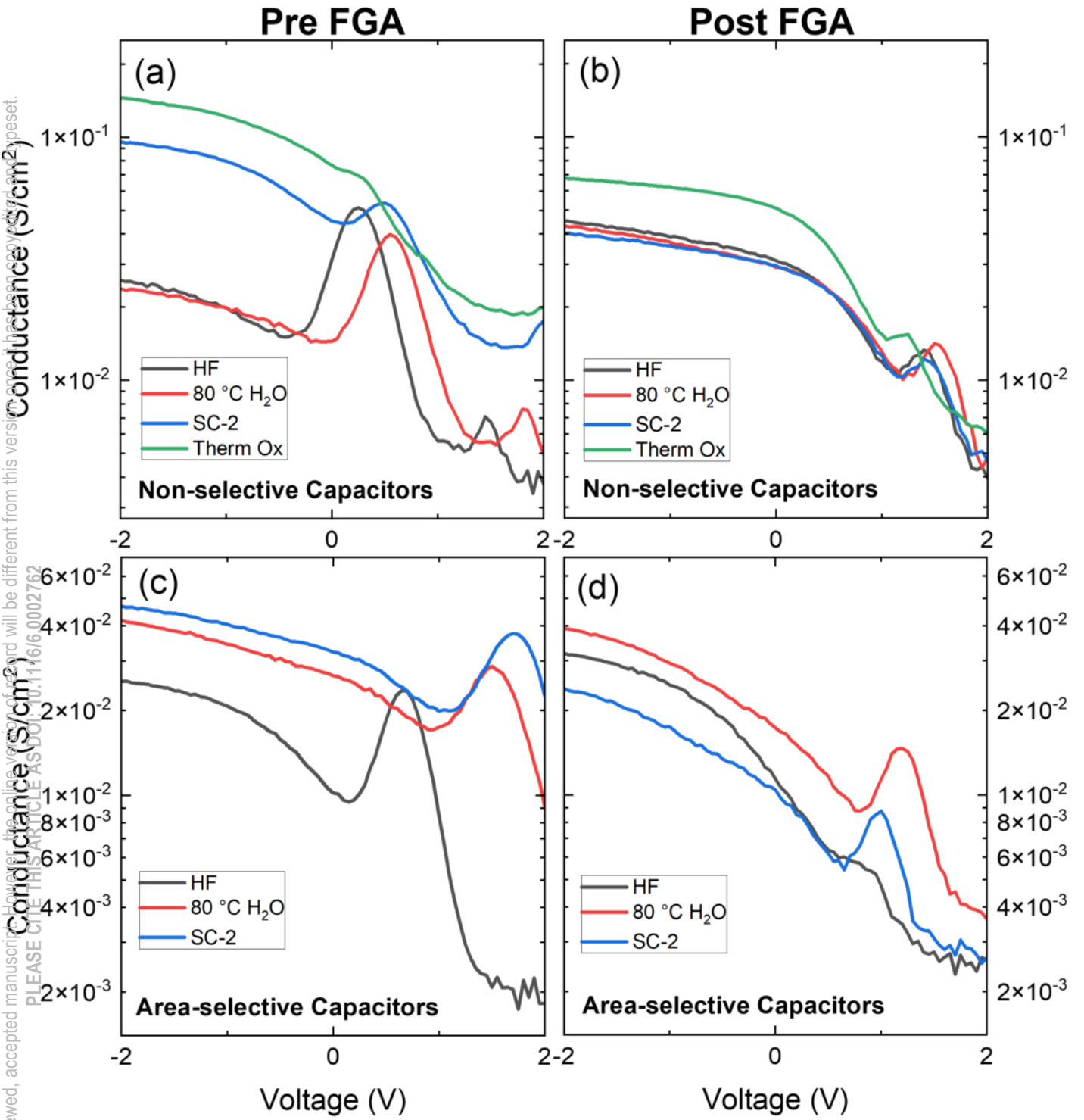

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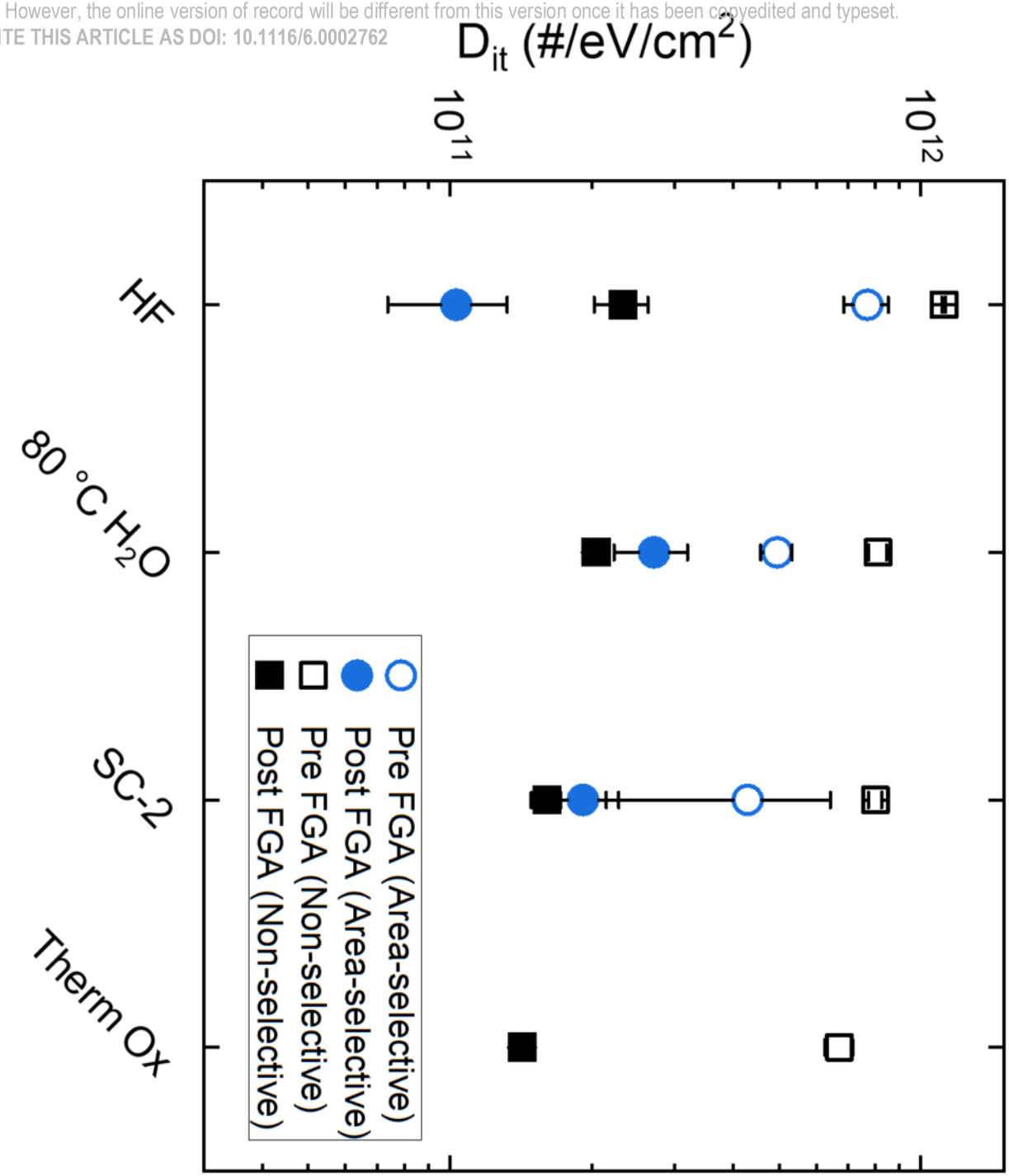

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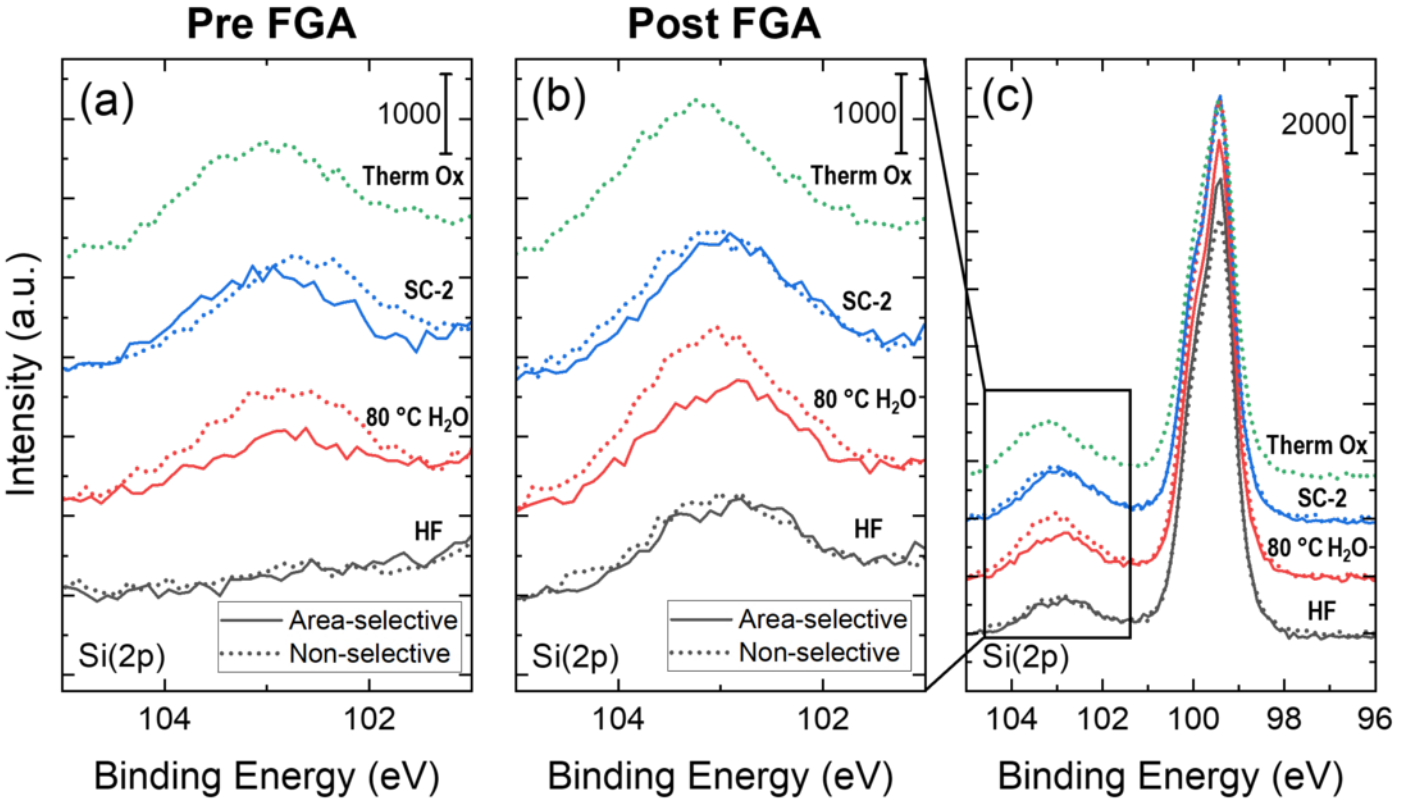

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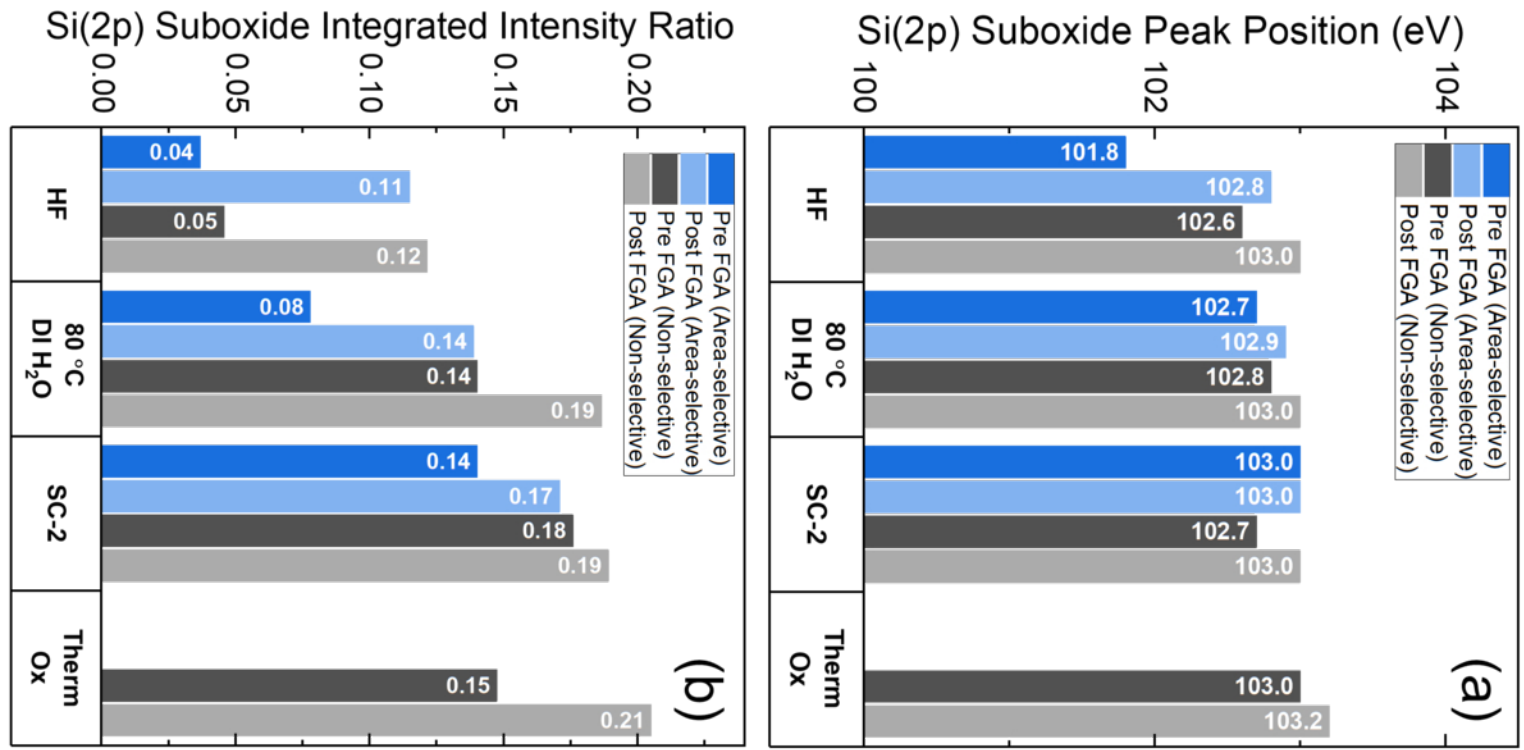

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