Gate Lifetime of P-Gate GaN HEMT in Inductive Power Switching

Bixuan Wang
Center for Power Electronics Systems (CPES)
Virginia Tech
Blacksburg, USA
bixuanwang@vt.edu

Ruizhe Zhang
CPES
Virginia Tech
Blacksburg, USA
rzzhang@vt.edu

Hengyu Wang
Department of Engineering
University of Cambridge
Cambridge, UK
hw595@cam.ac.uk

Quanbo He
Department of Engineering
University of Cambridge
Cambridge, UK
qh243@cam.ac.uk

Qihao Song
CPES
Virginia Tech
Blacksburg, USA
qihao95@vt.edu

Qiang Li
CPES
Virginia Tech
Blacksburg, USA
lqvt@vt.edu

Florin Udrea
Department of Engineering
University of Cambridge
Cambridge, UK
fu10000@cam.ac.uk

Yuhao Zhang
CPES
Virginia Tech
Blacksburg, USA
yhzhang@vt.edu

***Abstract*—The small gate overvoltage margin is a crucial concern in applications of GaN Schottky-type p-gate high electron mobility transistors (SP-HEMTs). The parasitic inductance of the gate loop can induce repetitive gate-voltage (V_G) spikes during the device turn-on transients. However, the gate lifetime of the GaN SP-HEMTs under V_G overshoot in power converters still remains unclear. We fill this gap by developing a new circuit method to measure the gate switching lifetime. The method features several capabilities: 1) *LC*-resonance-like V_G overshoots with pulse width down to 20 ns and dV_G/dt up to 2 V/ns; 2) adjustable power loop condition including the drain-source grounded (DSG) as well as the hard switching (HSW); and 3) repetitive switching test at an adjustable switching frequency (f_{SW}). We use this method to test over 150 devices, and found that the gate lifetimes under a certain peak magnitude of V_G overshoot ($V_{G(PK)}$) can be fitted by both Weibull and Lognormal distributions. The gate lifetime is primarily determined by the number of switching cycles and is higher under the HSW than under the DSG conditions. Finally, the max $V_{G(PK)}$ for 10-year gate lifetime is predicted under different f_{SW} in both DSG and HSW conditions. The results provide direct reference for GaN SP-HEMT's converter applications and a new method for the device gate qualification.**

Keywords—GaN, HEMT, gate, spike, overvoltage, switching, reliability, lifetime, hard switching, power switching

I. Introduction

Gallium nitride (GaN) high-electron mobility transistors (HEMTs) enable very-high-frequency switching in power electronics [1]. The Schottky-type p-gate GaN HEMT (SP-HEMT) has become a popular normally-off GaN device of choice in the market [2]. However, a major concern in their applications is the small V_G headroom between the typical driving voltage and the suggested maximum allowable voltage (as low as 1 V [3]). On the other hand, the common gate-loop inductance in power converters can easily induce the positive gate-voltage (V_G) overshoots in the device turn-on transient. It is thus critical to understand the gate switching lifetime of GaN SP-HEMTs under the application-use conditions.

The current practice for GaN SP-HEMT gate qualification is usually based on HTGB test at V_G=6.5 V [4]. This Si-MOS-based qualification is insufficient for GaN SP-HEMTs due to their higher gate leakage current (I_G) and narrower V_G margin. Many groups have used the accelerated DC tests with V_G = 9~10 V based on a constant stress or step stress [5]–[9]. Recently, the square-wave pulse IV was used to study the gate lifetime [10]–[12].

However, DC and pulse IV do not resemble the device's V_G overshoot in power converters, due to several reasons: 1) the V_G overshoot is usually resonance-like with a waveform different from DC or square-wave, and with a *dv/dt* higher than that in the pulse IV test; 2) in the inductive-load hard switching (HSW), sharp changes in drain-to-source voltage (V_{DS}) and current (I_{DS}) occur concurrently with the V_G overshoot, while prior SP-HEMT gate lifetimes are mostly extracted under the drain-source grounded (DSG) condition. Thus, a new method is needed to characterize the gate lifetime of SP-HEMTs in the inductive power switching.

Recently, we developed a new circuit method to produce V_G overshoot in power converters under both DSG and HSW conditions, and used this method to unveil the dynamic gate breakdown voltage of GaN SP-HEMTs [13]. In this work, we use this method to measure the gate switching lifetime of GaN SP-HEMTs under repetitive switching operations. The gate lifetime's dependences on the switching frequency (f_{SW}) and the peak magnitude of V_G overshoot ($V_{G(PK)}$) are studied. For the first time, the strong impact of the drain switching locus on the gate lifetime is also revealed for GaN SP-HEMTs.

II. Test Setup

A. Device Under Test and Circuit Design

The device under test (DUT) in this work is a 650V/30A rated GaN SP-HEMT [14] (Fig. 1(a)). Fig. 1(b) shows the static I_G-V_G characteristics at temperatures from 25 to 150 °C.

Fig. 2(a) shows the circuit schematics in the DSG condition. The DUT's gate loop comprises an inductor L_G, a low-voltage

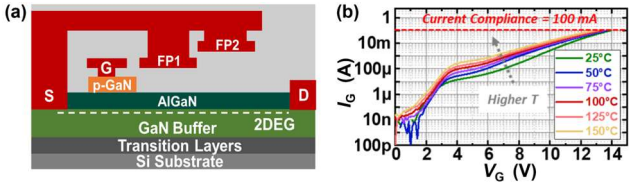

Fig. 1. (a) Schematics of the DUT. (b) Static I_G-V_G-T characteristics with a 0.1-A current compliance measured by Keysight B1505 curve tracer.

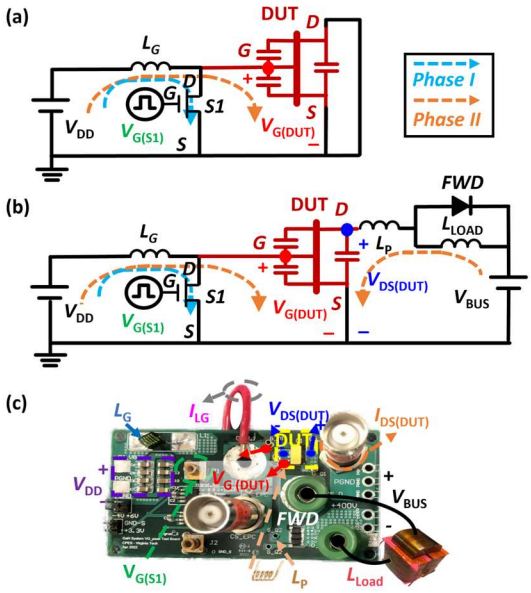

Fig. 2. Circuit schematics and working phases of circuits in (a) drain-source-grounded (DSG) and (b) hard-switching (HSW) conditions. (c) Circuit Photo.

DC source V_{DD} (0.5 V in this work), and a fast switch [15] (S_1). Fig. 3(a) shows the test waveforms in a single pulse. In *phase I*, S_1 turns on, L_G is charged by V_{DD}. In *phase II*, S_1 turns off, energy stored in L_G creates a positive LC-resonant overshoot directly at DUT's gate. Here $L = L_G$, and C can be estimated by the sum of the DUT's input capacitance [C_{ISS}(DUT)] and the S_1's output capacitance [C_{OSS}(S_1)]. The V_G-overshoot pulse width (defined as half of the resonant period) can be tuned by L_G. Once the L_G is selected, the V_G peak magnitude ($V_{G(PK)}$) can be tuned by the on time of S_1. This design shares the similar principle to the unclamped inductive switching circuit, which creates an overshoot on the drain side of the DUT [16]. After the positive overshoot, when DUT's V_G resonates to negative, and S_1 is reversely turned on, setting the DUT's V_G to the S_1's reverse conduction voltage (near -5 V). After that, the DUT's V_G will continue to ring and gradually damped by the loop-parasitic resistance till it is stabilized to be equal to V_{DD}.

To investigate the gate lifetime in HSW, an inductive load is added to the DUT's drain-source loop (Fig. 2(b) and Fig. 2(c)), which comprises a 400-V bus voltage (V_{BUS}), a 24-mH load inductor (L_{LOAD}), a free-wheeling diode (*FWD*) composed of three paralleled diodes [17]. Another 1-µH inductor (L_P) is added to mimic the main-loop parasitics and to suppress the peak I_{DS} and its overlap with high V_{DS} to prevent thermal runaway. Fig. 3(b) shows the test waveforms in a single pulse. When the V_G exceeds the DUT's threshold voltage (V_{TH}), DUT will go through the hard turn on during the V_G overshoot.

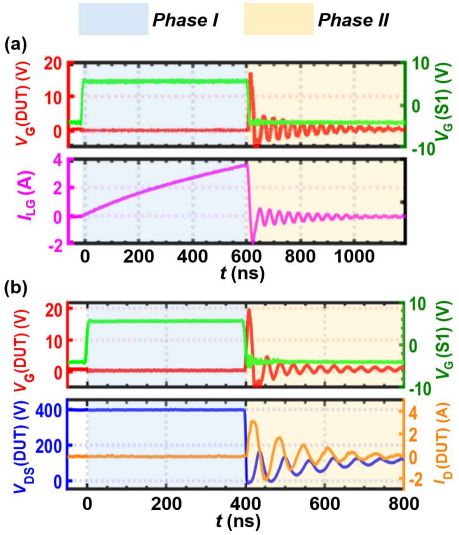

Fig. 3. Typical switching waveforms in a single cycle with V_G overshoot (pulse width = 20 ns) in (a) DSG and (b) HSW conditions.

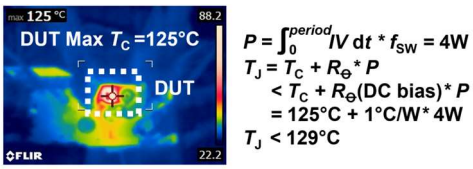

Fig. 4. (Left) Thermal camera image showing the DUT's case temperature (T_C) of 125 °C in switching. (Right) Junction temperature (T_J) estimation. The thermal resistance (R_Θ) is from the datasheet.

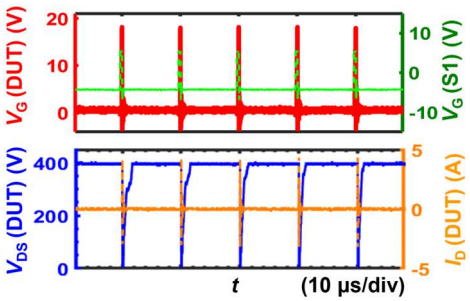

Fig. 5. Repetitive 400V/4A/100kHz HSW waveforms with V_G overshoot ($V_{G(PK)}$= 18V) in each cycle, showing the stable $V_{G(PK)}$ and HSW waveforms for gate lifetime characterization.

B. *Repetitive Switching for Lifetime Measurement*

The gate lifetime is measured under the repetitive switching with V_G overshoots until the DUT failure. We developed a customized program to record the waveform and count the number of switching cycles to failure (SCTF#). To best mimic the fast overshoot in practical applications, the V_G-overshoot pulse width is set as 20 ns. Under this pulse width, the DUT's single-pulse dynamic gate breakdown voltage (BV_{DYN}) is >20 V [13]. This work studies the gate lifetime at various $V_{G(PK)}$ below BV_{DYN}, at f_{SW} = 10 and 100 kHz, and under both DSG and HSW conditions. The DUT's case temperature (T_C) is kept at 125 °C, as heated by a power resistor attached to its case. The junction temperature (T_J) in HSW is estimated to be below 129 °C (Fig. 4). Over 150 devices from the same batch are characterized for

statistical significance. Fig. 5 shows the continuous waveforms under 18-V $V_{G(PK)}$, 100-kHz f_{SW}, and HSW as an example.

III. Test Results

For each test condition, 10 devices were tested to failure. As shown in Fig. 6, in either DSG or HSW condition, the measured SCTF# at 100 kHz shows a reducing trend at higher $V_{G(PK)}$ (15.5 to 17.5 V in DSG condition, and 17.5 to 19.5 V in HSW condition), and the SCTF# of the 10 devices tested at each $V_{G(PK)}$ can be fitted by both the Weibull and lognormal distributions. The Weibull fitting shows a shape factor $\beta > 2$, indicating a wear-out failure.

Also, in each test condition, using either Weibull or lognormal distribution, the SCTF# with failure probability (i.e., the cumulative distribution of failure) at 63% and 1‰ (SCTF#$_{63\%}$ and SCTF#$_{1‰}$) can be extracted, respectively. Then, based on the assumption that the power law relation between the SCTF# and the $V_{G(PK)}$ is valid at lower $V_{G(PK)}$, the maximum $V_{G(PK)}$ for a 10-year switching lifetime at this f_{SW} can be extrapolated from the measured SCTF#$_{63\%}$ and SCTF#$_{1‰}$ at several high $V_{G(PK)}$. As shown in Fig. 7(a), at f_{SW}= 100 kHz, in the DSG condition, $V_{G(PK)}$ = 7.6 and 7.7 V are predicted using the SCTF#$_{63\%}$ extracted from the Weibull and lognormal distributions, respectively, for a failure probability at 63% after 10 years; $V_{G(PK)}$ = 5.7 and 6.1 V are predicted correspondingly using data fitted from two distributions for a failure probability at 1‰ after 10 years. In the HSW condition (Fig. 7(b)), $V_{G(PK)}$ = 12.8 and 12.7 V are expected to cause 63% of the devices to fail after 10 years, using the same extrapolation method; and $V_{G(PK)}$ = 10.1 and 10.8 V are predicted to result in 1‰ of the devices with gate lifetime shorter than 10 years correspondingly.

The SCTF# at the same $V_{G(PK)}$, as well as the extracted maximum $V_{G(PK)}$ for 10-year lifetime, are found to be higher in HSW than those in DSG. This trend is consistent with the BV_{DYN} comparison in HSW and DSG [13], suggesting a similar underlying physics. Such phenomena can be explained by the channel potential lift by high V_{DS}, which reduces the potential drop across the gate stack and the peak electric field in the gate stack [13].

Finally, we studied the f_{SW} dependence of the SCTF#. The mean-SCTF# (MSCTF#) as well as the Weibull distribution of the SCTF# at f_{SW} = 10 kHz are found to be similar to those at f_{SW} = 100 kHz. Fig. 8 shows the exemplar data for two conditions: 1) DSG at $V_{G(PK)}$ = 17.5 V and 2) HSW at $V_{G(PK)}$ = 19.5 V. The similar MSCTF# at two f_{SW} indicates that the gate lifetime is primarily dominated by the switching cycle number instead of the total switching time when the device is switching in a range from 10 to 100 kHz. Based on the assumption that this phenomenon also holds at lower f_{SW} range, we can predict the maximum $V_{G(PK)}$ for a 10-year gate switching lifetime at a certain f_{SW} ($10\,years = SCTF\#/f_{SW}$). Fig. 9 shows the projected maximum $V_{G(PK)}$ for 10-year lifetime at f_{SW} from 100 Hz to 100 kHz, at a failure probability of 63% and 1‰, respectively. Here the SCTF#$_{63\%}$ and SCTF#$_{1‰}$ data extracted from the Weibull distribution are utilized.

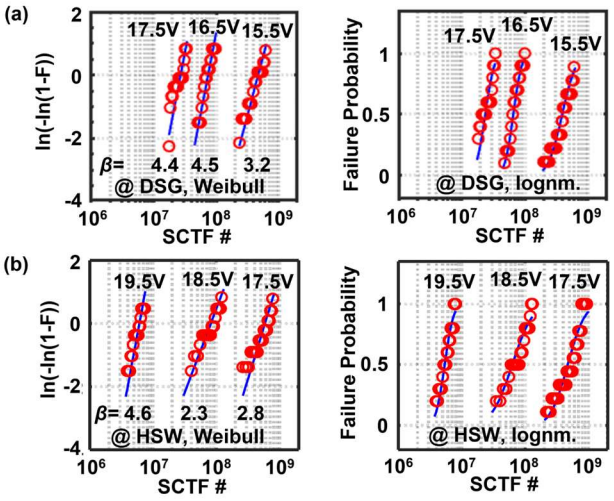

Fig. 6. Switching-cycle-to-failure number (SCTF#) tested at f_{SW}=100 kHz under various $V_{G(PK)}$, in (a) DSG and (b) HSW conditions. In each condition, 10 devices are tested. The SCTF# under each $V_{G(PK)}$ is fitted by (Left) Weibull and (Right) lognormal distributions. (Symbol: test results; line: fitting)

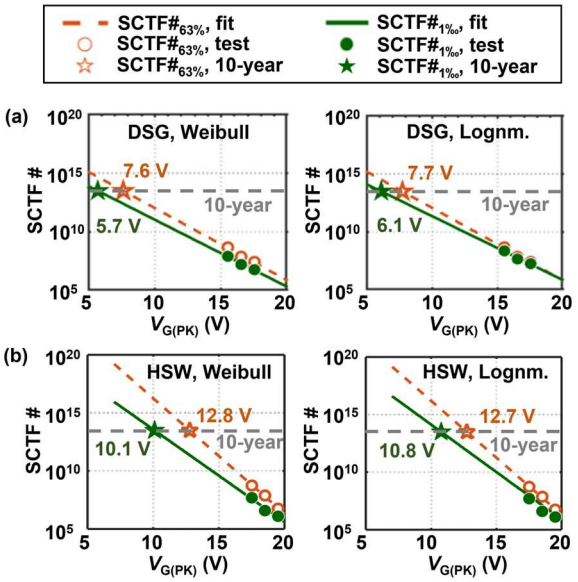

Fig. 7. The max $V_{G(PK)}$ predicted in (a) DSG and (b) HSW for 10-year switching lifetime at f_{SW} = 100 kHz. The prediction is based on a power law extrapolation from the SCTF#$_{63\%}$ and SCTF#$_{1‰}$ data extracted from (Left) Weibull and (Right) lognormal distributions.

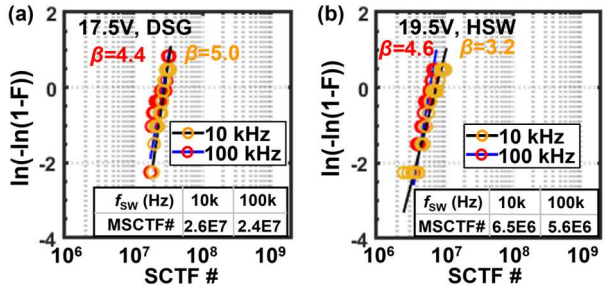

Fig. 8. SCTF# at $V_{G(PK)}$ of (a) 17.5 V in DSG and (b) 19.5 V in HSW, at f_{sw} of 10 kHz and 100 kHz, fitted by Weibull distribution. The mean-SCTF# (MSCTF#) at 10 kHz is close to that at 100 kHz.

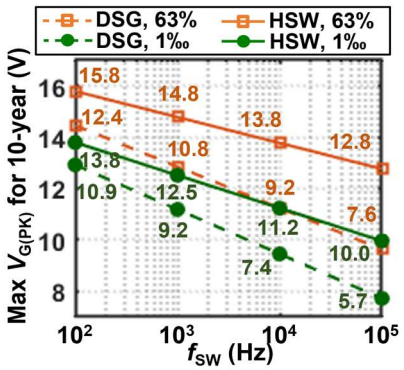

Fig. 9. The projected max $V_{G(PK)}$ for 10-year lifetime as function of f_{sw} (100 Hz ~100 kHz) under the DSG and HSW conditions, at failure probability of 63% and 0.1%. Weibull distribution is used. The max $V_{G(PK)}$ is estimated by assuming the same *SCTF#* ~$V_{G(PK)}$ relation in this f_{SW} range.

IV. Conclusions

This work characterizes the gate switching lifetime of GaN SP-HEMTs using a new circuit method. The circuit features: 1) repetitive, resonant V_G overshoot with practical dV_G/dt; 2) the HSW condition in the main power loop that is not accessible by the conventional DC or pulse-IV tests. Under the same gate overshoot voltage, the gate switching lifetime is found to be higher under the HSW condition than that under the DSG condition. The gate lifetimes of multiple devices tested under the same $V_{G(PK)}$ can be fitted by both Weibull and Lognormal distributions. The extracted SCTF#'s dependence on $V_{G(PK)}$ can be fitted by a power law. The max $V_{G(PK)}$ for 10-year-gate-switching lifetime is predicted at different switching frequencies under both the HSW and DSG conditions. Generally, the gate lifetime is found to be longer under the HSW condition than under the DSG condition at the same $V_{G(PK)}$.

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