A Matrix Autotransformer Switched-Capacitor Converter for Data Center Application

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***Abstract*—This article proposes a matrix auto-transformer switched-capacitor dc–dc converter to achieve a high voltage conversion ratio, high efficiency, and high power density for 48-V data-center applications. On the high-voltage side, the proposed converter can fully leverage the benefits of high-performance low voltage stress devices similar to the multilevel modular switched-capacitor converter. Compared with the traditional isolated LLC converter with a matrix transformer, the proposed solution utilized a matrix autotransformer concept with merged primary and secondary side windings, thus leading to reduced transformer winding loss. The resonant inductor could be integrated into the transformer similar to the LLC converter. Because of the matrix autotransformer design, it can achieve a current doubler rectifier on the low voltage side. For less than 8-V low output voltage application, the current doubler rectifier design can fully utilize the best figure-of-merit 25-V device, which is more efficient than the full-bridge rectifier solution using two 25-V devices during the operation. All the devices can achieve zero voltage switching or zero current switching and can be naturally clamped without additional clamping circuits. A 500-W 48-V to 6-V dc–dc converter hardware prototype has been developed with optimized device selection and integrated matrix autotransformer design. Both simulation and experiment results have been provided to validate the features and benefits of the proposed converter. The maximum efficiency of the proposed converter can reach 98.33%.**

***Index Terms*—Data-center application, LLC, matrix auto-transformer.**

Nomenclature

MASC	Matrix auto-transformer switched-capacitor converter.
TSLI	Total semiconductor loss index.
S_{R1}–S_{R7}	Low-voltage side devices.
S_{W1}–S_{W4}	High-voltage side devices.
C_{R1}–C_{R2}, C_{F1}	Resonant and non-resonant capacitor.
C_{in}, C_{out}	Input and output capacitors.
L_{m}, L_{k}	Derived magnetizing and leakage inductor of the matrix auto-transformer.
n	Derived transformer turn ratio.
Φ_A–Φ_D, Φ_L	Magnetic flux of the four-side cylinder and center cylinder in the matrix auto-transformer.
F_A–F_D	Magnetomotive force of the four windings.
$\Re_s$, $\Re_L$, $\Re_a$, $\Re_m$	Magnetic reluctance of the four-side cylinder, center cylinder as well as the top and bottom plane.
f_{res}, f_{pwm}	Resonant frequency of LC branch and PWM frequency.

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I. Introduction

With the development of artificial intelligence (AI), cloud computing, and mobile internet, a growing number of data-centers have been built all over the world. Currently, the dc distribution system for data center applications is gaining much more attention in industrial circles due to its high power efficiency, and thus replaces the ac distribution system [1], [2]. Fig. 1 shows the typical 48-V power delivery structure for the data-center application. A typical data-center power system input voltage source is a 3-phase 480-V ac voltage through a step-down transformer. A power factor correction ac–dc converter is connected to convert the 3-phase ac to a 400-V dc bus. Then, a 400 to 48-V isolated dc–dc converter is utilized to build a 48-V dc bus system for the data-center rack internal voltage distribution. The galvanic isolation at the rack level for the 48-V dc bus to the low voltage dc IT load, e.g., 1-V CPUs is not mandatory [3]. As a result, both the isolated circuit like LLC converter, and the nonisolated circuit like switched-capacitor converter could be utilized for the 48-V bus to the low voltage dc IT load application. It is a challenge to establish the 48 to 1-V dc power converter, so there are normally two approaches for the 48 to 1-V power delivery converter, i.e., single-stage solution and two-stage solution [1].

For the single-stage solution, the LLC converter can directly achieve 48 to 1.3-V power conversion with peak efficiency at 92.7% [4]. The sigma converter in [5], [6] can directly achieve 48 to 1 V with peak efficiency at 94%. Ref. [7] merges the active bridge converters and regulation stage, and it can realize 48 to 1 V with a peak efficiency of 91.5%. Moreover, a converter

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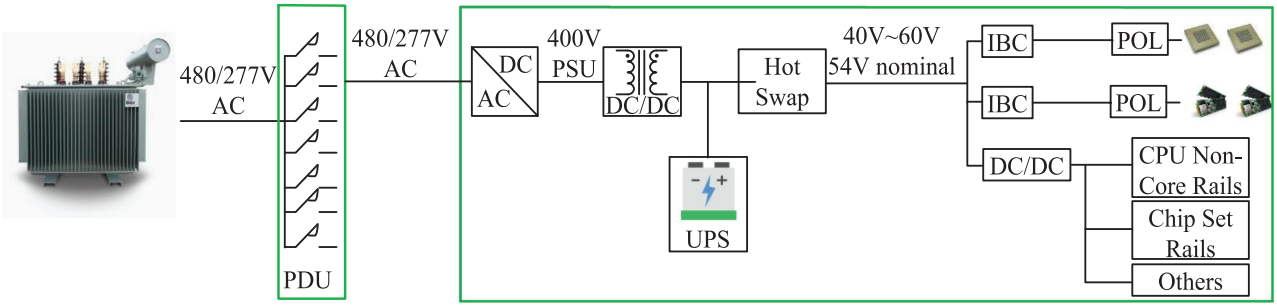

Fig. 1. Typical 48-V power delivery architecture for data-center application.

called LEGO-PoL, which merges a switched capacitor stage and the regulation stage together is proposed in [8] and [9], and it can realize peak efficiency at 91.1% under condition of 48 to 1 V. This LEGO-PoL approach successfully avoids the current spike issue that switched capacitor converter suffers from with the regulation stage inductors, utilizing the soft-charging concept proposed in [10], [11], and [12], and consequently, the intermediate bus capacitors can be also removed. Inspired by this "merging" concept, a variety of single stage converters have been proposed in [13], [14], [15], [16], and [17] that could achieve higher efficiency. However, single-stage solution lacks the flexibility for adapting new CPU loads with new current requirements, the whole 48 to 1-V solution has to be reoptimized, and the control bandwidth could also be a concern compared to the traditional multiphase buck point-of-load solution [18].

Regarding to the two-stage approaches, an intermediate bus converter (IBC) that converts 48 V to an intermediate voltage bus, e.g., 12 V, 6 V, followed by a point-of-load converter that converts the intermediate bus to the load voltage, i.e., 1 V are adopted in the industry. The 12-V intermediate bus has been first adopted in the data center industry for various reasons [18]. The multiphase buck converter is adopted for the point-of-load converter due to its high control bandwidth as well. However, it is very hard to convert 12 to 1 V with high efficiency due to the very high step-down voltage conversion ratio. Lang et al. [19] point out that the power levels of AI accelerator CPU/GPUs are already exceeding 750 W with voltage as low as 0.75 V. And future CPU/GPUs might get even lower core voltage. Therefore, a more optimized lower intermediate bus voltage shall be needed for future applications.

This article will focus on the IBCs for the two-stage solutions with various conversion voltages from 48 V. There exists various dc–dc converter topologies which can be applied to the IBC. Those can be mainly divided into two categories—switched capacitor converters and LLC converters. Switched capacitors converters are originally used for monolithic chip power supply design due to the good integration features without using magnetic components since the 1970s, such as the Dickson converter [20]. Dickson converter is widely adopted in low-power applications, and a Dickson-based switched-capacitor converter, i.e., the multilevel modular switched capacitor converter (MMSCC), has been proposed for high-current high-power applications by replacing the low voltage side single full bridge with multiple half bridges [21], [22]. In this case, the current stress is the same for all devices, which shows tremendous advantages for high current application and modular design. However, for high power and high current application, such traditional switched-capacitor converter still suffers from high current spikes and huge capacitor size issues. To address such issues, a new type of resonant switched-capacitor converter (ReSC) utilizing the magnetic components /air-core inductors /PCB traces to achieve resonant and soft-switching features have been proposed [23], [24], [25]. By utilizing the PCB stray inductance or air-core inductors, a zero current switching (ZCS) MMSCC can be achieved without high current spike issues, and it can also minimize capacitor design. Therefore, ZCS-MMSCC can achieve very high efficiency and high power density designs [24], [26], [27], [28], [29]. To further reduce the capacitor voltage stress for high-voltage applications, a double-wing ZCS-MMSCC has been proposed that can keep all the good features of ZCS-MMSCC, and reduce the capacitor voltage stress by half [30], [31], [32]. Recently, to apply this concept to industry data-center IBC application, our group works with Google to commercialize the technology. We realized that some inductors used in the ZCS-MMSCC could be eliminated without affecting operation, and a better device voltage clamping feature can be achieved. Therefore, the switched tank converter (STC) can be derived from ZCS-MMSCC by removing about half inductors, and all the devices can be naturally clamped, which is preferred for high-volume industry applications [33], [18], [34], [35], [36], [37]. The 48-V STC with 4x conversion ratio can realize 98.9% peak efficiency [34]. The 48-V STC with 6x conversion ratio can realize 98.55% peak efficiency [33]. The 8x STC can realize 98.53% peak efficiency by estimation without considering PCB loss [36]. However, the ZCS-MMSCC and STC are all zero current switching solutions that cannot recycle the device output capacitor, i.e., C_{oss} loss during the switching. Therefore, the light load efficiency is still relatively low. To recycle the C_{oss} loss, a phase-shift control method could be implemented for the ZCS-MMSCC, and a new zero voltage switching mode could be achieved with reduced device RMS current and recycle C_{oss} loss [38], [39]. And a 4x ZVS-MMSCC for 48-V application has been built that can achieve 99.35% peak efficiency for the data-center application [40]. Many other switched capacitor circuits besides the Dickson-derived circuit utilizing the resonant concept can also achieve high efficiency and high power density for 48-V data center applications. The cascaded resonant switched capacitor converter in [41] and

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TABLE I
COMPARISON OF IBC FOR DATA-CENTER APPLICATION

Reference	Topology Category	Voltage ratio	Max Output current	Power Density(W/inch^3)	System Efficiency (%)
[34]	STC (Google Adopted)	48 to 12 V (4x)	58 A	500	Full load: 97.7%(Iout=58 A) Peak: 98.9% (Iout=15 A)
[40]	ZVS-MMSCC	48 to 12 V (4x)	50 A	795	Full load: 97.5%(Iout=50 A) Peak: 99.35% (Iout=8.5 A)
[41]	Cascaded multi-resonant ReSC	54 to 13.5 V (4x)	60 A	4700	Full load: 98.14% (Iout=60 A) Peak: 98.99% (Iout=13 A)
[53]	Hybrid switched capacitor converter	54 to 13.5 V (4x)	62.5 A	-	Full load: 97.15% (Iout=62.5 A) Peak: 99.1% (Iout=10 A*)
[33]	STC	54 to 9 V (6x)	50 A	750	Full load: 97.18% (Iout=50 A) Peak: 98.55% (Iout=13 A)
[43]	Series-Parallel based ReSC	48 to 6 V (8x)	70 A	2140	Full load: 95.1% (Iout=70 A) Peak: 98% (Iout=15 A*)
[44]	Fibonacci based ReSC	48 to 6 V (8x)	40 A	1675	Full load: 95.9% (Iout=40 A) Peak: 98% (Iout=12 A)
[45]	LLC Converter	48 to 6 V (8x)	150 A	1200	Full load: 97.6% (Iout=150 A) Peak: 98.1% (Iout=75 A)
[19]	Hybrid switched capacitor converter (HSC:Infineon adopted)	48 to 6 V (8x)	90 A	-	Full load: 96.4% (Iout=90 A) Peak: 98.34% (Iout=25 A*)
[54]	Hybrid switched capacitor converter (HSC)	48 to 6 V (8x)	130 A	-	Full load: 97.2% (Iout=130 A) Peak: 98.15% (Iout=50 A)
[57]	Hybrid ReSC	48 to 3.4 V (13x)	140 A	415	Full load: 91.7% (Iout=140 A) Peak: 96.3% (Iout=30 A)
-	MASC (Proposed Circuit)	48 to 6 V (8x)	83 A	767.4	Full load: 97.09% (Iout=76.6 A) Peak: 98.33% (Iout=26.7 A)

[42] can achieve 98.99% peak efficiency with 4x conversion ratio. The resonant series–parallel switched capacitor converter with 8x conversion ratio can realize 98% peak efficiency [43]. The Fibonacci-based ReSC with 8x conversion ratio shows the ability to reach 98% peak efficiency [44]. A 4x unregulated LLC converter can realize 98.4% peak efficiency and 8x unregulated LLC converter can reach 98.1% peak efficiency [45], [46], [47] with high-performance autotransformer design [48], [49], [50], [51].

Table I shows the comparison of different IBCs for data-center applications. Both the cascaded ReSC in [41], STC in [34], and ZVS-MMSCC in [40] can realize very good performance for 4x conversion ratio. However, cascaded ReSC is difficult to keep high efficiency to extend its conversion ratio from 4x to 8x, because under this case all the cascaded inner stages have to process all the power [36], [52]. Instead, STC and ZVS-MMSCC can be extended to 8x with better performance because of the input series output parallel structure, but they still suffer from high loss issues for the high current application at heavy load due to the "full-bridge" like rectifying structure on the high current low voltage side [33], [18], [36], [40]. Series–parallel-based ReSC in [43] and Fibonacci-based ReSC in [44] can easily realize 8x conversion ratio, but the low voltage stress device cannot be fully utilized, therefore the efficiency will decrease to less than 96% at heavy load. The LLC converter in [45] can keep its efficiency higher than 97.6% at full load. Therefore, the LLC converter seems to be a more attractive choice for 8x IBC. The main reason why LLC converter can keep relatively higher efficiency at heavy load is that the current doubler rectifier structure only requires the transformer winding and one single device to conduct the current in each loop. Besides, it is possible to design a transformer winding with a smaller resistance than a semiconductor device. Therefore, the current doubler rectifier could achieve better performance than a full-bridge rectifier for low-voltage applications. If the current doubler rectifier is introduced into the switched capacitor converter like STC to replace its full-bridge rectifier on the low voltage side, the efficiency could be improved as well. A circuit called a hybrid switched capacitor converter (HSC) that merges the current doubler rectifier and switched capacitor converter has been proposed in [53], [54], [55], [56], and [62] and it can realize better performance at both light and heavy loads. However, this converter also possesses many issues. First, it is hard to extend its conversion ratio higher than 8x. Although the conversion ratio is increased to 14x [57], extra inductors are required, and the resonant frequency has to be adjusted to the same value. Second, the output current is concentrated to a single point, which would cause a large termination loss under the large current situation. Third, the transformer turns of the windings are not the same, resulting in difficulty in design and more copper loss which can be further shown in Table III. Moreover, a matrix transformer with integrated inductors could be used to save the inductor counts in [58], [59]. Based on the analysis above, this article proposes an MASC with the following two major contributions.

1) The first contribution would be the newly proposed rectifier structure that replaces the traditional low-voltage rectifier side of STC to further improve the system efficiency for data center applications.
2) The second contribution is that the RMS current through the newly proposed integrated matrix autotransformer's winding is less than LLC converter's power loss. Moreover, the primary side windings of the proposed integrated matrix autotransformer are removed. Therefore, the copper loss is greatly reduced compared with traditional isolated LLC converter. The core size and electrical parameters of traditional 8x LLC and the proposed 8x MASC are still the same, while the proposed 8x MASC's transformer copper loss is just 17.1% compared to 8x LLC's transformer copper loss.

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TABLE II
KEY PARAMETERS OF THE PROTOTYPE

V_{in}	46–50 V
$Vout$	5.75–6.25 V
P_{in}	0–500 W
f_{res}	445 kHz
f_{PWM}	417 kHz
C_{in}	22 μF×3 (X7S,100 V) C5750X7S2A226M280KB
C_{out}	47 μF×9(X5R,10 V) C4532X5R1A476M280KA
C_{F1}	22 μF×2(X7R,50 V) CGA9P3X7R1H226M250KB
C_{R1} & C_{R2}	1.4 μF(U2J,50 V) C1812C145J5JLC7805
S_{R1}~S_{R7}	BSZ010NE2LS5ATMA1(25 V,1 mΩ)
S_{W1}~S_{W5}	BSZ018N04LS6ATMA1 (40 V,2.1 mΩ)
Gate Driver	8×1EDN7136GXTMA1
PCB	39 mm× 39 mm (10 layer, 4oz, 2borads)
Core	ML95S@Hitachi Company

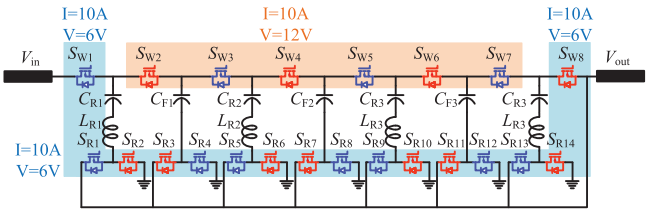

Fig. 2. 48 to 6 V(8x) STC working at 300 W.

The rest of this article is organized as follows. Section I makes a comprehended review of dc–dc converter for data center application. A detailed explanation of contributions is introduced in Sections II and III. The operation principle of the circuit is introduced in Section IV. The design consideration of MASC is described in Section V. Both simulation and experimental results are shown in Section VI. Finally, Section VII concludes this article.

II. CHALLENGES OF HIGH CONVERSION RATIO RESC FOR LOW OUTPUT VOLTAGE APPLICATIONS

STC is one typical kind of ZCS-MMSCC that has been widely studied and adopted in data center applications due to its high efficiency as well as high power density performance [18]. In this section, the STC is adopted as an example to show the challenge that ReSC suffers from for data center applications.

Fig. 2 shows an 8x STC with an output voltage of 6 V. The voltage stress of the low voltage side devices S_{R1}–S_{R14} is 6 V. So it is reasonable to adopt 12-V devices for S_{R1}– S_{R14}. Assuming

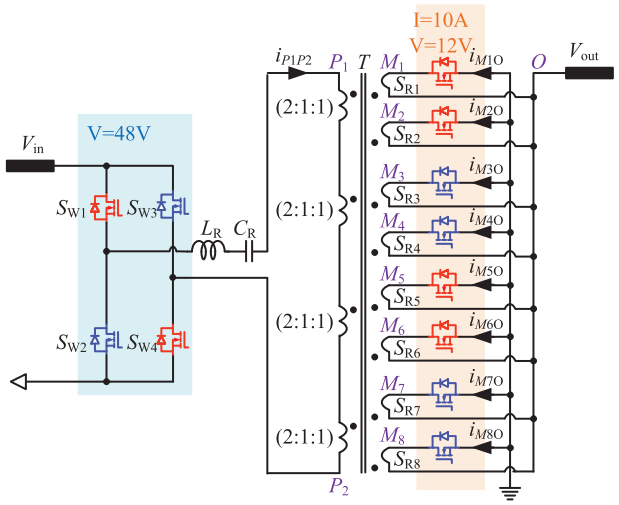

Fig. 3. 48 to 6 V(8x) LLC in [58] converter working at 300 W.

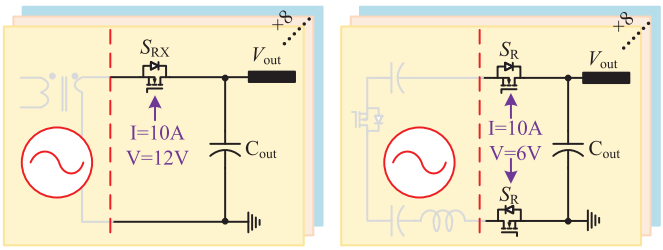

Fig. 4. Low voltage side devices' voltage and current stress at 300 W. (a) LLC: 12 V & 10 A. (b) STC: 6 V & 12 A.

the input power is 300 W, then the RMS current stress through each device is 10 A.

On the other hand, LLC converter has been proven to be a very good candidate for the high conversion ratio dc–dc converter due to its high efficiency and high power density features in [45]. Fig. 3 demonstrates the 48 to 6-V LLC converter working at 300 W in [58]. It has full bridges on the primary side and a matrix transformer as well as the current doubler circuit on the secondary side. The voltage stress of devices S_{R1}–S_{R8} on the secondary side is 12 V, and the RMS current stress through every device is also 10 A. Therefore, it is reasonable to adopt 25-V devices for S_{R1}–S_{R8}.

Detailed comparison results of the low voltage side circuits for both 8x LLC and 8x STC are illustrated in Fig. 4. For every secondary side current loop from 8x LLC converter, there is one device conducted with its voltage stress is 12 V. So 25-V voltage rating devices can be used. For low voltage side current loop from 8x STC, there are two devices in series conducted with their voltage stress are 6 V. So, 12 or 25-V voltage rating devices can be adopted. Fig. 5 shows the targeted low-voltage devices used for the comparison. Moreover, there are eight current loops in total for both 8x LLC and 8x STC. So the counts of the low voltage side devices for the current doubler circuit are just half of the devices compared with STC's, while its voltage

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TABLE III
COMPARISON OF THE PROPOSED 8X MASC AND THE HSC UNDER THE CONDITION THAT INPUT POWER IS 300 W, AND THE AUTOTRANSFORMER SIZE IS THE SAME

		Proposed 8x MASC	Two phases interleaved 8x MASC	Single phase 8x HSC	8x HSC in [53] ,[54],[55], [56], [62] (Two phases interleaved)
Copper Loss		33.3% p.u.	33.3% p.u.	1 p.u.	1 p.u.
High voltage Side devices stress	Voltage	4x(24 V)	4x(24 V)	8x(48 V)	8x(48 V)
	Current	1x(10 A)	0.5x(5 A)	1x(10 A)	0.5x(5 A)
	Counts	3	6	1	2
High voltage Side devices stress	Voltage	2x(12 V)	2x(12 V)	6x(36 V)	6x(36 V)
	Current	1x(10 A)	0.5x(5 A)	1x(10 A)	0.5x(5 A)
	Counts	1	2	1	2
Low voltage Side devices stress	Voltage	2x(12 V)	2x(12 V)	2x(12 V)	2x(12 V)
	Current	1x(10 A)	0.5x(5 A)	1x(10 A)	0.5x(5 A)
	Counts	7	14	7	14
Resonant Capacitors Counts		2	4	1	2
Non-Resonant Capacitors		1	2	/	/
Output Capacitors		The same			
Input Capacitors		The input capacitance of single phase MASC/HSC is 5 times larger than two-phase interleaved MASC/HSC under the condition that input voltage ripple is equal			

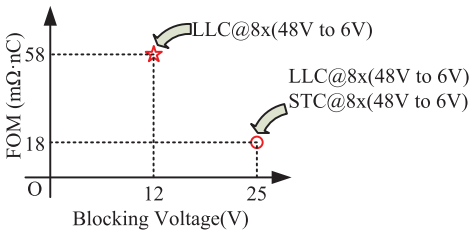

Fig. 5. Target devices for 8x LLC and 8x STC on the low voltage side.

stress is doubled. To demonstrate which topology is better in Fig. 4, a method called TSLI in [37] that reveals the relationship between devices' die area and power loss is then adopted to prove that less power loss can be realized by the current doubler circuit shown in Fig. 4(a). For a specific technology device, its conduction resistance is expressed in (1), and its gate driver total charges as well as output capacitance are expressed in (2) and (3). A_{die} is the die area of the device, γ, β, ξ are the coefficients related to semiconductor technology. The resistance is inversely proportional to its die area [60]. Its gate charges and output capacitance need to be proportional to the die area [61]

$$R_{ds(\text{on})}\, A_{\text{die}} = \xi \tag{1}$$

$$\frac{Q_g}{A_{\text{die}}} = \beta \tag{2}$$

$$\frac{C_{\text{oss}}}{A_{\text{die}}} = \gamma. \tag{3}$$

Since the ZCS can be realized on the low voltage side for both circuits shown in Fig. 4, the TSLI for the low voltage side devices can be expressed in (4), where P_{cond}, P_{Gate}, and P_{Coss} represent the conduction loss, gate driver loss, and output capacitor loss, respectively. Combine the (1)–(4), the detailed TSLI for the low voltage side devices are expressed in (5) and (6), where TSLI_{A}, TSLI_{B} represent the total power loss of the circuit shown in Fig. 4(a) and (b) respectively. I_{RMS} is the current RMS value through the device, V_{g} is the gate voltage of the device, C_{oss} is the output capacitance, f is the switching frequency, V_{ds} is the drain to source voltage across the device during off-time, and A_{die} is the die area. N_1 and N_2 are the total counts of low voltage side devices of STC and LLC, respectively, in Fig. 4

$$\text{TSLI} = \frac{(P_{\text{cond}} + P_{\text{Gate}} + P_{\text{Coss}}) \times N}{P_{IN}} \tag{4}$$

$$\text{TSLI}_A = \frac{\left(\frac{I_{\text{RMS}}^2 \cdot \xi}{A_{\text{die}}} + \beta A_{\text{die}} V_g f + \gamma A_{\text{die}} V_{ds}^2 f\right) \times N_1}{P_{IN}} \tag{5}$$

$$\text{TSLI}_B = \frac{\left(\frac{I_{\text{RMS}}^2 \cdot \xi}{A_{\text{die}}} + \beta A_{\text{die}} V_g f + \gamma A_{\text{die}} (2V_{ds})^2 f\right) \times N_2}{P_{IN}}. \tag{6}$$

Taking a 48 to 6 V, 300-kHz converter at 300 W as an example, the TSLI of the low voltage side devices for both STC and LLC is shown in Fig. 6. Obviously, the current doubler circuit shown in dashed purple line has less power loss compared with full bridge shown in solid purple line, and around 37.5% efficiency can be improved with about 80-mm^2 total device die area. Moreover, the power loss when 12-V devices are adopted is much higher than the 25-V devices as shown in the purple dotted line in Fig. 6.

Since the current doubler circuit is better than the full bridge circuit from the power loss point of view, we propose a matrix autotransformer switched-capacitor dc–dc converter which is also called MASC. It merges the benefits of the current doubler circuit with the high voltage side of the STC, as shown in Fig. 7. On the high voltage side, the circuit structure is similar to the STC while the circuit on the low voltage side changes to current doubler circuit. Assume the input is 48 V and the output is 6 V with 300-W input power in Fig. 7, then the current stress through all the devices is 10 A, and the voltage stress of the high voltage

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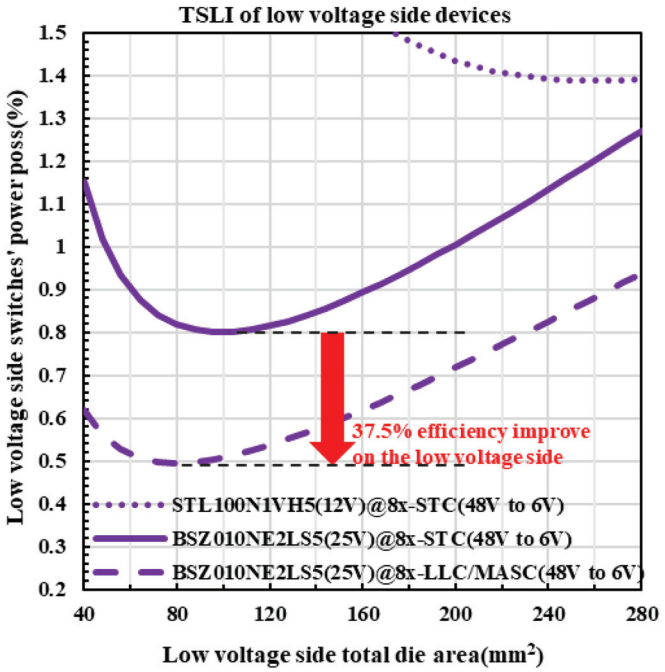

Fig. 6. SLI of low voltage side devices for 8x-LLC & 8x-STC with target devices.

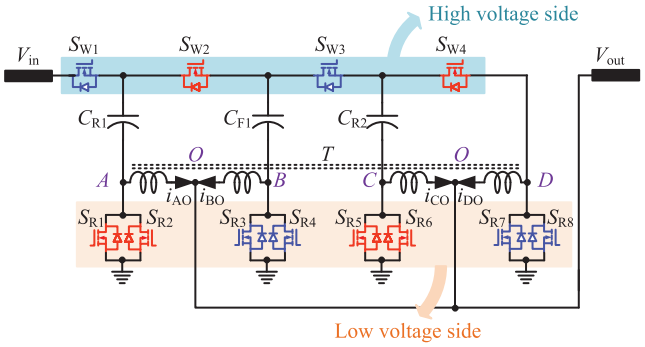

Fig. 7. Proposed MASC that merges the low voltage side of LLC and the high voltage side of STC.

side devices is 24 V, while the low voltage side devices voltage stress is 12 V.

III. Transformer Copper Loss Comparison Between the Proposed MASC and LLC Converter

The proposed MASC in Fig. 7 can save 37.5% power loss compared to STC for low-voltage devices. Moreover, the transformer copper loss between the proposed MASC and LLC converter is compared in this section. Figs. 8 and 9 demonstrate the current waveforms through the windings of MASC and LLC converter, respectively. In Fig. 8, the subscripts AO, BO, CO, and DO refer to windings labeled in Fig. 7. In Fig. 10, the subscripts M_1O–M_8O and P_1P_2 refer to windings labeled in Fig. 3. For the proposed MASC, the current through the autotransformer's windings is in full wave rectifier mode, while the current through the LLC's transformer windings is in half wave rectifier mode.

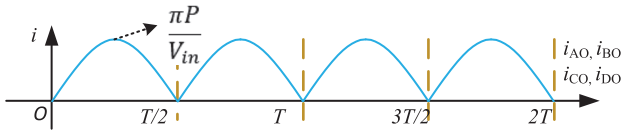

Fig. 8. The current through the proposed MASC's autotransformer windings in Fig. 7. (AO, BO, CO, DO are the windings labeled in Fig. 7).

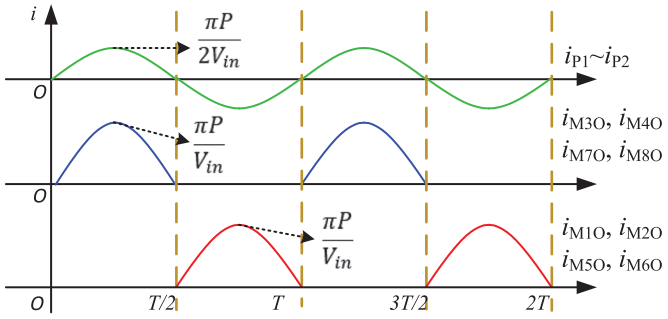

Fig. 9. Current through the LLC's transformer windings in Fig. 3. (M_1O–M_8O & P_1P_2 are the windings labeled in Fig. 7).

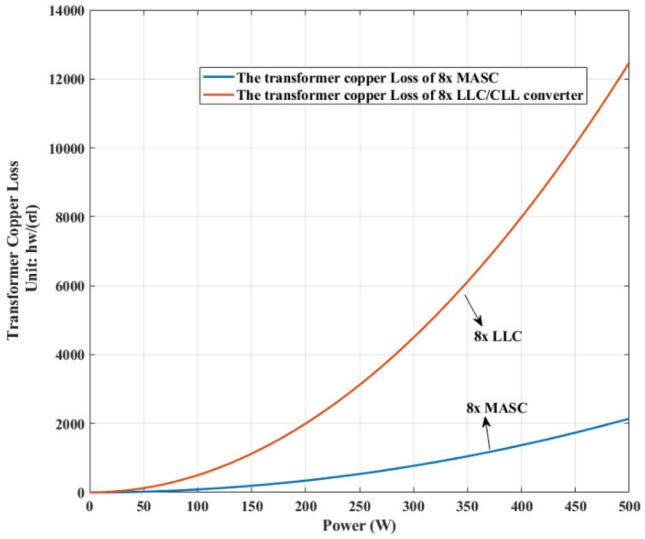

Fig. 10. Copper loss comparison between MASC and LLC under the condition that the core size and electrical parameters are the same.

Therefore, the total RMS current through the windings of the MASC is less than the total RMS current through the secondary side of LLC's when the output power is the same. This will lead to less autotransformer copper loss compared with LLC's under the condition that core size and PCB thickness are the same. Moreover, removing the primary side windings of the proposed MASC further reduces its transformer copper loss compared with LLC. As a result, the transformer's copper loss of the proposed 8x MASC is just around 17.1% compared with 8x LLC converter shown in Fig. 10, when all the electrical parameters and magnetic core size are the same. h, w, σ, l are copper thickness, width, resistance coefficient of the copper, and the length of one turn. The detailed derivation is shown in Appendix II.

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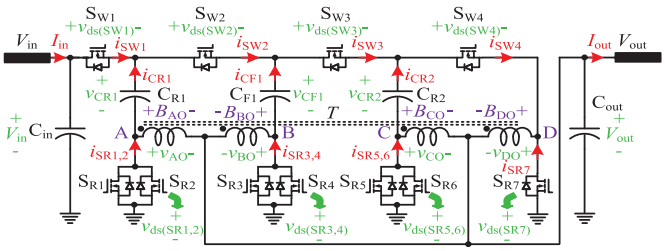

Fig. 11. Specific labels of the all the current (red color), voltage (green), and magnetic flux density (purple).

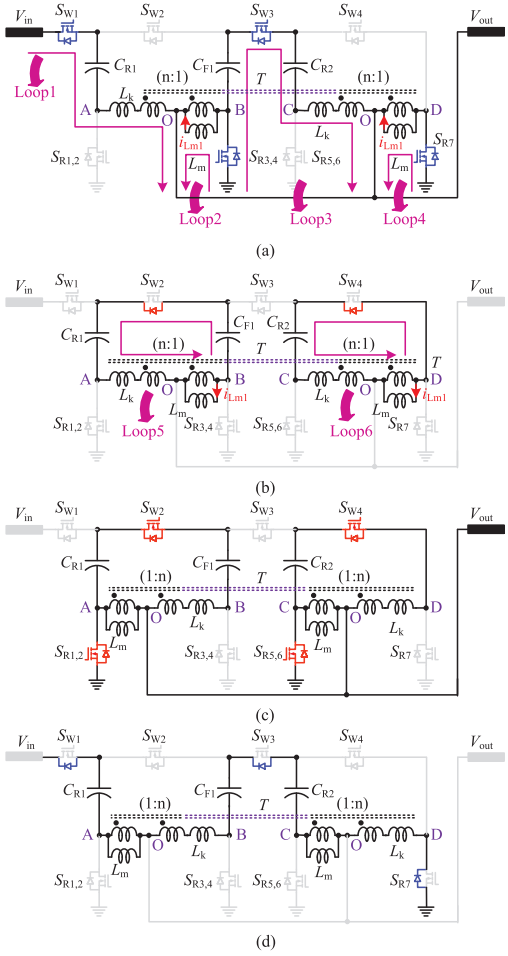

Fig. 12. Operation principle of the 8x MASC during one period. (a) Time t_0–t_1. (b) Time t_1–t_2. (c) Time t_2–t_3. (d) Time t_3–t_4. (a) The circuit commutation loops during time t_0–t_1 in Fig. 13. (b) The circuit commutation loops during time t_1–t_2 in Fig. 13. (c) The circuit commutation loops during time t_2–t_3 in Fig. 13. (d) The circuit commutation loops during time t_3–t_4 in Fig. 13.

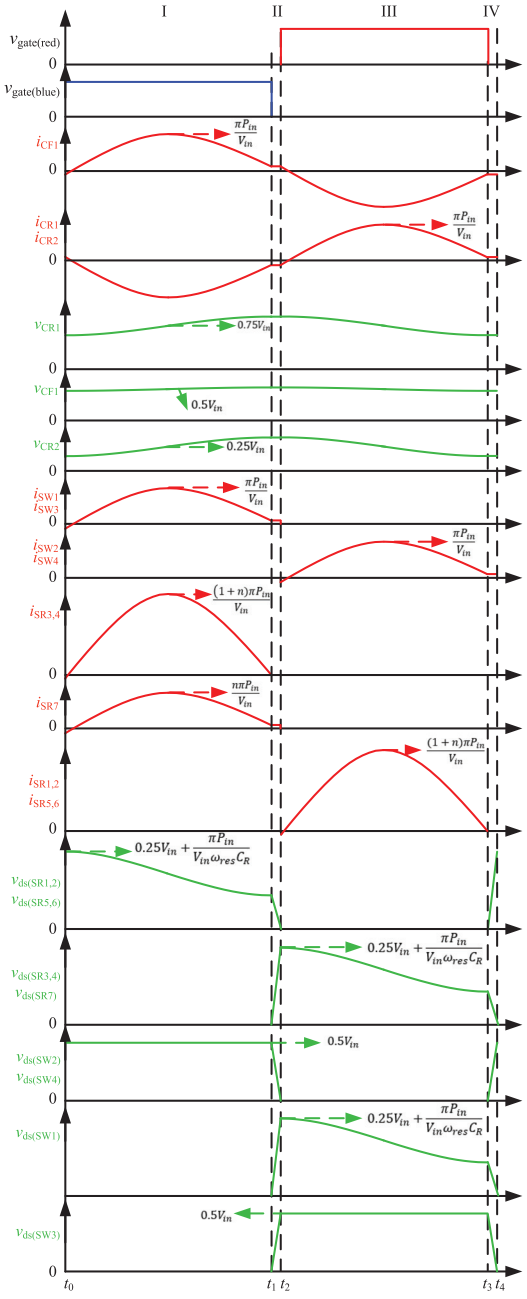

Fig. 13. Main waveforms during one period.

IV. Operating Principle of MASC

To analyze the working principle of the proposed MASC circuit, the voltage, current, and magnetic flux density labels are shown in Fig. 11. The red, green, and purple labels represent current, voltage, and magnetic flux density, respectively.

Figs. 12 and 13 show the working principle of the proposed circuit during one period, and the low voltage side parallel devices are merged to simplify analysis. For instance, S_{R1} and S_{R1} are merged as $S_{R1,2}$. The integrated transformer model and its equivalent circuit are shown in the Appendix and it can be modeled as two independent autotransformers with turn ratio n, and their magnetizing inductors as well as leakage inductors are labeled in L_m and L_k, respectively. The circuit commutation loops are mainly divided into four stages shown in Fig. 12, including the two-half cycle resonant stages and the two dead time transition stages. The current and voltage through windings AO–DO in Fig. 12(a) are expressed in (7) and (8)

$$\frac{i_{AO}(t)}{i_{BO}(t)-i_{Lm1}(t)}=\frac{i_{CO}(t)}{i_{DO}(t)-i_{Lm1}(t)}=\frac{1}{n} \tag{7}$$

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$$\begin{cases} v_{\mathrm{AO}}(t) = nv_{\mathrm{OB}}(t) + L_k \frac{di_{\mathrm{AO}}(t)}{dt} = nV_{\mathrm{out}} + L_k \frac{di_{\mathrm{AO}}(t)}{dt} \\ v_{\mathrm{CO}}(t) = nv_{\mathrm{OD}}(t) + L_k \frac{di_{\mathrm{CO}}(t)}{dt} = nV_{\mathrm{out}} + L_k \frac{di_{\mathrm{CO}}(t)}{dt}. \end{cases} \tag{8}$$

Suppose $C_{\mathrm{R1}} = C_{\mathrm{R2}} = C_{\mathrm{R}} = 0.1C_{\mathrm{F1}}$, and the resonant frequency of "Loop 1" can be expressed in (9). By assuming the input power P_{in}, the peak current through capacitor C_{R1} can be expressed in (10). The peak magnetizing current $I_{\mathrm{Lm(peak)}}$ through magnetizing inductor L_{m} can be expressed in (11), where T_{res} is the resonant period

$$f_{\mathrm{res}} = \frac{1}{2\pi\sqrt{L_K\left(\frac{C_{R2}C_{F1}}{C_{F1}+C_{R2}}\right)}} = \frac{1.049}{2\pi\sqrt{L_K C_R}} \approx \frac{1}{2\pi\sqrt{L_K C_R}} \tag{9}$$

$$I_{C_{R1}(\mathrm{peak})} = \frac{2\pi P_{\mathrm{in}}}{V_{\mathrm{in}}\int_0^{\pi}\sin(\omega_{\mathrm{res}}t)\,d(\omega_{\mathrm{res}}t)} = \frac{\pi P_{\mathrm{in}}}{V_{\mathrm{in}}} \tag{10}$$

$$I_{Lm(\mathrm{peak})} = \left|\frac{v_{\mathrm{OB}}T_{\mathrm{res}}}{4L_m}\right| = \frac{V_{\mathrm{out}}}{4f_{\mathrm{res}}L_m}. \tag{11}$$

During stage I, the current through $S_{\mathrm{w1}}, S_{\mathrm{w3}}$ and the capacitors C_{R1}, C_{F1}, C_{R2} are expressed in (12) and (13). Combined with the peak current of the magnetizing inductor, the instantons magnetizing current i_{LM1} is expressed in the following:

$$i_{CF1}(t) = i_{SW1}(t) = i_{SW3}(t) = \frac{\pi P_{\mathrm{in}}}{V_{\mathrm{in}}}\sin(\omega_{\mathrm{res}}(t-t_0)) \tag{12}$$

$$i_{CR1}(t) = i_{CR2}(t) = -\frac{\pi P_{\mathrm{in}}}{V_{\mathrm{in}}}\sin(\omega_{\mathrm{res}}(t-t_0)) \tag{13}$$

$$i_{Lm1}(t) = -\frac{V_{\mathrm{out}}}{L_m}\left(t - t_0 - \frac{1}{4f_{\mathrm{res}}}\right). \tag{14}$$

Combing (7) and (14), the current through devices $S_{\mathrm{R3,4}}$ can be expressed in (15) and the current through device $S_{\mathrm{R7,8}}$ can be expressed in (16)

$$\begin{aligned} i_{SR3,4}(t) &= i_{CF1}(t) + i_{\mathrm{BO}}(t) \\ &= i_{CF1}(t) + ni_{AO}(t) + i_{Lm1}(t) \\ &= \frac{(1+n)\pi P_{\mathrm{in}}}{V_{\mathrm{in}}}\sin(\omega_{\mathrm{res}}(t-t_0)) \\ &\quad - \frac{V_{\mathrm{out}}}{L_m}\left(t - t_0 - \frac{1}{4f_{\mathrm{res}}}\right) \end{aligned} \tag{15}$$

$$i_{SR7,8}(t) = \frac{n\pi P_{\mathrm{in}}}{V_{\mathrm{in}}}\sin(\omega_{\mathrm{res}}(t-t_0)) - \frac{V_{\mathrm{out}}}{L_m}\left(t - t_0 - \frac{1}{4f_{\mathrm{res}}}\right). \tag{16}$$

The dc component of capacitors C_{R1}, C_{F1}, C_{R2} are 2x, 4x, 6x, respectively. As a result, the voltage across C_{R1} is expressed in (17). Similarly, the voltage across C_{R2} is shown in (18). For the nonresonant capacitor C_{F1}, its voltage can be treated as constant since its value is very large, which is equal to $0.5\mathrm{V_{in}}$. The voltage stress of devices S_{R1}, S_{R2}, $S_{\mathrm{R5,}}$ and S_{R6} are expressed in (19). It is easy to find the voltage stress among low-voltage side devices is equal. The voltage stress of the high voltage side devices $\mathrm{S_{w2}}$ and $\mathrm{S_{w4}}$ is $0.5\mathrm{V_{in}}$

$$v_{CR1}(t) = \frac{-\pi P_{\mathrm{in}}}{V_{\mathrm{in}}\omega_{\mathrm{res}}C_R}\cos(\omega_{\mathrm{res}}(t-t_0)) + 0.75V_{\mathrm{in}} \tag{17}$$

$$v_{CR2}(t) = \frac{-\pi P_{\mathrm{in}}}{V_{\mathrm{in}}\omega_{\mathrm{res}}C_R}\cos(\omega_{\mathrm{res}}(t-t_0)) + 0.25V_{\mathrm{in}} \tag{18}$$

$$v_{ds(SR1)}(t) = 0.25V_{\mathrm{in}} + \frac{\pi P_{\mathrm{in}}}{V_{\mathrm{in}}\omega_{\mathrm{res}}C_R}\cos(\omega_{\mathrm{res}}(t-t_0)) \tag{19}$$

$$v_{ds(SW2)}(t) = v_{ds(SW4)}(t) = 0.5V_{\mathrm{in}}. \tag{20}$$

At t_1, the high voltage side devices S_{w1} and S_{w3} are turned OFF and the devices S_{w1} and S_{w3} are charged while the devices S_{w2} and S_{w4} are discharged. Therefore, the ZVS turning ON of the high voltage side devices can be realized. After the diodes of the S_{w2} and S_{w4} are conducted during stage II, the current through winding AO should satisfy (21). The charge $Q_{\mathrm{coss\text{-}H}}$ on the high voltage side devices during turning OFF is expressed in (22). As a result, the dead time can be estimated in (23). Therefore, one-period time T_{PWM} should be expressed in (24)

$$i_{AO}(t_1{\sim}t_2) = i_{OB}(t_1{\sim}t_2) = \frac{-i_{Lm1}(t_1)}{n+1} = \frac{V_{\mathrm{out}}}{4(n+1)f_{\mathrm{res}}L_m} \tag{21}$$

$$Q_{coss-H} = v_{SW2}\,C_{coss-H} = 0.5V_{\mathrm{in}}C_{coss-H} \tag{22}$$

$$T_{\mathrm{dead}} = \frac{2Q_{coss\_H}}{i_{\mathrm{AO}}(t_1)} = 32(n+1)f_{\mathrm{res}}L_mC_{coss-H} \tag{23}$$

$$T_{\mathrm{PWM}} = 2T_{\mathrm{dead}} + \tfrac{1}{f_{\mathrm{res}}} = 64(n+1)f_{\mathrm{res}}L_mC_{coss\_H} + \tfrac{1}{f_{\mathrm{res}}}. \tag{24}$$

For stage III and stage IV, the waveforms are symmetric to stage I and stage II, therefore, the derivation for the rest two stages are not presented here. Moreover, it should be pointed out that the voltage stress of the device S_{W1} is not constant during stage III, and it can be expressed in (25) while the voltage stress of S_{W3} is constant and expressed in (26)

$$v_{ds(SW1)}(t) = 0.25V_{\mathrm{in}} + \frac{\pi P_{\mathrm{in}}}{V_{\mathrm{in}}\omega_{\mathrm{res}}C_R}\cos(\omega_{\mathrm{res}}(t-t_0)) \tag{25}$$

$$v_{ds(SW3)}(t) = v_{CR1}(t) - v_{CR2}(t) = 0.5V_{\mathrm{in}}. \tag{26}$$

V. Converter Design

A. Design of the Resonant and Nonresonant Capacitors C_{R1}–C_{R2} and C_{F1}

According to (10), the current RMS stress of the capacitors C_{R1}, $C_{\mathrm{R2,}}$ and C_{F1} are calculated in (27). Suppose the maximum input power is 500 W and the input voltage is 48 V, then the RMS current through these capacitors is equal to 23.1 A at 500 W. The

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capacitors voltage stress of C_{R1}, C_{F1} and C_{R2} are 36 V, 24 V, 12 V, respectively. Set the resonant frequency as 450 kHz, so the resonant capacitors C_{R1} and C_{R2} should be 1.37 μF according to (28). The nonresonant capacitor C_{F1} should be ten times larger than resonant capacitors, which is calculated to be 13.7 μF in (29)

$$I_{\mathrm{RMS}(C_{R1})} = I_{\mathrm{RMS}(C_{R2})} = I_{\mathrm{RMS}(C_{F1})} = \frac{i_{CR1}(t)_{\mathrm{peak}}}{\sqrt{2}} = \frac{\pi P_{\mathrm{in}}}{\sqrt{2} V_{\mathrm{in}}} \tag{27}$$

$$C_{R1} = C_{R2} = \frac{1}{L_k (2\pi f_{\mathrm{res}})^2} \approx 1.37\mu\mathrm{F} \tag{28}$$

$$C_{F1} \geq 10\, C_{R1} = 13.7\mu\mathrm{F}. \tag{29}$$

Based on the above calculation result, the resonant C_{R1} and C_{R2} adopt the U2J capacitor C1812C145J5JLC7805 (1.4 μF, 50 V) from KEMET corporation. The nonresonant C_{F1} adopts the X7R capacitor CGA9P3X7R1H226M250KB (22 μF, 50 V) from TDK corporation. Its capacitance decreases to 15.7 μF at 24 V, and two capacitors in parallel are used to satisfy (29).

B. Design of the Input Capacitor C_{in}

For the input capacitor C_{in}, ΔV_{in} can be expressed in (30). By setting ΔV_{in} less than 0.5 V, then the input capacitor C_{in} should be larger than 20.4 μF according to the following equation:

$$\Delta V_{\mathrm{in}} \approx \frac{0.55 P_{\mathrm{in}}}{V_{\mathrm{in}} f_{\mathrm{res}} C_{\mathrm{in}}}. \tag{30}$$

The X7S capacitor C5750X7S2A226M280KB (22 μF, 100 V) from TDK corporation is adopted for the input capacitor, and its capacitance decreases to 10 μF at 48 V. Thus, three of the capacitors in parallel are used as input capacitors.

C. Design of the Output Capacitor C_{out}

For the output capacitor C_{out} design, the ΔV_{out} can be expressed in (31). By setting the ΔV_{out} less than 1% of V_{out}, then the output capacitor C_{out} should be larger than 260 μF. The X5R capacitor C4532X5R1A476M280KA (47 μF, 10 V) from TDK corporation is adopted for the output capacitor, and its capacitance decreases to 32 μF at 6 V. Therefore, nine of the capacitors in parallel are used as output capacitors

$$\Delta V_{\mathrm{out}} \approx \frac{0.84 P_{\mathrm{in}}}{V_{\mathrm{in}} f_{\mathrm{res}} C_{\mathrm{out}}}. \tag{31}$$

D. Design of the High Voltage Side Devices

The voltage stress of the high voltage side devices is 24 V, and the RMS current stress of all the devices is the same which is expressed in (32). As a result, the RMS current is 16.4 A at 500 W, and the 40 V rating devices BSZ018N04LS6ATMA1 are used

$$I_{\mathrm{RMS}(SW)} = 1.57 \frac{P_{\mathrm{in}}}{V_{\mathrm{in}}}. \tag{32}$$

VI. Simulation and Experiment Results

A. Simulation Result at Peak Efficiency (160 W)

The simulation of the proposed 8x MASC at 160 W (peak efficiency point) is conducted by PLECS. Fig. 14(a) illustrates the high-voltage side devices' simulation waveforms, and the ZVS turning ON of the high-voltage side devices is verified. Fig. 14(b) shows the simulation waveforms of the low-voltage side devices. Fig. 14(c) shows the flux density waveforms of the matrix autotransformer. The peak flux density through four side cylinders is 0.1 T, while the peak flux density through the center cylinder is 0.06 T. Fig. 14(d) shows the simulation waveforms of the input and output ports. The output voltage ripple is 0.15 V at 160 W. Fig. 14(e) shows the current simulation waveforms of the resonant capacitors and nonresonant capacitors.

B. Experimental Result at Peak Efficiency (160 W)

Fig. 15 presents the prototype of the 8x MASC. The RMS value of the input voltage, input current, and output voltage is measured by the 87 V Fluke digital voltage meter and the experimental efficiency is calculated based on (33). The experimental waveform below is measured by oscilloscope MSO68B-6-BW-6000 from Tektronix corporation. The current of the capacitors C_{R1}–C_{R2} and C_{F1} are measured by CWT Ultra Mini(CWT) Rogowski Current Waveform Transducer from PEM corporation. The labels of the experimental results are all defined in Fig. 11

$$\eta = \frac{V_{\mathrm{out(Fluke)}} \times I_{\mathrm{out(Electrical\ load)}}}{V_{\mathrm{in(Fluke)}} \times I_{\mathrm{in(Fluke)}}}. \tag{33}$$

Fig. 16 shows the voltage waveforms of the low-voltage side devices at 160 W. The voltage stress of the low voltage side devices S_{R1}–S_{R7} should change from 14.7 to 9.3 V according to (25). However, there exists a voltage spike during the transition, and the peak voltage when the devices are turned off is around 17 V, which means 2.3 V voltage overshoot.

Fig. 17 shows the voltage waveforms of the high-voltage side devices at 160 W. The light-yellow, blue, light-red, and light-blue waveforms demonstrate the voltage across the devices $\mathrm{S_{w4}}$, $\mathrm{S_{w3}}$, $\mathrm{S_{w2}}$, and $\mathrm{S_{w1}}$, respectively. The calculated voltage stress of the high voltage side devices S_{W2}–S_{W4} is 4x around 24 V. The calculated voltage stress of the device S_{W1} is around 14.7 V based on (25). The tested voltage stress of S_{W1}–S_{W3} and S_{W4} are 25 V and 14 V, respectively.

Fig. 18 shows the ZVS turning ON operation waveforms of the high voltage side devices S_{W3} and S_{W4} at 160 W. The light red and light-yellow waveforms are the voltage across the devices $\mathrm{S_{W3}}$ and $\mathrm{S_{W4}}$. The light-blue and blue waveforms are the gate driver voltage of the devices $\mathrm{S_{W3}}$ and $\mathrm{S_{W4}}$. The dead time is set as around 100 ns based on (23), and obviously, the devices' voltage decreases to 0 V before the gate driver signal turns ON.

Fig. 19 illustrates the current waveforms of the capacitors C_{R1}–C_{R2} and C_{F1}. The light-yellow, light-red waveforms and blue waveforms are current through the resonant capacitor C_{R1}, C_{R2}, and C_{F1}. The peak to zero current should be 10.79 A based on (12) and (13), which also can be verified by the

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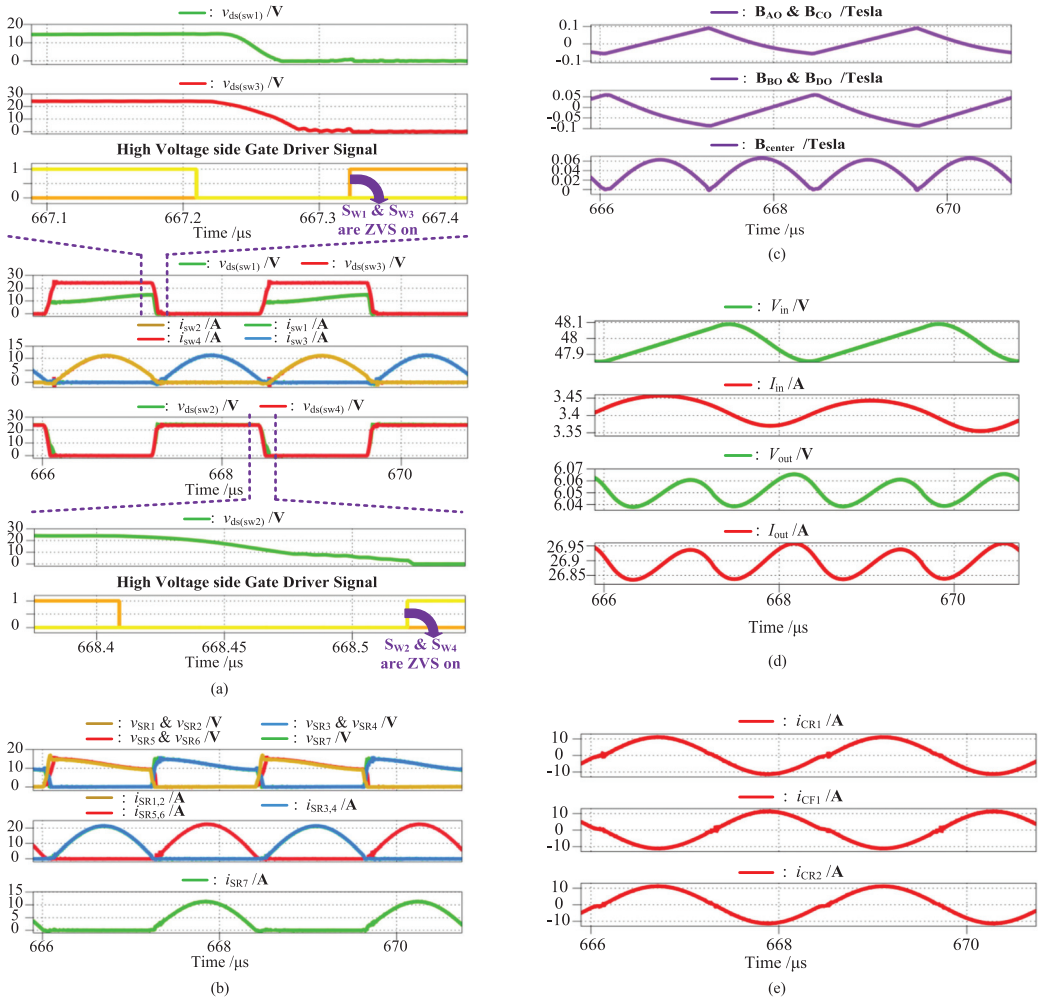

Fig. 14. Simulation waveforms at peak efficiency point (160 W). (a) High voltage side devices' waveforms. (b) Low voltage side devices' waveforms. (c) Waveforms of the matrix autotransformer flux density. (d) Input side and output side waveforms. (e) Waveforms of the capacitor C_{R1}, C_{R2}, and C_{F1}.

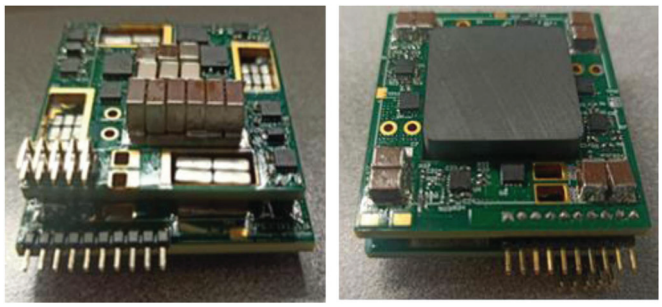

Fig. 15. Prototype of the 8x MASC.

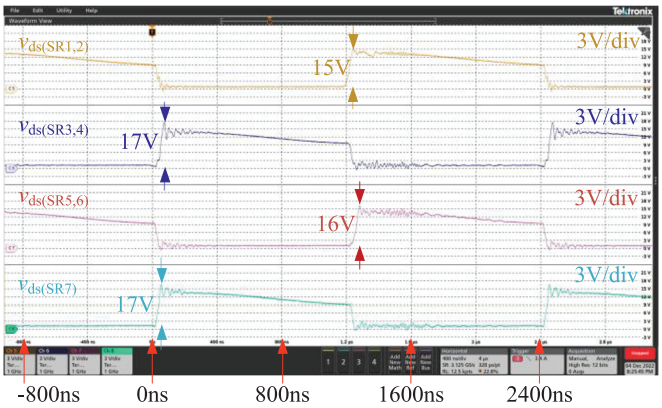

Fig. 16. Voltage waveforms of the low voltage side devices S_{R1}–S_{R7} at 160 W.

experimental result shown in Fig. 19. Fig. 20 shows the voltage and current waveforms of the input and output port at 160 W. The light-yellow waveform is the output current which is 24.4 A. The blue waveform shows the output voltage which is 6.2 V. The light-red waveform shows the input current which is 3.2 A, and the light-blue waveform shows the input voltage which is 48 V.

C. Experimental Result at 460 W

Fig. 21 shows the voltage and current waveforms of the input port and output port at 460 W. The black waveform is the input voltage which is 47.27 V. The light-blue waveform shows the

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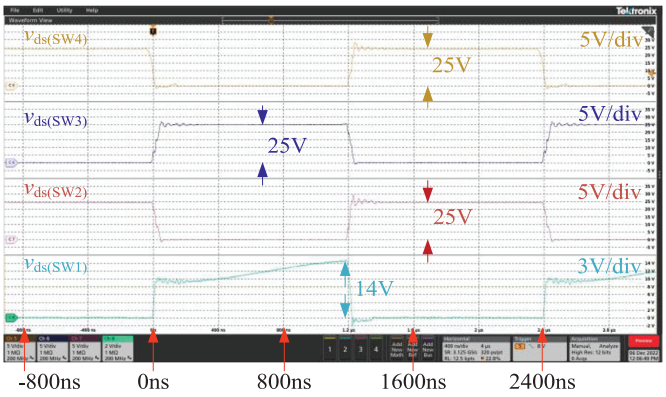

Fig. 17. Voltage waveforms of the high voltage side devices S_{W1}–S_{W4} at 160 W.

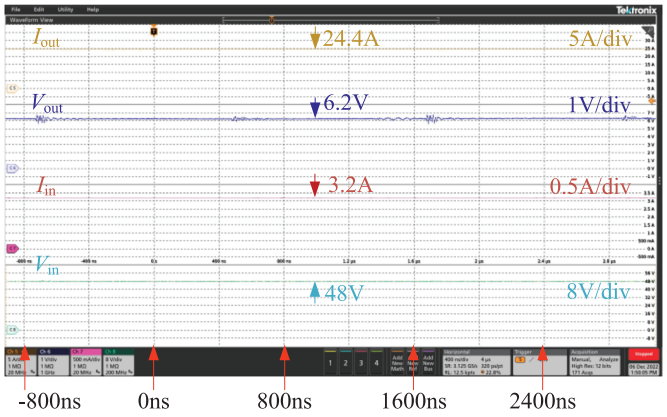

Fig. 20. Voltage and current waveforms of the input and output at 160 W.

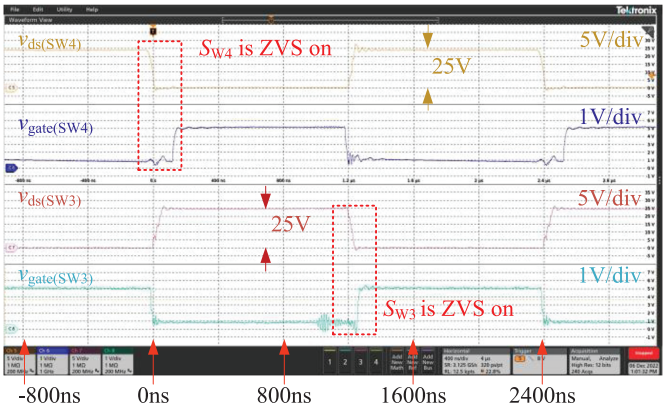

Fig. 18. ZVS soft switching for high voltage side devices at 160 W.

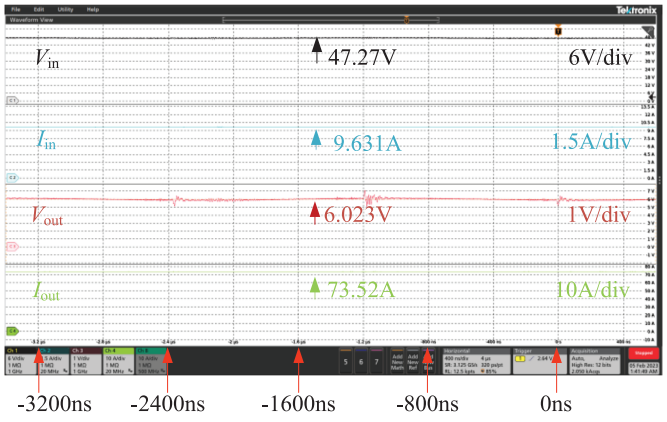

Fig. 21. Voltage and current waveforms of the input and output at 460 W.

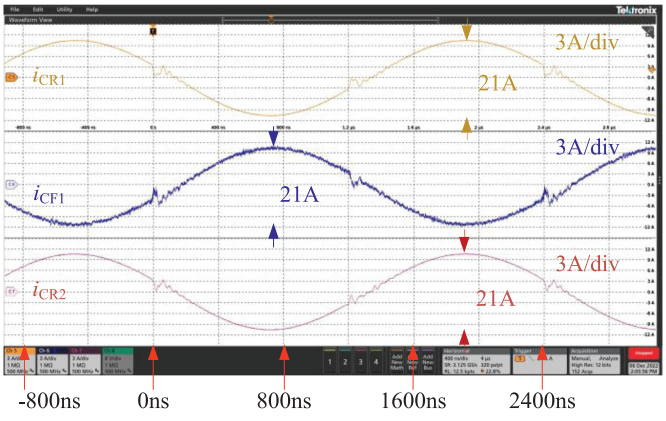

Fig. 19. Current waveforms of the resonant and nonresonant capacitors at 160 W.

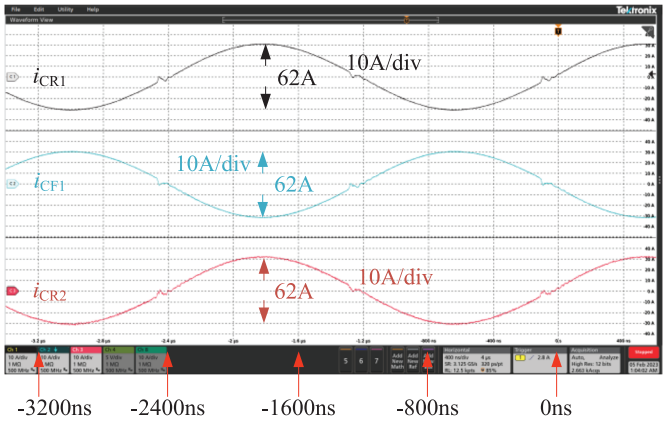

Fig. 22. Current waveforms of the resonant and nonresonant capacitors at 460 W.

input current which is 9.631 A. The light-red waveform shows the output voltage which is 6.023 V, and the green waveform shows the output current which is 73.52 A.

Fig. 22 shows the current waveforms of the capacitors C_{R1}–C_{R2} and C_{F1} at 460 W. The peak to zero current should be 30.1 A based on (12) and (13), but the measured peak to zero current is 31 A due to the dead time zone influence.

D. Power Loss Analysis

The hardware parameters of the prototype are listed in Table II and the power efficiency curve is shown in Fig. 23. The blue triangle is the measured efficiency points from 40 to 460 W without considering the gate driver loss. The maximum measured efficiency is at 460 W due to the limitation of the measurement

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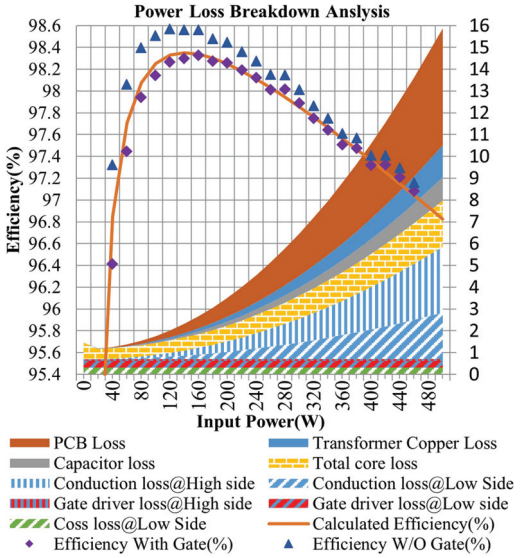

Fig. 23. Power efficiency curve and its breakdown analysis.

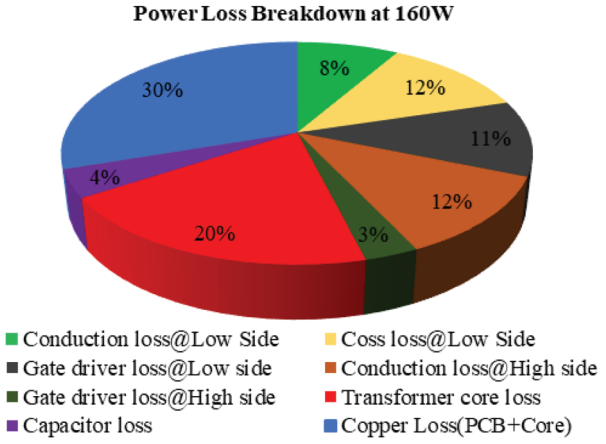

Fig. 24. Power loss breakdown figure at peak efficiency(160 W).

equipment. The maximum efficiency is 98.57% at 160 W, and the efficiency at 460 W is 97.16%. The purple diamond shows the measured efficiency by subtracting the additional estimated gate driver loss. The maximum efficiency is 98.33% at 160 W, and the efficiency is 97.09% at 460 W. The solid orange line draws the estimated efficiency. The right-side *Y*-axis shows the power loss estimation results. When the load is light, the core loss as well as gate driver loss are the dominant part of the whole power loss. However, the conduction loss becomes the dominant part of the whole power loss under heavy load. The power density of the developed prototype is 767.4 W/in^3 assuming 500-W maximum power. The optimization of the prototype component size and height would be considered as future work. The power loss breakdown analysis at the peak efficiency point(160 W) is shown in Fig. 24. The autotransformer's core loss accounts for 20%. The copper loss including the PCB and core windings is around 30%. The power loss contributed by low-voltage side devices is 31%, while the power loss contributed by high-voltage side devices is 15%. The capacitors' loss is 4%. In future papers,

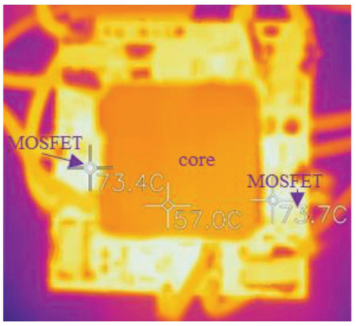

Fig. 25. Temperature distribution of the prototype at 460 W.

a more accurate power loss estimation of the auto-transformer will be built with the finite element analysis software.

Table III shows a detailed comparison between HSC in [53], [54], [55], [56], and [62] and the proposed MASC. Both MASC and HSC can be built in single-phase and two-phase interleaved structures, and some major comparisons are concluded as follows: First, the autotransformer's copper loss is just 33.3% when compared with HSC under the condition that the autotransformer's size is the same. Second, the RMS current through all devices and windings is the same for MASC, which results in the temperature average distribution of the prototype, while the RMS current is different among windings and devices of HSC resulting in nonaverage temperature distribution. Third, the lower voltage stress devices with better performance can be adopted for MASC but the counts are more. Fourth, the counts of resonant/nonresonant capacitors of MASC are more than HSC's. Finally, it is easier to extend the conversion ratio of MASC, i.e., 12x, while difficult for HSC to do so.

Fig. 25 shows the thermal image at 460 W. The magnetic core is on the center of the PCB board, and its temperature is around 57 °C, and the MOSFETS of the low voltage side are around 73.7 °C at steady state.

VII. Conclusion and Future Work

This article proposes a MASC that targets improving the efficiency of the high conversion ratio dc–dc bus converter for 48–6-V data-center applications. A hardware prototype with peak efficiency at 98.33% and power density of 767.4 W/in^2 have been developed. 25-V Si devices with the lowest TSLI are used for the proposed circuit and design, but in the future, if better 12-V devices with lower TSLI become available, a better-performance circuit could be developed using the proposed MASC. The matrix autotransformer without the primary winding is also designed and optimized to integrate all magnetic components into one core for high-efficiency purposes. The ZVS switching of the high-voltage side devices is realized by the magnetizing current within full power range. The ZCS for all the low-voltage side devices can be achieved. Both simulation and experimental results prove the validity of the proposed circuit.

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Fig. 26. Core shape of the integrated matrix auto-transformer.

APPENDIX I
DESIGN OF MAGNETIC CORE

The core shown in Fig. 26 is adopted to merge the resonant inductors and transformers. The material of the customized core is ML95S from Hitachi Metal Corporation. In an isolated LLC converter, a matrix transformer with a similar core shape has been designed in [58] and [59]. It can greatly decrease the termination power loss since the current on the secondary side is averagely distributed on all the side cylinders [45], [51]. In this article, this kind of core is also adopted. The center cylinder works as the resonant inductor and a small partial magnetic flux flows through it, while the side cylinder works as a transformer since a large partial magnetic flux flows through it. The major difference between the proposed integrated matrix transformer design with the traditional LLC matrix transformer is the proposed solution does not have a primary side winding. Therefore, it is possible to save the transformer winding loss using the proposed design. The specific design of the core parameters is shown in Appendix I, and the relationship among the magnetic reluctance, leakage inductance $L_{\rm k}$, magnetizing inductance $L_{\rm m}$ as well as equivalent turn ratio n are derived in this section.

Fig. 27 shows the equivalent magnetic circuit of the integrated matrix autotransformer. According to the working principle of the circuit, the voltage across AO and CO are equal which is labeled as v_1, and the voltage across BO and DO are also equal which is labeled as v_2. The voltage relationship of the four winding ports is expressed in (34). Moreover, the average current through windings AO and CO are the same due to the balance of the charge across the capacitor $C_{\rm R1}$–$C_{\rm R2}$ and $C_{\rm F1}$. So are the same current for BO and DO. As a result, the instantaneous current through AO and CO is equal, and so is the same current through BO and DO which are expressed in (35)

$$\begin{cases} v_{\rm AO}\,(t) = v_{\rm CO}\,(t) = v_1\,(t) \\ v_{\rm BO}\,(t) = v_{\rm DO}\,(t) = v_2\,(t) \end{cases} \tag{34}$$

$$\begin{cases} i_{\rm AO}\,(t) = i_{\rm CO}\,(t) = i_1\,(t) \\ i_{\rm BO}\,(t) = i_{\rm DO}\,(t) = i_2\,(t). \end{cases} \tag{35}$$

Since the voltage among four ports and magnetic reluctance is symmetric, therefore the magnetic flux is also symmetric. The detailed magnetic flux is labeled in Fig. 27 and the relationship among all the magnetic fluxes is expressed in (36)–(38)

$$\Phi_{\rm A} = \Phi_C = 2\Phi_1 + \Phi_{m1} \tag{36}$$

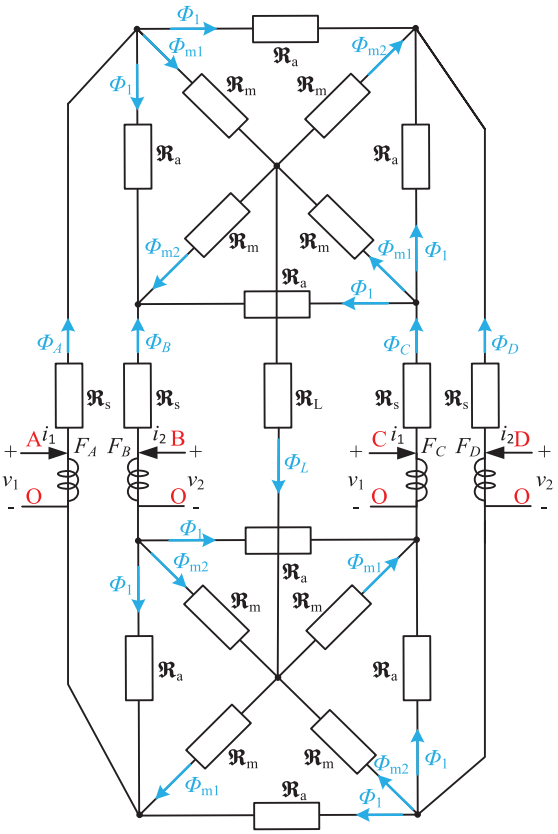

Fig. 27. Equivalent magnetic circuit of the Integrated Transformer.

$$\Phi_B = \Phi_D = -2\Phi_1 - \Phi_{m2} \tag{37}$$

$$\Phi_A + \Phi_B + \Phi_C + \Phi_D = 2\Phi_{m1} - 2\,\Phi_{m2} = \Phi_L. \tag{38}$$

Moreover, the relationship among magnetic flux, magnetic reluctance, and magnetomotive force is shown in (39)–(41)

$$\Phi_{m1}\Re_m + \Phi_{m2}\,\Re_m = \Phi_1\,\Re_a \tag{39}$$

$$F_A - \Phi_A\,\Re_s = F_B - \Phi_B\Re_s + 2\Phi_1\Re_a \tag{40}$$

$$F_A - \Phi_A\,\Re_s = 2\Phi_{m1}\Re_m + \Phi_L\Re_L. \tag{41}$$

By eliminating variables $F_{\rm A}, \Phi_1, \Phi_{m1}, \Phi_{m2}, \Phi_{\rm L}$ in (36)–(41), then the relationship between $F_{\rm B}$, $\Phi_{\rm A}$, $\Phi_{\rm B}$ can be expressed in the following:

$$\Phi_B = \frac{-\left(2\Re_L + \dfrac{4\Re_m}{4 + \dfrac{\Re_a}{\Re_m}}\right)\Phi_A + F_B}{\left(\Re_s + 2\Re_L + 2\Re_m + \dfrac{4\Re_m}{4 + \dfrac{\Re_a}{\Re_m}}\right)}. \tag{42}$$

By eliminating variables $\Phi_{\rm B}$, Φ_1, Φ_{m1}, Φ_{m2}, $\Phi_{\rm L}$ in (36)–(41), then the relationship between $F_{\rm A}$, $F_{\rm B}$, $\Phi_{\rm A}$ are expressed

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in the following:

$$F_A = \frac{\left(\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}+2\Re_L\right)F_B+\left(\frac{2\Re_a}{4+\frac{\Re_a}{\Re_m}}+\Re_s\right)(\Re_s+2\Re_m+4\Re_L)\Phi_A}{\left(\frac{4\Re_m+2\Re_a}{4+\frac{\Re_a}{\Re_m}}+2\Re_L+\Re_s\right)}. \tag{43}$$

Since the $\Re_{\mathrm{L}} >> \Re_{\mathrm{a}}$ and $\Re_{\mathrm{L}} >> \Re_{\mathrm{m}}$ because there exists an air gap in the center cylinder, so the approximate (44) can be derived. The magnetomotive force is expressed in (45)

$$\frac{4\Re_m+2\Re_a}{4+\frac{\Re_a}{\Re_m}}+2\Re_L+\Re_s \approx \Re_s+2\Re_L+2\Re_m+\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}} \tag{44}$$

$$\begin{cases} F_A = F_C = i_1 \\ F_B = F_D = i_2. \end{cases} \tag{45}$$

As a result, (43) can be re-expressed in the following:

$$i_1 \approx \frac{\left(\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}+2\Re_L\right)i_2+\left(\frac{2\Re_a}{4+\frac{\Re_a}{\Re_m}}+\Re_s\right)(\Re_s+2\Re_m+4\Re_L)\int v_1 \mathrm{d}t}{\left(\Re_s+2\Re_L+2\Re_m+\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}\right)}. \tag{46}$$

By differentiating (42), (47) can be derived. According to (46) and (47), The parameters of the transformer's equivalent turn ratio n, magnetizing inductor L_{m}, and leakage inductor L_{k} are expressed in (48)

$$v_2(t) = \frac{-\left(\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}+2\Re_L\right)v_1(t)+\frac{di_2(t)}{dt}}{\left(\Re_s+2\Re_L+2\Re_m+\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}\right)}. \tag{47}$$

The integrated matrix autotransformer equivalent circuit is shown in Fig. 28(a) according to (46) and (47). Symmetrically, the equivalent circuit can be also expressed in Fig. 28(b). Set the initial leakage inductor L_{k} as 100 nH. By optimizing the parameters in Appendix I, the updated equivalent turn ratio, leakage inductance, and magnetizing inductance are 0.907, 91.2 nH, and 1.922 μH, respectively

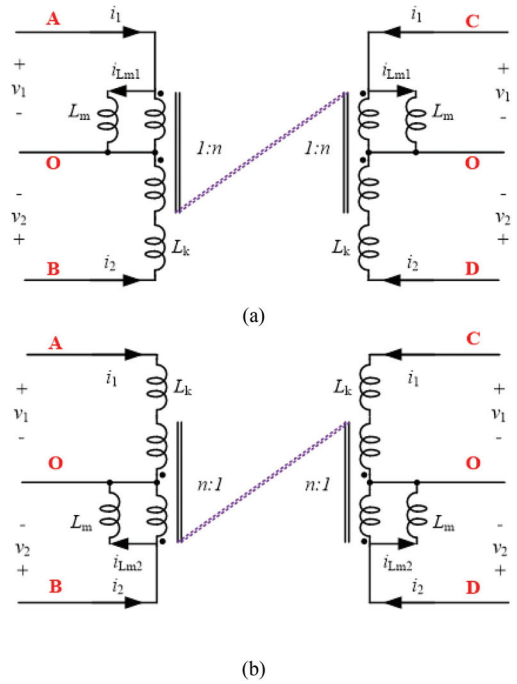

Fig. 28. Integrated autotransformer's model. Both the two models in (a) and (b) are equivalent.

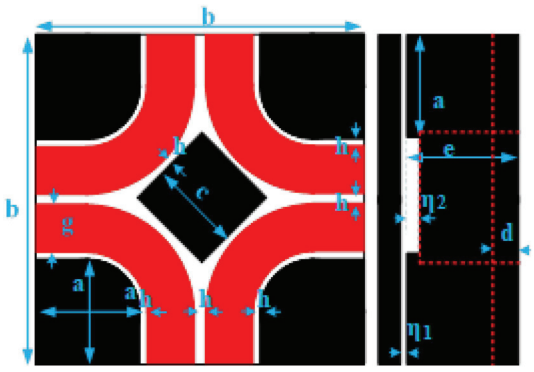

Fig. 29. Core shape with specific parameters.

$$\begin{cases} n = \frac{\left(\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}+2\Re_L\right)}{\left(\Re_s+2\Re_L+2\Re_m+\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}\right)} \\ L_k = \frac{1}{\left(\Re_s+2\Re_L+2\Re_m+\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}\right)} \\ L_m = \frac{\left(\Re_s+2\Re_L+2\Re_m+\frac{4\Re_m}{4+\frac{\Re_a}{\Re_m}}\right)}{\left(\frac{2\Re_a}{4+\frac{\Re_a}{\Re_m}}+\Re_s\right)(\Re_s+2\Re_m+4\Re_L)}. \end{cases} \tag{48}$$

The specific core shape including parameters is shown in Fig. 29. The red arc in the figure is copper, and the black shape is the ferrite core. The core can be divided into three parts which are the top and bottom plane, the center cylinder,

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and the four-side cylinder. VOL_p, VOL_l, VOL_g, and $\mathrm{VOL}_{\mathrm{total}}$ represent the volume of two plane cylinders, center cylinder, and four-side cylinder as well as total transformer volume, and they can be expressed in (49). Moreover, the window area of center cylinder-A_1 and four-side cylinder-A_g are expressed in (50)

$$\begin{cases} \mathrm{VOL_p} = b^2\ d \\ \mathrm{VOL}_l = c^2\ (e-\eta_l) \approx c^2 e \\ \mathrm{VOL}_g = \left(\frac{3}{4}+\frac{\pi}{16}\right)\ a^2 e \\ \mathrm{VOL}_{\mathrm{total}} = b^2\ (e+\eta_g+2d) \approx b^2\ (e+2d) \end{cases} \tag{49}$$

$$\begin{cases} A_l = c^2 \\ A_g = \left(\frac{3}{4}+\frac{\pi}{16}\right)\ a^2 \end{cases}. \tag{50}$$

Since the magnetic reluctance of the center cylinder and the four-side cylinder is far larger than the magnetic reluctance of the top and bottom plane cylinder due to the air gap, so the $\Re_a$ and $\Re_m$ are ignored to simplify the calculation. According to the (48) and set $\Re_a$ and $\Re_m$ as 0, then the relationship between the equivalent transformer model and the magnetic resistance is expressed in (51). By setting L_{k} as 100 nH and L_{m} as 2 μH, then $\Re_g$ and $\Re_L$ can be obtained according to (51)

$$\begin{cases} \Re_g = \frac{1}{L_k} - \sqrt{\frac{L_m - L_k}{L_m (L_k)^2}} = \frac{\eta_l + \eta_g}{\mu_0 A_g} \\ \Re_L = \frac{\frac{1}{L_k} - R_g}{2} = \frac{\eta_g}{\mu_0 A_l}. \end{cases} \tag{51}$$

The maximum magnetic flux of four-side cylinder $B_{\mathrm{g(max)}}$, center cylinder $B_{\mathrm{l(max)}}$, and two planes $B_{\mathrm{p(max)}}$ is expressed in (52). The general core power loss density P_{CV} is expressed in (53). For the material ML95S, $K = 8.604 \times 10^{-8}$, $\alpha = 2.688$, $\beta = 2.22$. Therefore, the total core loss P_{core} is expressed in (54). The copper loss is expressed in (55), where ρ is the resistivity of copper, and m is the thickness of the copper

$$\begin{cases} B_{g(\max)} = \frac{V_{\mathrm{out}}}{4 f A_g} \\ B_{l(\max)} = \frac{2\sqrt{2} L_k' I_{\mathrm{rms}}}{A_l} \\ B_{p(\max)} = \frac{V_{\mathrm{out}}}{8 a d f} \end{cases} \tag{52}$$

$$P_{CV} = K B_{\max}^{\alpha} f^{\beta} \tag{53}$$

$$\begin{aligned} P_{\mathrm{Core}} &= 4P_{CV(g)}\mathrm{VOL}_g + 2P_{CV(P)}\mathrm{VOL}_p + P_{CV(L)}\mathrm{VOL}_l \\ &= \left(3+\frac{\pi}{4}\right)\ a^2 e P_{CV(g)} + 2b^2 d P_{CV(P)} + c^2 e P_{CV(L)} \end{aligned} \tag{54}$$

$$P_{\mathrm{Copper}} = \rho\ \frac{l_{\mathrm{copper}}}{S_{\mathrm{copper}}} = \rho \frac{2\pi\left(\frac{a}{2}+h+\frac{g}{2}\right)+4a}{gm}. \tag{55}$$

Therefore, the total loss of autotransformer can be expressed in (56), and there are seven variables in the equation which are *a, b, c, e, d, g, h.* The thickness of the board is 2.5 mm, and set *h* as 2.5 times of airgap plus board thickness to avoid the fringing effect [51] and *h* is the electrical distance between different nets which is set as 0.2-mm. Moreover, *b, c, e, h* can be expressed by *a, g, d* showed in (57). Therefore, there are three freedoms of degrees—*a, g, d*.

In order to find the best parameters of core size, there are three steps shown as follows: First, fix *d*, i.e., 2.5 mm, and obtain the relationship between the total transformer $\mathrm{VOL}_{\mathrm{total}}$ and total power loss P_{total} with different copper width *g* shown in Fig. 30. Then the minimum power loss curve can be plotted as a red dash curve in Fig. 30

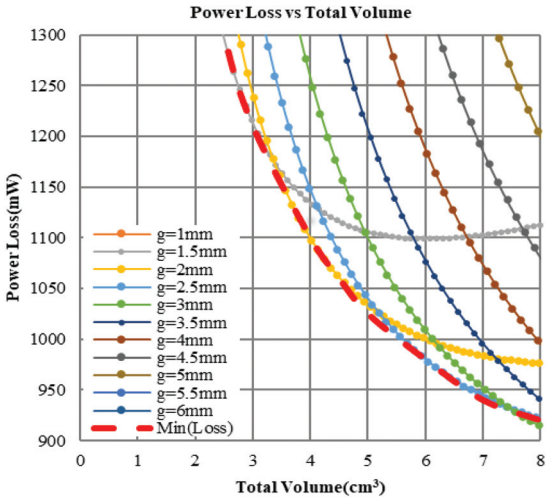

Fig. 30. Relationship between the total transformer power loss and its volume when $d = 2.5$ mm. The minimum power loss curve is shown as red dash.

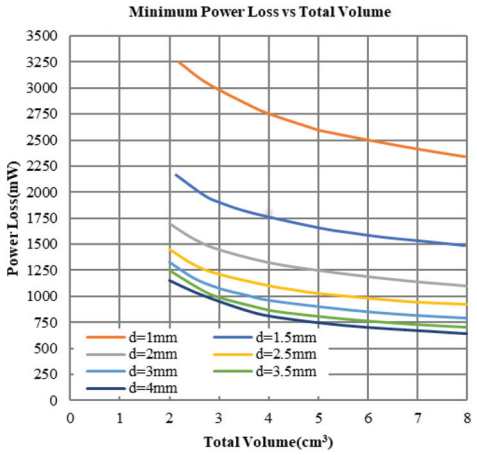

Fig. 31. Relationship between minimum power loss curve and total volume with different *d*.

$$\begin{aligned} P_{\mathrm{total}} &= P_{\mathrm{Core}} + P_{\mathrm{Copper}} \\ &= \left(3+\frac{\pi}{4}\right)\ a^2 e P_{CV(g)} + 2b^2 d P_{CV(P)} \\ &\quad + c^2 e P_{CV(L)} + \rho \frac{2\pi\left(\frac{a}{2}+h+\frac{g}{2}\right)+4a}{gm} \end{aligned} \tag{56}$$

$$\begin{cases} b = 2a + 2g + 3h \\ c = \sqrt{2}\ b - \left(\sqrt{2}a + a + 2g + 4h\right) \\ e = 0.0025 + 2.5\eta_l \\ h = 0.002 \end{cases}. \tag{57}$$

The next step is to sweep the parameter *d* to find a cluster of minimum power loss curves shown in Fig. 31. It can be found that the minimum power loss decreases with the increase of parameter *d*, and *d* is chosen as 3.5 mm according to Fig. 31.

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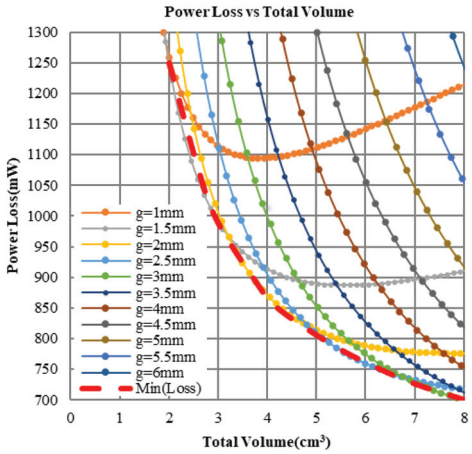

Fig. 32. Relationship between the total transformer power loss and its volume when d=3.5 mm, and the minimum power loss curve is shown in the red dash.

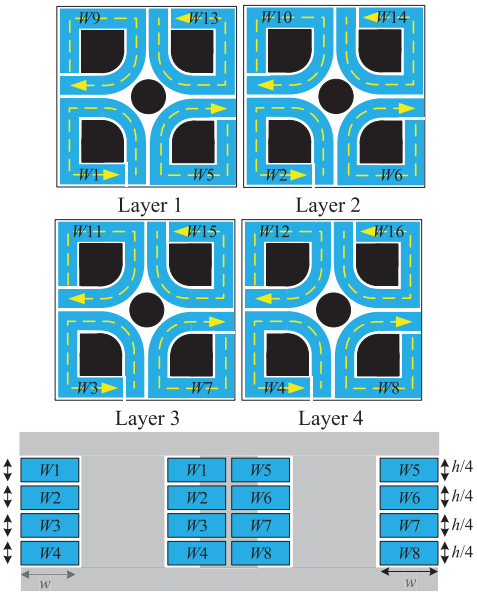

Fig. 33. Magnetic core and its layer distribution for the proposed 8x MASC.

Finally, the relationship between the total volume $\mathrm{VOL}_{\mathrm{total}}$ and total power loss P_{total} with different ring width g when d = 3.5 mm is shown in Fig. 32. The total volume increases when the minimum power loss decreases according to Fig. 32. Select a tradeoff point as $g = 2.5$ mm, $\mathrm{VOL}_{\mathrm{total}} = 4.7\ \mathrm{cm}^3$, and the total power loss is around 810 mW. Therefore, the total transformer size is 21.2 mm × 21.2 mm × 10.5 mm according to (57). Then, by recalculating the inductance when taking $\Re_a$ and $\Re_m$ into consideration, then $L_{\mathrm{K}} = 91.2$ nH, $L_{\mathrm{m}} = 1.922\ \mu$H and n = 0.912.

Appendix II
Comparison of Autotransformer's Copper Loss Between MASC and LLC

Assuming there are four PCB layers for 8x MASC, and the specific layer distribution is shown in Fig. 33. All layers for the proposed 8x MASC in Fig. 33 are identical which are $W1$–$W16$. It should be noticed that the current through proposed 8x MASC's windings $W1$–$W16$ is in full wave rectifier mode, while the current through LLC's secondary side is in half wave rectifier mode. Therefore, the RMS current through 8x MASC's windings is less than the current through LLC's secondary side windings. Assume 8x MASC input voltage, output voltage, total copper height, copper width, power rating, copper resistance, and perimeter for one turn as V_{in}, V_{out}, h, w, P, l, σ, respectively. As a result, $h = 2h_{\mathrm{s}}+2h_{\mathrm{p}}$. Then the RMS current through the windings can be expressed in the following equation:

$$I_{W1} = \ldots = I_{W16} = \frac{P\pi}{4\sqrt{2}V_{\mathrm{in}}}. \tag{58}$$

Therefore, the copper loss for the proposed 8x MASC's autotransformer can be expressed in the following equation:

$$P_{\mathrm{loss\_MASC}} = 16I_{W_1}^2 R_{\mathrm{copper}} = 16 \times \left(\frac{\pi P}{4\sqrt{2}V_{\mathrm{in}}}\right)^2 \frac{\sigma l}{w\,(h/4)} = 2\frac{\sigma l}{wh}\left(\frac{\pi P}{V_{\mathrm{in}}}\right)^2. \tag{59}$$

Assume the LLC converter in [58] has the exact core size and PCB layers, and thickness as the MASC's in this article, and the minimum value of the power loss can be obtained as $11.65\frac{\sigma l}{hw}\left(\frac{\pi P}{V_{\mathrm{in}}}\right)^2$. Therefore, the transformer copper loss of MASC is just 17.1% compared to LLC under the condition that core size, PCB layers, copper thickness, input voltage, output voltage as well as power rating are the same.

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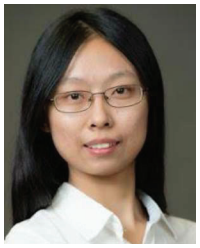

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