500 kW 3-Phase Interleaved SiC Switched Tank Converter for Transportation Electrification

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***Abstract*—Electric vehicles (EVs) draw more attention nowadays since they have now direct vehicle emissions which are harmful to human health and the major source of greenhouse gases. Compared with traditional 400V or 800V EV battery architecture, a 1600V battery system attracts more attention which can use lighter, thinner wiring to charge at unprecedented speeds with less heat. In this paper, a three-phase interleaved switched tank converter is proposed and designed for 800V to 1600V transportation electrification applications. The operation principle is discussed with a detailed analysis and design of the component, including SiC MOSFET loss and thermal analysis, and the passive component is shown in this paper. The 3D structure of the designed prototype is shown in the paper with the double pulse test to validate the gate driver and busbar design. The estimated power density can reach 135 kW/L with an efficiency of 99.3% at 500kW load conditions.**

Keywords— DC-DC converter, switched tank converter (STC), zero-current switching, electric vehicle (EV)

I. INTRODUCTION

Electric vehicles (EVs) draw more attention nowadays since they have now direct vehicle emissions which are harmful to human health and the major source of greenhouse gases. The powertrain of an electric vehicle includes an onboard charger, battery system, bi-directional dc-dc converter, and motor drive system. Compared with traditional 400V or 800V EV battery architecture, a 1.6 kV battery system attracts more attention and can use lighter, thinner wiring to charge at unprecedented speeds with less heat. For example, Atlis is developing the next generation of electric pickup trucks in which the battery will function at 1600 V and it can be charged from zero to 100 percent in 15 minutes[1]. The power rating of charging the EV battery is 1.5 MW. However, the DC bus voltage of the inverter in EV is around 600 ~ 800 V. Therefore, the bi-directional DC-DC converter is needed to step down the battery voltage for the motor drive system.

A conventional bidirectional boost/buck converter has been used for such applications. For example, in [2]–[4], boost based topology bidirectional converter is designed. The interleaved boost converter is proposed in [5]–[7] to achieve higher power density by reducing the input and output capacitor size. Also, flyback bidirectional converter topology is proposed for EV application in [8] and its EMI problem is analyzed in [9]–[12]. To further increase the power density and efficiency of the converter, resonant multilevel converters, resonant switched capacitor converters, and switched tank converters (STC) have been researched by using soft switching. For example, in [13], [14], a 100 kW STC-based topology is proposed and tested for transportation electrification applications. The topology can achieve high voltage, high current, and high conversion ratio by using low voltage and low current devices. By using the STC topology, at 300V to 600 V conversion ratio, the efficiency can achieve 98.7% with 42 kW/L power density.

However, the previous papers mentioned above are still focusing on 300V to 600V voltage ratings. In this paper, a three-phase interleaved STC is proposed and designed for 800V to 1600V transportation electrification applications with high efficiency and high-power density. The operation principle is discussed with a detailed analysis and design of the component, including SiC MOSFET loss and thermal analysis, and the passive component is shown in this paper. Finally, the simulation result and hardware prototype experiment design and verification are presented.

II. CIRCUIT STRUCTURE AND OPERATION PRINCIPLE

In the 3-phase interleaved operation, the control signals of the converter in different phases shift 120-degree for the 3-phase interleaved connection. Fig. 1 shows the connection of the 3-phase interleaved circuit topology.

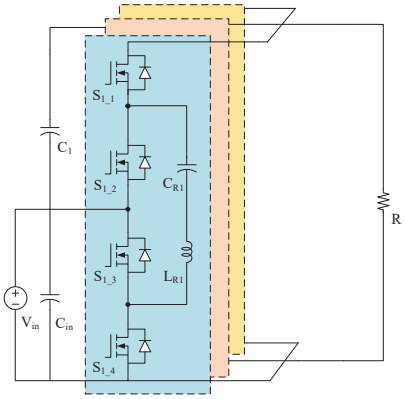


Fig. 1. 3-phase interleaved STC topology

The single-phase STC topology is shown in Fig. 2.

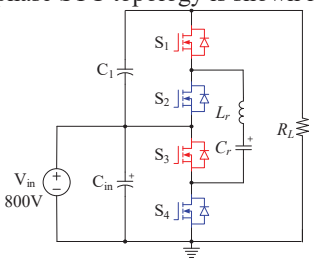


Fig. 2. One-cell STC topology

It is composed of two half-bridge MOSFET, one resonant link, and two clamping capacitors on the half-bridge module. The switch voltage stress and resonant tank capacitor dc bias are equal to low side voltage, which is 800 V in this design. The current stress of each phase is also analyzed.

$$I_s = \begin{cases} I_{s(pk)} * \sin \omega t & 0 \le t \le (\frac{T_s}{2}) \\ 0 & (\frac{T_s}{2}) \le t \le T_s \end{cases} \quad (1)$$

$$I_{s(avg)} = \left(\frac{1}{T_s}\right)\int_0^{\frac{T_s}{2}} I_{s(pk)} * \sin \omega t \, dt = \frac{I_{s(pk)}}{\pi} \quad (2)$$

The relationship between the output current and MOSFET current in the proposed 3-phase interleaved converter is expressed as $I_o = 3 * I_{s(avg)}$.

The two switch mode of the single phase STC is shown in Fig. 3. When S1 and S3 turn on as shown in switching mode 1, the resonant capacitor Cr discharges and resonant inductor Lr releases energy. When S2 and S4 turn on as shown in switching mode 2, the resonant capacitor C_r charges, and the resonant inductor L_r stores energy.

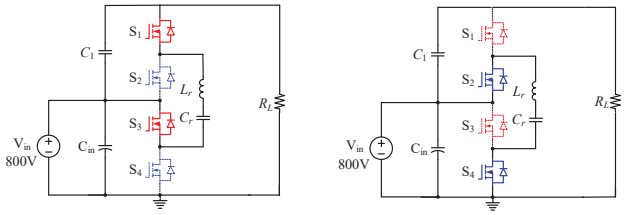


Fig. 3. Equivalent circuit of one cell STC in two switching modes (a) Switching mode 1 (b) Switching mode 2

The ideal operating waveforms of the proposed topology are shown in Fig. 4.

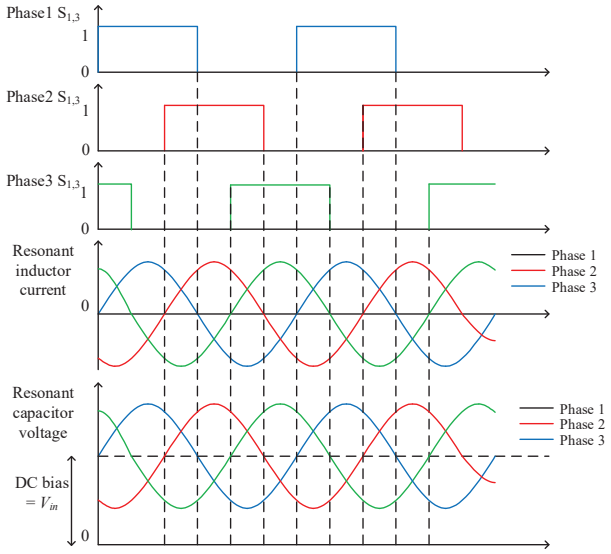


Fig. 4. Theoretical waveforms of the 3-phase interleaved STC

III. Design of Device and Passive Components

The detailed component selection and design are presented in this section. Firstly, the selection of the MOSFET module is discussed and the corresponding heatsink selection is presented. Secondly, the high current high-frequency resonant capacitor and inductor design is presented in this section considering the minimization of resonant link component size and power loss. Finally, the dc link capacitor design is also discussed in this section.

A. Design of switching device

The major challenges for the switch device design in high-power applications are caused by switch device power loss and corresponding temperature rise. Therefore, a detailed SiC switch model is built for analysis when the 3-phase interleaved converter operates at zero-current switching (ZCS) conditions. The switching loss is only caused by the discharge of output capacitance C_{oss} during turn-on transient. The SiC MOSFET conduction and switching loss in 3-phase interleaved STC is represented in (3) and (4):

$$P_{cond} = I_{rms}^2 * R_{DSon} \quad (3)$$

$$P_{sw} = \frac{1}{2} * C_{oss} * V_{DS}^2 * f \quad (4)$$

where I_{rms} is the root mean square (RMS) current of the MOSFET; R_{DSon} is the internal equivalent resistance of the MOSFET; E_{oss} is the output capacitance stored energy at 800V input voltage; f is the MOSFET switching frequency. The switching frequency is chosen as 100kHZ in this 3-phase interleaved STC design. MOSFET loss and efficiency comparison result at different load conditions is shown in Fig. 5 and Fig. 6. Therefore, in this design, FF6MR12W2M1_B70 from Infineon is chosen as the switch device.

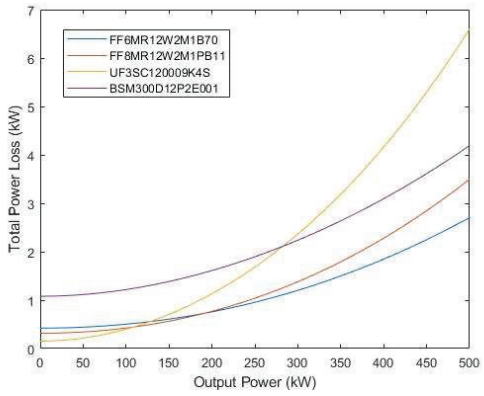


Fig. 5. Total MOSFET power loss comparison

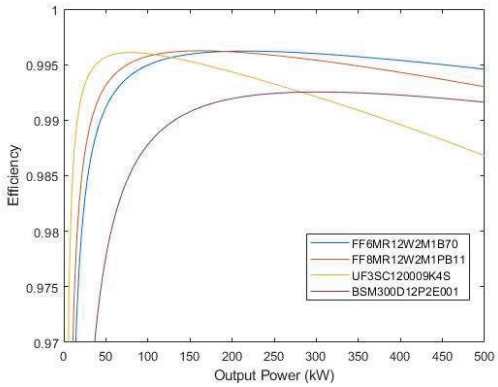


Fig. 6 Total MOSFET efficiency comparison

B. Design of Heatsink

The heatsink design is based on the thermal resistance circuit as shown in Fig. 7.

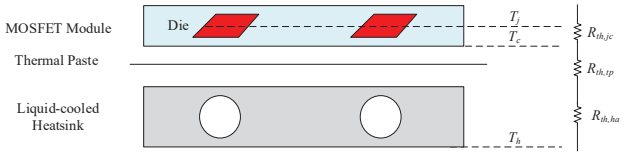


Fig. 7. Thermal model of the MOSFET

The temperature rise of the MOSFET junction is calculated as:

$$T_j = (R_{th,jc}+R_{th,tp}) * P_{loss} + R_{th,ha} * P_{loss} * 3 \quad (5)$$

$$T_c = T_a + R_{th,ha} * P_{loss} * 6 \quad (6)$$

T_j, T_c and T_h are the temperature of the SiC MOSFET junction, MOSFET module case, and ambient, respectively. P_{loss} is the loss of per switch module, $R_{th,jc}$, $R_{th,tp}$ and $R_{th,ha}$ are the thermal resistance of the power module, thermal paste, and heatsink, respectively. In this design, the switch module's thermal resistance $R_{th,jc} = 0.192$ °C/W, thermal paste thermal resistance $R_{th,tp} = 0.003$ °C/W for each module. The maximum junction temperature for the selected SiC module is 175 °C for each module.

The total device loss is 3156 W based on the previous MOSFET loss calculation. The ambient temperature is designed as 25 °C. Therefore, the maximum designed heatsink thermal resistance $R_{th,ha}$ is 0.009 °C/W. An off-the-shelf water cooling heatsink ATS-CP-1001-DIY from Advanced Thermal Solutions has been selected considering heatsink temperature and size constrain. With a 4 L/min water flow rate, the thermal resistance is around 0.007 °C/W. Fig. 8 shows the relationship between MOSFET junction temperature and different load conditions. If considering the real cooling system in hybrid electric vehicles in which the water tank outlet temperature is 85 °C, the maximum output power is 400 kW.

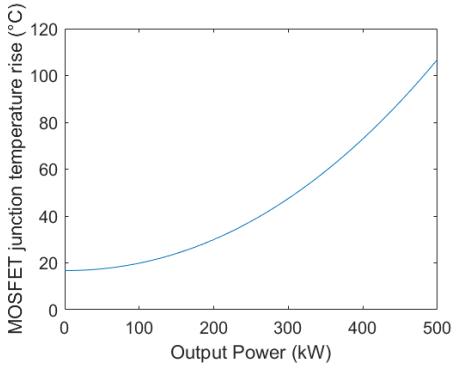


Fig. 8. Thermal performance of selected MOSFET

C. Design of Resonant Capacitor

The challenges of high-power resonant capacitor design are high frequency and high RMS current. Therefore, both ceramic and film capacitors are considered in this design.

The polypropylene capacitors from Illinois Capacitor provide specifically designed high-current, high-frequency resonant capacitors for the high-power resonant capacitor application. However, the power density of film capacitors is lower compared with ceramic capacitors assuming the same capacitance and current rating. Considering the average resonant capacitor voltage is 800V, so 1.1 kV voltage rating capacitor is compared in this section. The film capacitors LC5 and HC5 from Illinois Capacitor, and ceramic capacitors from TDK and KEMET are compared for capacitance density is compared in Table 1.

Table 1: Capacitance density comparison

Series	Capacitance (μF)	Volume (L)	Capacitance density (uF/L)
LC5	1.2	0.54	2.22
HC5	1.2	0.34	3.49
TDK Ceralink	0.75	0.00061	1237.50
Kemet KC-link	0.14	0.00097	144.84

Besides, not only the volume of the resonant capacitors needs to be considered, but also the higher capacitance is preferred in the high-power converter resonant link design.

The reason for higher capacitance preference is for a certain resonant frequency, the smaller inductance value can be used in the design. The relationship between required inductance and total resonant capacitance is shown in Fig. 9.

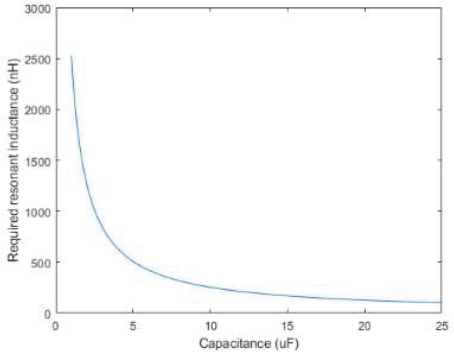


Fig. 9. Required inductance at 100 kHz resonant frequency

Because of the capacitance density and capacitance value, the TDK Ceralink capacitor has been chosen as the resonant capacitor. In this design, 24 capacitors are connected in parallel to increase the current rating. The total capacitance is 18 μF and the total rated current is 264 A. Multilayer copper PCB board ac busbar is designed for this high current high-frequency capacitor board. This arrangement can help to reduce the ac loss caused by the skin effect by uniformly distributing the current through multiple layers. The skin effect is calculated as:

$$\delta = \sqrt{\rho/(\pi f \mu)} \tag{7}$$

where f is the ac frequency. The copper resistivity ρ and permeability μ are $1.76*10^{-8}$ Ω*m, and $1.257*10^{-6}$ H/m, respectively. At 100 kHz, the skin depth is calculated as 0.211 mm. Therefore, a 6-layer PCB board has been designed with 4 oz copper on each layer for the resonant capacitor board.

D. Design of Resonant Inductor

With the above 18 μF resonant capacitance value, to achieve a 100 kHz resonant frequency, the resonant inductance value is required to be 140 nH. The inductor design method includes analytical method[15], experimental method[16], [17], and machine learning-based method [18]. For high power high-frequency inductor evaluation, the design consideration includes not only efficiency and volume but also inductor core thermal performance. For the 3-phase interleaved STC resonant inductor, the peak current is 1/3 times compared with the 1-phase STC at the same input voltage and power rating. Therefore, the size and power of the magnetic component size can also be decreased in the interleaved structure. The winding design and core design will be conducted in this section.

1) Winding design

The copper losses are induced not only by the DC resistance of the winding but also ac resistance by the skin and proximity effects due to the high-frequency current excitations. The litz type of conductor is implemented to reduce the ac loss by winding multiple strands in parallel.

In this design, AWG 14 litz wire from Remington Industries is adopted which is constructed with 260 strands of 38 AWG magnetic wire. 13 pairs of selected litz wire are connected in parallel to satisfy the current requirements of resonant link.

2) Core design

The core losses of the resonant inductor are caused by the alternating in the magnetic core. For such high-frequency inductors, ferrite material is preferred for its low power loss density. The core loss and temperature rise are analyzed in the core selection. The tradeoff between core temperature rises and volume is analyzed.

For the ferrite material comparison, ferrite materials from Magnetics and Ferroxcube are selected. The core loss density equation of the selected core material is given as follows:

$$P_V = a * \left(B_{pk}\right)^b * (f)^c \tag{8}$$

where P_V is the core loss density with the unit of mW/cm^3. B_{pk} is the peak flux density of the inductor core. f is the inductor's resonant frequency. The core loss density comparison result is compared in Fig. 10.

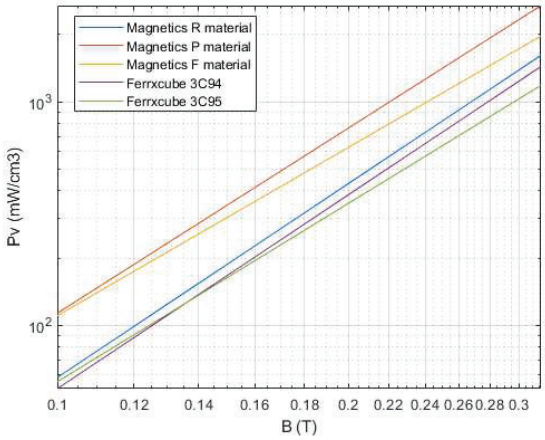


Fig. 10. Core loss density comparison at 100 kHz among different material

E-shaped cores are selected in this project considering the geometry of the converter. Fig. 11 (a) shows the typical E-core dimension. Fig. 11 (b) shows the resonant inductor magnetic path.

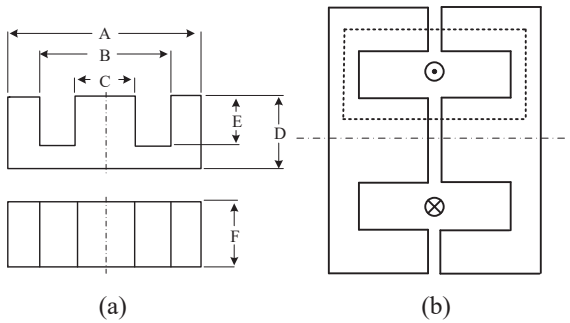


Fig. 11. Resonant inductor core design (a) E core geometry (b) magnetic path of the designed inductor

Resonant inductor core cross-section area A_e and air gap length l_g need to be designed based on the required inductance value, which is calculated as:

$$L = N^2 * A_e/(\frac{l_g}{\mu_0} + \frac{l_e}{\mu_c}) \quad (9)$$

where N is the turns ratio; A_e is cross section area which equal to $\frac{A-B}{2} * F$; l_g is the airgap length; μ_0 and μ_c are permeabilities of the free space and core, respectively; l_e is the equivalent magnetic path length.

According to Faraday's law, the flux density swing ΔB is calculated as:

$$\Delta B = \left| \left[\int_{\frac{T_S}{4}}^{\frac{3T_S}{4}} L di_L(t) \right] /(N * A_e) \right| \quad (10)$$

The peak resonant current of the resonant inductor is $\pi/3$ times the average output current. Therefore, ΔB is calculated as:

$$\Delta B = (L * 2I_o * \frac{\pi}{3})/(N * A_e) \quad (11)$$

$$B_{pk} = \Delta B/2 \quad (12)$$

Resonant inductor core loss and temperature rise can be calculated as:

$$P_{core} = P_V * V \quad (13)$$

$$\Delta T_{core} = \left(\frac{P_{core}}{A_{surface}}\right)^{0.833} \quad (14)$$

where ΔT_{core} is the inductor core temperature rise with the unit of °C.

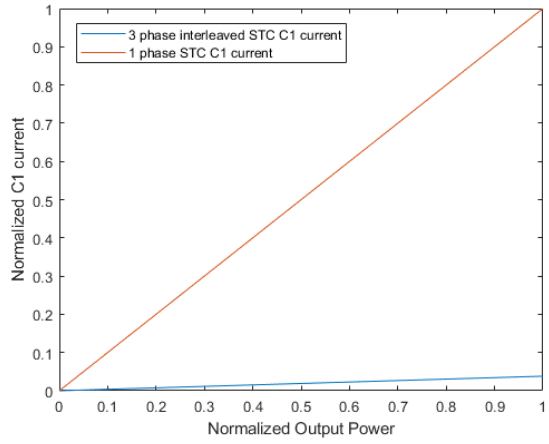
Considering both the geometry constraint and inductor core loss, the geometry of the E55/28/21 inductor core is selected. At the given core geometry, ΔB is calculated as 260 mT. At such ΔB value, Ferroxcube 3C94 has the lowest core loss density value. The total calculated core loss is 5.4 W and the corresponding temperature rise is 43 °C.

E. Design of DC link capacitor

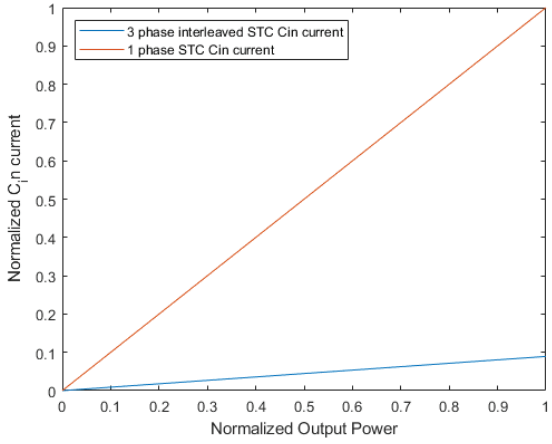
The challenge of DC link capacitor design is the high RMS current. However, compared with single-phase STC, the DC link capacitor RMS current of 3-phase interleaved STC can decrease dramatically. Fig. 12 shows the normalized capacitor RMS current comparison between 1-phase STC and 3-phase interleaved STC, which proves that the size of the input capacitor can be reduced significantly when using 3-phase interleaved design as shown in this paper. At full load conditions, the input capacitor RMS current is 10 A, and the output capacitor RMS current is 15 A.

In ZCS mode, the 3-phase interleaved operation allows the current stress of the input capacitor C_{in} drops from 402 A to 14.25 A, which is 28 times lower. And the current stress of the output capacitor C_1 is reduced by 12 times, from 147 A to 12.5 A.

Therefore, in this design, a film capacitor from KEMET has been chosen. The capacitance value is 24 µF each and 4 capacitors are connected in parallel. The RMS current rating for each capacitor is 19.5 A. Therefore, the total current rating for the input and output capacitors is 78 A.



(a)



(b)

Fig. 12. Normalized current stress of DC link capacitors (a)

F. Summary

In summary, the design specifications of the proposed 3-phase interleaved STC is summarized in Table 2.

Parameter	Value
Input voltage	800 V
Output voltage	1600 V
Rated power	500 kW
Switching frequency	100 kHz
Resonant inductor value	140 nH
Resonant capacitor value	18 µF
DC link capacitor value	100 µF

IV. Simulation and Experimental Result

A 500kW 800V-1600V 3-phase interleaved STC at ZCS mode has been simulated in PLECS and the simulation result is shown in Fig. 13.

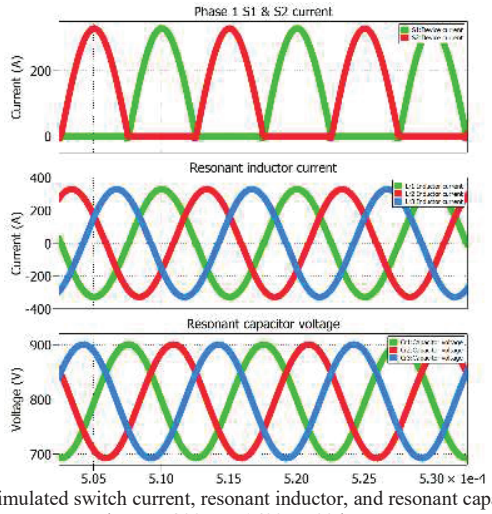


Fig. 13. Simulated switch current, resonant inductor, and resonant capacitor voltage at 800V to 1600V 500 kW

The 3D structure of the proposed 3-phase interleaved STC is shown in Fig. 14. The control is realized through Xilinx Zynq 7000 SoC FPGA. The specification of the prototype is shown in Table 3.

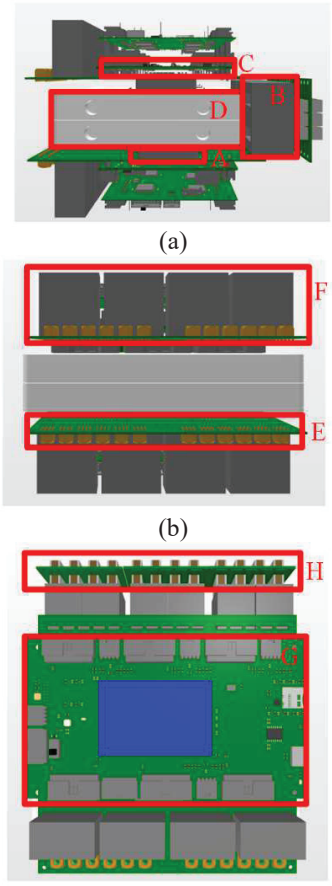


Fig. 14. 3D structure of designed 3-phase interleaved STC (a) side view (b) front view (c) top view

Table 3: Prototype specification

Tag	Component
A	Infineon FF6MR12W2M1_B70 SiC MOSFET module
B	Resonant inductor
C	Gate driver
D	Liquid-cooled heatsink
E	Mainboard busbar
F	DC link capacitor
G	FPGA-based control board
H	Resonant capacitor

With a double-side cooling layout, the dimension of the converter is 100mm*185mm*200mm. Therefore, the estimated power density could reach 135 kW/L with an efficiency of 99.3% at full load conditions.

Fig. 15. Vertical structure of gate driver board design

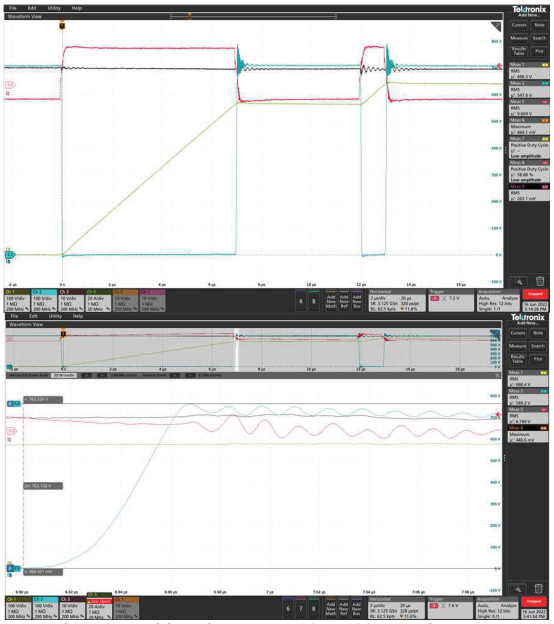


Fig. 16. Double pulse test at 700V, 130 A peak current

A vertical structure of the gate driver board has been designed to minimize the stray inductance and increase the system power density by implementing a compact design geometry. The hardware implementation of the converter is shown in Fig. 15. The gate driver board and main board busbar have been validated through the double pulse test (DPT). DPT result has been shown in Fig. 16. The peak surge voltage is 763V at 700 V DC link voltage and 130A peak current conditions.

A more comprehensive prototype testing result will be presented in the following paper.

V. Conclusion and Future Work

In this paper, a three-phase interleaved converter is proposed and designed for 800V to 1600V transportation electrification applications. Three-phase interleaved switched tank converter topology is proposed and zero current switching (ZCS) operation mode is studied. SiC MOSFET switch loss model is analyzed under ZCS conditions and a liquid-cooled heatsink is designed based on the switch loss analysis. A detailed design and optimization of the resonant inductor, resonant capacitor and DC link capacitor is also fully investigated. Simulation results are provided to show the ZCS operation mode. The double pulse test result shows the effectiveness of the gate driver circuit to minimize the surge voltage. The estimated power density could reach 135 kW/L with an efficiency of 99.3% at full load conditions.

In the future, the converter will be tested under full load conditions.

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