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Analysis and Design of High-Efficiency Modular Multilevel Resonant DC-DC Converter

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ABSTRACT This paper demonstrates a high-efficiency modular multilevel resonant DC-DC converter (MMRC) with zero-voltage switching (ZVS) capability. In order to minimize the conduction loss in the converter, optimizing the root-mean-square (RMS) current flowing through switching devices is considered an effective approach. The analysis of circuit configuration and operating principle show that the RMS value of the current flowing through switching devices is closely related to the factors such as the resonant tank parameters, switching frequency, converter output voltage and current, etc. A quantitative analysis that considers all these factors has been performed to evaluate the RMS current of all the components in the circuit. When the circuit parameters are carefully designed, the switch current waveform can be close to the square waveform, which has a low RMS value and results in low conduction loss. And a design example based on the theoretical analysis is presented to show the design procedures of the presented converter. A 600 W 48 V-to-12 V prototype is built with the parameters obtained from the design example section. Simulation and experiments have been performed to verify the high-efficiency feature of the designed converter. The measured converter peak efficiency reaches 99.55% when it operates at 200 kHz. And its power density can be as high as 795 W/in^3.

INDEX TERMS Modular, multilevel, resonant, resonant DC-DC converter, switched-capacitor, zero-voltage switching (ZVS).

I. INTRODUCTION

DC-DC power converters are widely used all over the world and cover a lot of essential applications. On the one hand, high-power DC-DC converters have been used in photovoltaic (PV) applications [1], [2], [3], [4] to interface the PV arrays with high voltage DC-Link. In electric vehicle (EV) applications, a boost converter is usually used to step up the low battery voltage to high DC-Link voltage [5], [6], [7]. On the other hand, low-power DC-DC converters are used in applications such as DC motor drive and intermediate bus converters (IBC) [8], [9], [10], [11], [12]. With the rapid development of DC-DC power conversion technology, conventional inductor-based switching mode power supplies (SMPS) can no longer meet the high efficiency and high power density requirement of the market. In order to improve the performance of the DC-DC converters, wide bandgap devices are widely used to replace traditional silicon devices because they have better thermal performance, reliability, and lower switching loss than conventional semiconductor devices [13], [14], [15]. Because the inductor-based topologies rely heavily on magnetic components to achieve their functions, there are no optimal solutions to solve the problem that the magnetic components are bulky and heavy. This means the fundamental issues of the traditional inductor-based converters cannot be solved.

Switched-capacitor converters are famous for their magnetic-less feature. The capacitors are used in the circuits to transfer energy as well as achieve voltage conversion functions. Because the capacitors have much higher energy density than inductors [16], the switched-capacitor converters have great potential to surpass the traditional inductor-based

converters in terms of power density and weight [17]. Therefore, switched-capacitor converters are widely used in different applications.

The traditional switched-capacitor concept has been widely used in low-power applications, such as charge pump circuits. And intensive research efforts have been conducted to apply the conventional switched-capacitor concept to medium and high-power applications during the past decades [18], [19], [20], [21]. In these circuits, the capacitors directly charge/discharge each other to transfer the energy. Although the power density of the switched-capacitor converters is increased when compared with inductor-based converters, they still suffer from low efficiency and severe electromagnetic interference (EMI) issues. In order to solve the low-efficiency issue, increasing switching frequency and capacitor capacitance turn out to be very effective solutions [22]. However, the increasing capacitance will lead to a large passive component volume, which is against the essential concept of switched-capacitor converters. Therefore, the resonant switched-capacitor concept has been applied to the switched-capacitor circuits to provide better converter performance. With the resonant operation, the switched-capacitor can achieve soft-switching, which significantly alleviates the generation of EMI and semiconductor switching loss. Most importantly, the volume of passive components can be minimized. As a result, high power density and high efficiency can be achieved. In low power areas, the converters based on the resonant switched-capacitor concept have fully integrated features [23], [24] and therefore have a very small form factor [25], [26], [27], [28], [29], [30], [31]. At medium and high power levels, utilizing stray inductance to achieve soft-switching was proposed to eliminate magnetic components [32], [33], [34]. Besides, tiny planar inductors and surface mount inductors are used to provide superior circuit integration [11], [35].

The switched-tank concept [10], [36] is one very good example of using the resonant switched-capacitor concept to achieve a small form factor as well as soft-switching of a switched-capacitor converter. The switched-tank converter (STC) shown in Fig. 2 is derived from the modular multilevel resonant DC-DC converter (MMRC) shown in [37]. And the zero-current switching (ZCS) operation and design methodology of STC has been fully investigated in [35]. In the STC, analysis shows that the MOSFET C_{oss} loss and conduction loss are two of the major contributors to the total power loss because of its ZCS operation characteristic. Minimizing these two types of loss will help improve efficiency. Therefore, the presented converter that is capable of ZVS operation is studied in this work.

This paper is an extension work of the conference paper [37]. We proposed an MMRC with ZVS capability with reduced RMS current of the switching devices. By analyzing the circuit's operating principle, a mathematical model that can predict all the devices' current waveforms has been developed. The design procedure of a 600 W prototype with 48 V input and 12 V output for data center application is demonstrated. Simulations and experiments have been carried out to validate the developed mathematical model and ZVS operation. The measured peak efficiency of the laboratory prototype reaches 99.35%. And its power density achieves 795 W/in^3.

This paper is organized as follows: Section II demonstrates the circuit configuration and the converter's ZVS operation mode. This section also explains the voltage stress of components in the converter. Section III clarifies how to get the current waveforms of the switching devices, and provides a mathematical method to calculate the RMS value of the current flowing through all the devices. Section IV provides analysis and design of a 48 V–12 V converter base on the information obtained from Section III. Section V presents the simulation and experimental results of the designed converter. Multiple operating points are measured to validate the correctness of the presented analysis and design methodology. ZVS operation is validated in this section as well. At last, Section VI concludes this paper.

II. CIRCUIT CONFIGURATION AND OPERATION OF THE PROPOSED CONVERTER

In this section, the circuit structure of the analyzed converter will be introduced first. Then, the operation of the converter will be demonstrated, which includes the ZVS implementation. And voltage stress of all the components is analyzed. It is worth mentioning that the presented circuit structure can be also used for high-power applications, which is similar to the high-power converter based on the switched-tank concept [38].

A. CIRCUIT CONFIGURATION AND THE OPERATION STATES OF THE ANALYZED CONVERTER

Fig. 1 shows the generalized circuit structure of the analyzed converter. This architecture can be divided into two parts. Switching devices in the first part are named wing side devices. It includes all the switches that are floating in reference to the ground. The other switches in the half-bridges that are connected to the ground or the output directly are called rectifier side devices. They work as synchronous rectifiers in the circuit, which comprise the second part. Fig. 3 shows a converter with a four times voltage conversion ratio based on the presented circuit structure. It is composed of 10 switching devices: 6 devices on the rectifier side, and 4 devices on the wing side.

With different control methods, the presented circuit structure can operate at two operation modes, which are ZCS mode and ZVS mode. The converter design and optimization method for ZCS operation is accomplished in [35], [36], [39], [40]. This paper focuses on analyzing and designing the converter that is operating in ZVS mode. Note that the switches that have the same color on the wing side turn on and turn off at the same time, and so do the switches on the rectifier side. Fig. 4 shows the four switching states of the analyzed converter. The four switching states can be classified into two groups, which are two phase-shift states and two non-phase-shift states. When the switches that have the same color on

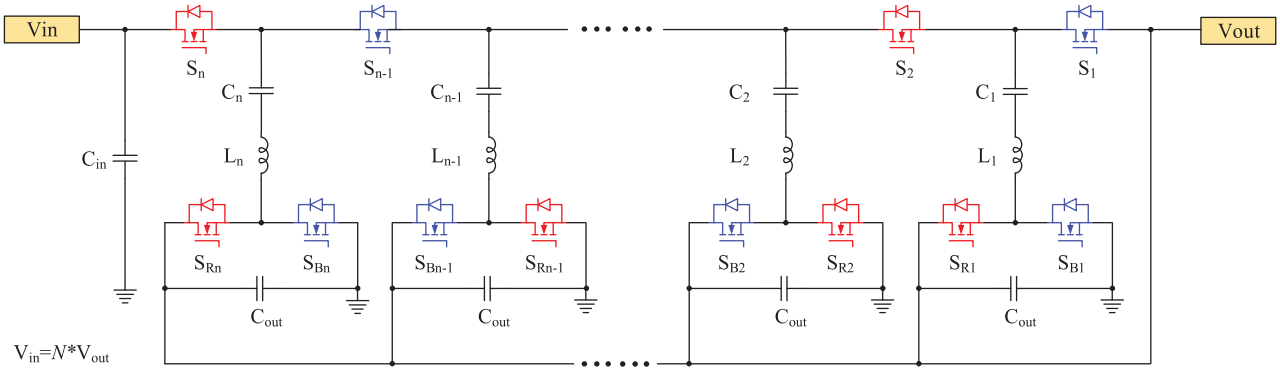

FIGURE 1. System level configuration of the proposed converter.

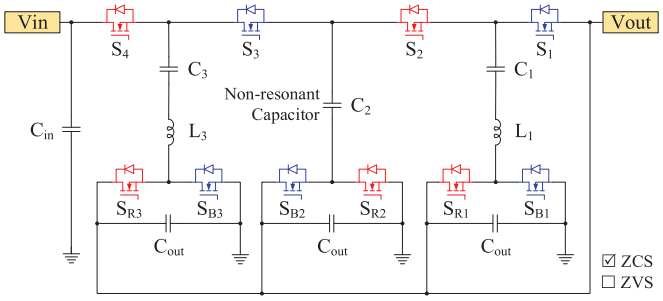

FIGURE 2. State-of-the-art the 4:1 switched-tank converter [35], [36].

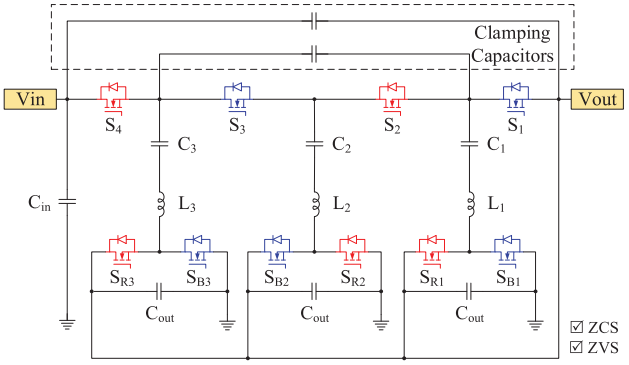

FIGURE 3. The proposed converter with 4:1 voltage conversion ratio.

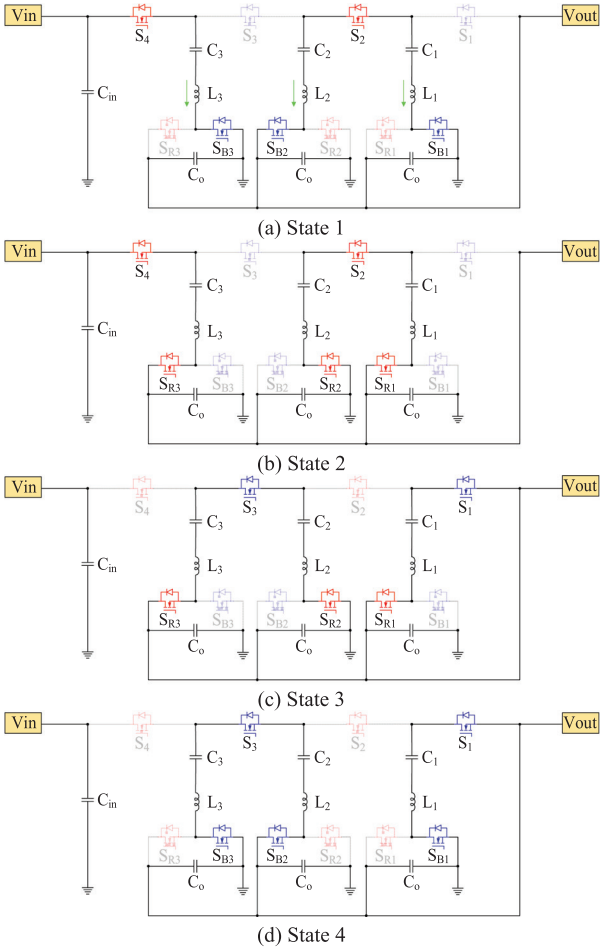

FIGURE 4. Operating states of the presented converter.

the wing side and rectifier side are conducting simultaneously, as shown in Fig. 4(b) and Fig. 4(d), the two switching states are non-phase-shift states. On the other hand, Fig. 4(a) and Fig. 4(c) show the two phase-shift states.

According to the volt-second balanced condition on all the resonant inductors, one can easily tell the average voltage values across the capacitors. In the generalized circuit shown in Fig. 1, which is a converter with N times conversion ratio, the DC voltage bias on capacitor C_n is n times the voltage of the output voltage, which means $V_{Cn} = n*V_{out}$. With the capacitors' voltage information, we can calculate switching devices' voltage stress. For the devices that are located on the wing side, the voltage across devices $S_2 \sim S_{n-1}$ is two times the output voltage, which is $2V_{out}$. While the other wing side devices have voltage stress of V_{out}. For the devices that are located on the rectifier, their voltage stress is V_{out}. To be specific, in Fig. 3, the average voltage values of C_3, C_2, and C_1 are $3V_{out}$, $2\ V_{out}$ and V_{out}, respectively. As a result, we can derive the voltage stress of S_4, S_1 and all the rectifier side devices is the same as the output voltage V_{out}. And switch S_2, S_3 have a voltage stress of $2V_{out}$.

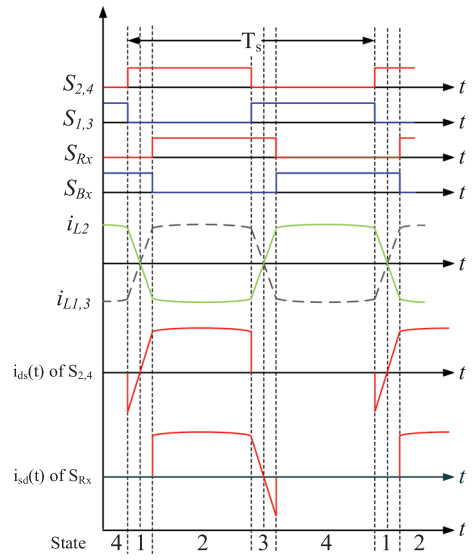

FIGURE 5. Waveforms of inductors and switching devices.

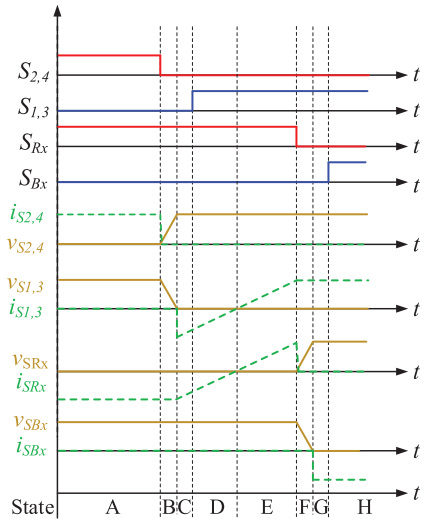

FIGURE 6. Commutation waveforms of ZVS operation.

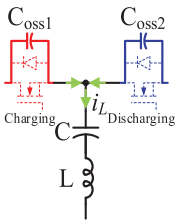

FIGURE 7. The circuit used to estimate the deadtime.

For a more detailed analysis, the current waveforms of all the components will be derived. The following assumptions have been made to simplify the analysis:

- All the switching devices in the analyzed circuit are ideal. Their dynamic switching behavior and on-state resistance are not considered in the analysis.
- Deadtime is not considered in this analysis.
- The parameters of all LC branches are identical. Thus, the current waveforms of all the LC tanks are the same.

In order to achieve ZVS on all of the switching devices, the switching frequency should be set to higher than the resonant frequency of the LC tank. This means the resonant circuit should operate at the inductive impedance region of the LC tank, as shown in (1).

$$f_s = \frac{1}{T_s} > \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

Here, L_r and C_r are the values of resonant inductor L_n and resonant capacitor C_n in the circuit, respectively. The f_s means switching frequency, and T_s represents the switching period.

Fig. 5 shows the switch and inductor current waveforms of the presented converter. For a half-switching cycle, when the red switches on the wing side turn on, the current waveform can be divided into two parts, which are state 1 and state 2 shown in Fig. 5. For the first part, the circuit is in the phase-shift state, which is state 1 in Fig. 5. The equivalent circuit of this state is shown in Fig. 4(a). During this state, the rectifier side devices S_{Bx} are conducting. And the drain-source current of the wing side devices S_2 and S_4 changes from negative to positive with slope V_{out}/L_r. This is because the voltage across the inductor L_3 is $V_{in} - V_{C3}$, where $V_{C3} = 3V_{out}$ and $V_{in} = 4V_{out}$. Note that the amplitude values of the positive part and the negative part of the current are the same in ideal case. For the second part, the circuit operates in non-phase-shift state, which is state 2 in Fig. 5. The equivalent circuit of this state can be found in Fig. 4(b). With the assumption that the switching frequency is much higher than the resonant frequency of the LC tank, the inductor and switch current waveforms during this state are part of the resonant current waveform that has the frequency of $1/(2\pi\sqrt{L_r C_r})$. It is worth mentioning that when the switching frequency is much higher than the resonant frequency, the current waveform in this state can be simplified to a straight line. Similarly, the components' current waveforms of equivalent circuits Fig. 4(c) and (d) correspond to the waveforms during state 3 and state 4 in Fig. 5, respectively.

B. ZVS OPERATION OF THE PRESENTED CONVERTER

The presented converter can operate in ZVS mode. By utilizing the resonant inductor in the resonant circuit, the phase-shift control enables ZVS on all the switching devices. In half a switching period, the detailed converter operation can be divided into eight states to show the realization of ZVS. Fig. 6 shows the detailed switching transient waveforms of the eight states, with the consideration of deadtime. The equivalent circuits of these eight states are shown in Fig. 8. Among which Fig. 8(a)∼(d) and Fig. 8(e)∼(h) show the ZVS realization of the wing side devices and rectifier side devices, respectively. Note that we assume the converter already reached the steady state in this study.

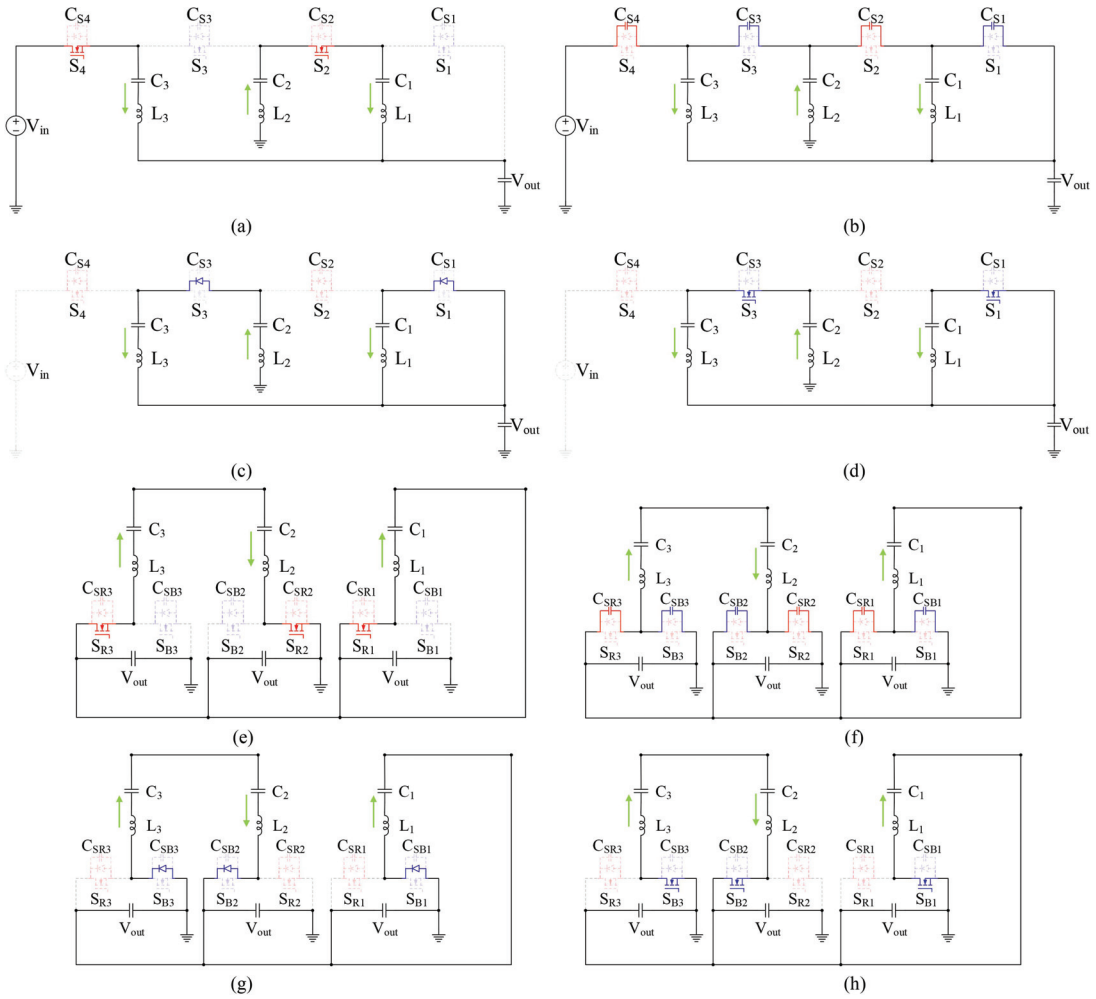

FIGURE 8. **Commutation states during half switching cycle.**

State A: In this state, MOSFETs S_2, S_4, and $S_{R1\text{-}3}$ are turned on. Capacitors C_1 and C_3 are charging while C_2 is discharging. The C_2 and the voltage source provide energy to the output during this state.

State B: MOSFETs S_2 and S_4 turn off at the beginning of this state. The inductor currents commute from S_2 and S_4 to the output capacitors of all the wing side switches. Therefore, the LC tanks will interact with the output capacitors of the MOSFETs on the wing side, which are C_{S1} to C_{S4}. The inductor currents discharge the MOSFETs' output capacitors C_{S1} and C_{S3}. And charge capacitors C_{S2} and C_{S4}. Note that after the switches' output capacitors are fully discharged, they will not be charged again during the deadtime.

State C: After the capacitors C_{S1} and C_{S3} are fully discharged, the corresponding device body diodes will kick in and keep the voltage across the devices equal to the diodes' forward voltage. During this state, all the inductor currents start reducing and approaching zero.

State D: MOSFETs S_1 and S_3 turn on at the beginning of this state. Because their output capacitors C_{S1} and C_{S3} are fully discharged in the previous state, the zero-voltage switching of these devices has been achieved. At the end of this state, all the inductor currents reach zero.

State E: In this state, all the inductor currents keep increasing in the other direction. The capacitors C_1 and C_3 are discharging and providing energy to the output, while C_2 is charging through C_1.

State F: At the beginning of this state, rectifier side MOSFETs $S_{R1}\sim S_{R3}$ turn off. The inductor currents commute from switches $S_{R1}\sim S_{R3}$ to all the rectifier side devices' output capacitors $C_{SR1}\sim C_{SR3}$ and $C_{SB1}\sim C_{SB3}$. The inductors will interact with all these capacitors to charge/discharge them. Thus, we can recycle the energy that is stored in the capacitors.

State G: Similar to state C, once the MOSFETs' output capacitors of $S_{B1}\sim S_{B3}$ are fully discharged, all the currents will commute to their body diodes. After that, the voltage across them is the diode forward voltage.

State H: MOSFETs $S_{B1}\sim S_{B3}$ turn on at the beginning of this state. Because the voltage across them is the same as their body-diode forward voltage, the ZVS of these devices has been achieved.

TABLE 1. Operating States and Capacitor Charging Balance

States	Capacitor Energy
A	C_1: ↑ C_2: ↓ C_3: ↑ $C_{S1,S3}$: → $C_{S2,S4}$: → C_{SRx}: → C_{SBx}: →
B	C_1: ↑ C_2: ↓ C_3: ↑ $C_{S1,S3}$: ↓ $C_{S2,S4}$: ↑ C_{SRx}: → C_{SBx}: →
C	C_1: ↑ C_2: ↓ C_3: ↑ $C_{S1,S3}$: → $C_{S2,S4}$: → C_{SRx}: → C_{SBx}: →
D	C_1: ↑ C_2: ↓ C_3: ↑ $C_{S1,S3}$: → $C_{S2,S4}$: → C_{SRx}: → C_{SBx}: →
E	C_1: ↓ C_2: ↑ C_3: ↓ $C_{S1,S3}$: → $C_{S2,S4}$: → C_{SRx}: → C_{SBx}: →
F	C_1: ↓ C_2: ↑ C_3: ↓ $C_{S1,S3}$: → $C_{S2,S4}$: → C_{SRx}: ↑ C_{SBx}: ↓
G	C_1: ↓ C_2: ↑ C_3: ↓ $C_{S1,S3}$: → $C_{S2,S4}$: → C_{SRx}: → C_{SBx}: →
H	C_1: ↓ C_2: ↑ C_3: ↓ $C_{S1,S3}$: → $C_{S2,S4}$: → C_{SRx}: → C_{SBx}: →

↑: Capacitor charging; ↓:Capacitor discharging; →: Capacitor energy unchange
S_{Rx}: rectifier-side red switches; S_{Bx}: rectifier-side blue switches.

So far, the ZVS mechanism is introduced in this section. It is worth mentioning that during the deadtime, the conduction of the body diodes will lead to considerable power loss. Therefore, the conduction time of the diodes should be minimized. Fig. 7 shows the circuit used to predict the deadtime. Assume the capacitances of the MOSFETs' output capacitors are C_{oss1} and C_{oss2} and the voltage stress of the two switches are V_{ds1} and V_{ds2}. In order to calculate the correct deadtime. The total charge stored in MOSFETs' output capacitors can be calculated with (2). Assuming the average inductor current during the deadtime is I_{L_avg}, the integral of the current over the deadtime should equal to the total charge stored in C_{oss1} and C_{oss2}, as shown in (3). Finally, the estimated deadtime could be calculated with (4).

It is worth emphasizing that the estimated deadtime may deviate from the actual optimal deadtime due to factors such as MOSFET switching transition and real-time converter operating condition (including the C_{oss} value variation due to the variation of the voltage across the device). Therefore, the estimation should be used to make sure the deadtime falls within the correct ballpark, and guide the hardware design. In practical application, synchronous rectifier ICs (such as APR349) can be used to determine when to turn on the switch by detecting the MOSFET's drain-source voltage. Besides, Table 1 shows all the capacitor energy information that corresponds to each state.

$$C_{oss1}V_{ds1} + C_{oss2}V_{ds2} = Q_{coss} \tag{2}$$

$$I_{L\_avg}t_{dead} = Q_{coss} \tag{3}$$

$$t_{dead} = \frac{C_{oss1}V_{ds1} + C_{oss2}V_{ds2}}{I_{L\_avg}} \tag{4}$$

III. RMS CURRENT OF THE SWITCHES IN THE CONVERTER

A. THE RMS VALUE OF THE CURRENT FLOWING THROUGH THE SWITCHING DEVICES

In order to calculate the RMS value of the current flowing through the switching devices, the average current flowing through them has to be figured out as the first step. According to the four operating states shown in Fig. 4, we can tell those 4 branches are providing power to the output. And the average currents flowing through all the switching are identical. Thus, the average current I_{sw_avg} flow through each device can be calculated according to the conversion ratio and the output current of the presented converter I_{out}. For the 4:1 converter, I_{sw_avg} is calculated in (5).

$$I_{sw\_avg} = \frac{I_{out}}{4} \tag{5}$$

In the general case, the average current flow through each switch in a converter with an *N:1* voltage conversion ratio can be calculated through (6). Where the P_{out} represents the output power of the converter, V_{out} represents the output voltage.

$$I_{sw\_avg} = \frac{I_{out}}{N} = \frac{P_{out}}{V_{out} * N} \tag{6}$$

According to (6), the average device current is a function of converter output current I_{out} and voltage conversion ratio N. On the other hand, by analyzing the switch current waveform shown in Fig. 5, one can tell that the average current during the phase-shift state is zero. This means the switch's average current value equals its average current value during the non-phase-shift state. Assume the phase-shift time is T_{shift} and the switching frequency is much higher than the resonant frequency, average value of the current flowing through each switching device can be reorganized, as shown in (7).

The next step is to figure out the current waveform of the switching devices. By plugging (6) into (7), the relationship between phase-shift time and other key parameters of the converter (switching frequency, resonant inductance, voltage conversion ratio, output voltage, output current) can be derived, as shown in (8). With the phase-shift time information, the devices' current waveform can be calculated. (9) shows the derived equation that represents the waveform of current flowing through wing-side switches S_2 and S_4. The current waveform shape of switches S_1 and S_3 is the same as that of S_2 and S_4. Similarly, the waveforms of the current flowing through all the rectifier side devices can also be derived. Furthermore, the waveform of the current flow through the LC tank is derived, which can be found in (10).

$$I_{sw\_avg} = \frac{V_{out}T_{shift}}{2T_sL_r} * \left(\frac{T_s}{2} - T_{shift}\right) \tag{7}$$

$$T_{shift} = \frac{T_s}{4} - \sqrt{\frac{T_s^2}{16} - T_s\frac{2I_{out}L_r}{N * V_{out}}} \tag{8}$$

$$i_{sw\_zvs}(t) = \begin{cases} -\left(\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}\right) + \frac{t}{\frac{L_r}{V_{out}}}, & 0 \le t \le T_{shift} \\ \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}, & T_{shift} \le t \le \frac{T_s}{2} \\ 0, & \frac{T_s}{2} \le t \le T_s \end{cases} \tag{9}$$

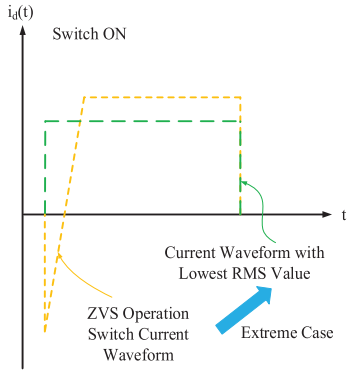

FIGURE 9. Two current waveforms that has the same average value.

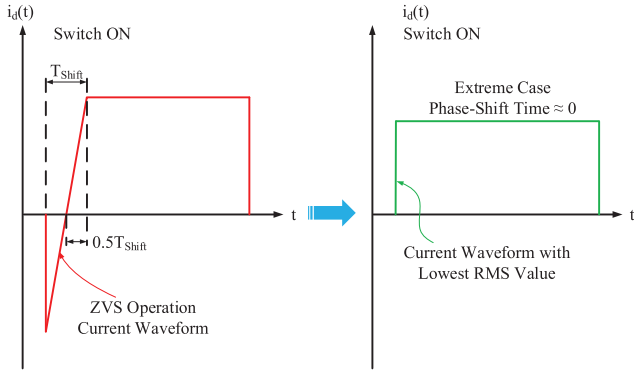

FIGURE 10. Switch current waveforms in ZVS operation.

$$i_{L\_zvs}(t) = \begin{cases} -\left(\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}\right) + \frac{t}{\frac{L_r}{V_{out}}}, & 0 \le t \le T_{shift} \\ \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}, & T_{shift} \le t \le \frac{T_s}{2} \\ \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2} - \frac{t-0.5T_s}{\frac{L_r}{V_{out}}}, & \frac{T_s}{2} \le t \le T_s + T_{shift} \\ -\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}, & T_s + T_{shift} \le t \le T_s \end{cases} \tag{10}$$

Finally, with the switch current waveform derived in (9), the RMS value of the current flow through the switching devices can be calculated using (11). Note that all the switching devices in the presented circuit have the same $I_{sw\_zvs\_rms}$ value.

$$I_{sw\_zvs\_rms} = \sqrt{\frac{1}{T_s}\left[\int_0^{T_{shift}}\left(\frac{t}{\frac{L_r}{V_{out}}} - \frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}\right)^2 dt + \int_{T_{shift}}^{0.5T_s}\left(\frac{1}{\frac{L_r}{V_{out}}} * \frac{T_{shift}}{2}\right)^2 dt\right]} \tag{11}$$

B. THE LOWEST VALUE OF THE RMS CURRENT

According to (11), we can easily conclude that the devices' RMS current in ZVS operation is not only related to the output current I_{out} and voltage conversion ratio of the converter N, but also depends on switching period T_s, phase-shift time T_{shift}, and the value of L_r/V_{out}. By plugging (8) into (11), the the factor T_{shift} will be canceled out. And leaving four factors that are related to the devices' RMS current, which are I_{out}, N, T_s and L_r/V_{out}.

In order to analyze the RMS value range of the switch current when the presented converter has a certain output current value, the square shape current waveform is analyzed at first. There are two reasons for doing this. First, we assume the two different current waveforms shown in Fig. 9 have the same average value within a certain period. The RMS value of the square shape current waveform is the lowest, which will be verified in the following analysis. Second, in the ideal case, the device's current waveform could be infinitely close to a square shape when the di/dt of the current waveform during the phase-shift state is very high, as shown in Fig. 10. Note

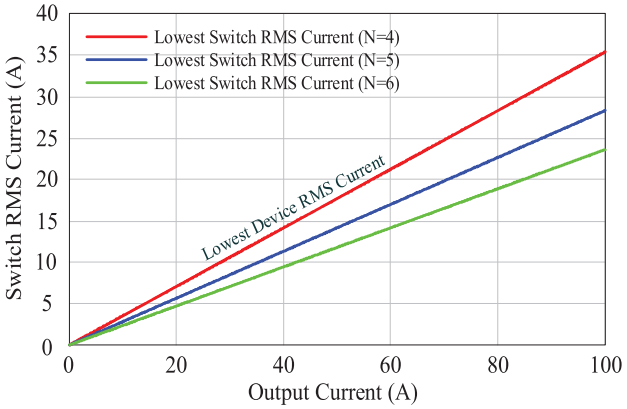

FIGURE 11. Theoretical lowest RMS current value of switching device.

that the switch current waveform cannot be a square shape since the phase-shift time is a non-zero value.

$$i_{square}(t) = \begin{cases} \frac{2I_{out}}{N}, & 0 \le t \le \frac{T_s}{2} \\ 0, & \frac{T_s}{2} \le t \le T_s \end{cases} \tag{12}$$

$$I_{sw\_square\_rms} = \frac{\sqrt{2}I_{out}}{N} \tag{13}$$

Assuming all the switching devices in the converter have a square current waveform when the converter operates at steady-state, then the switch current waveform can be derived accordingly, as shown in (12). We can tell that the magnitude of the square waveform is a function of the converter output current and voltage conversion ratio. And (13) calculates the RMS value of the square shape current waveform.

With the same converter output current, the calculation based on (11) and (13) shows that $I_{sw\_zvs\_rms}$ is always higher than $I_{sw\_square\_rms}$ as long as the phase-shift time is not zero. This means the RMS value of the square waveform is theoretically the lowest boundary of switch RMS current in ZVS operation. In Fig. 11, the lowest values of switch RMS current for converters that have different voltage conversion ratio is demonstrated. Because the switching devices' RMS current is directly related to their conduction loss, the presented converter with ZVS operation has the potential to achieve superior

TABLE 2. Basic Converter Specification Used in the Design Example

Description	Items	Values
Voltage Conversion Ratio	N	4
Typical Input Voltage	V_{in}	48 V
Typical Output Voltage	V_{out}	12 V
Typical Output Power	P_{out_typ}	450 W
Typical Output Current	I_{out_typ}	37.5 A
Peak Output Power	P_{out_max}	600 W
Peak Output Current	I_{out_max}	50 A

efficiency. Therefore, a comprehensive analysis of converter parameters for ZVS operation is very meaningful. And the design procedure will be provided in the following section.

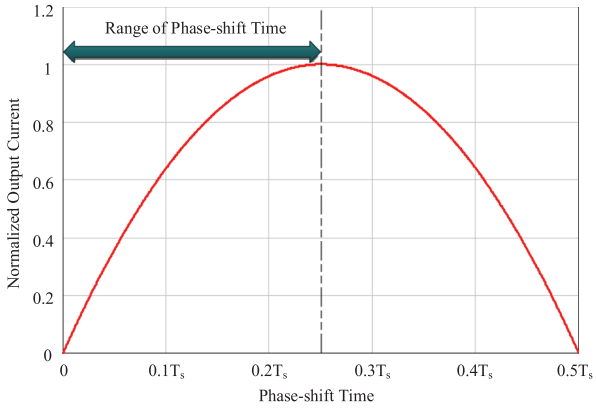

FIGURE 12. Relationship between the phase-shift time and converter normalized output current.

IV. ANALYSIS AND DESIGN OF A 48 V–12 V CONVERTER

The ZVS and low switch RMS current features are enabled by the phase-shift control method. In order to fully leverage these advantages brought by the phase-shift control, this section shows how to properly select the component parameters for the presented converter.

In Table 2, the basic converter specification in this design example is provided. In this design, the 4x modular multilevel resonant DC-DC converter with 48 V input and 12 V output will be analyzed and designed. The typical and maximum output power of the converter is 450 W and 600 W, respectively. And the output current capability of the converter is 50 A. It is worth mentioning that the specification of this converter is a representative specification of an intermediate bus converter that is used in data center applications. And we can tell that the converter has low voltage and high current output.

Based on the information obtained from previous analysis and the converter specification, three essential aspects need to be considered in terms of the converter design. The first is the phase-shift time of the control signals. The second is the switching frequency of the switching devices. The third is the inductance value of resonant inductors in the circuit.

The design procedure is divided into three parts. The part-one focuses on preliminarily determining the key parameters of the converter and making sure it has enough power delivery capability. The part-two focuses on the further selection of the converter parameters so that the converter can achieve superior performance. At last, the control algorism is briefly introduced.

A. DESIGN CONSTRAINTS ON CONVERTER OUTPUT POWER

Because the ultimate goal of the phase-shift control method is to control the output current of the converter by adjusting the phase-shift time, there is no doubt that the determination of the key parameters, which are T_{shift}, f_s and L_r, need to ensure the designed converter can deliver enough power to the output.

The first step of the design procedure is to find the relationship between the converter output current and phase-shift time. According to (5), when the converter delivers maximum current within its output current capability, the average value of current flow through switching devices is maximum. Therefore, when the derivative of the switch average current shown in (7) equals zero, the phase-shift time that allows the converter generates the maximum output current can be found, as shown in (14). As a result, when the phase-shift time T_{shift} equals to 1/4 of the switching period T_s, the presented converter has the highest output current. With this information, we use the maximum converter output current as the base value, and the relationship between the normalized output current and phase-shift time can be calculated using (15). Fig. 12 shows the calculated results. When $0 < T_{shift} < 0.25T_s$, the converter's output current capability increases as the increase of phase-shift time. On the other hand, when $0.25T_s < T_{shift} < 0.5T_s$, the converter's output current capability and phase-shift time have a negative relationship. This means for a certain output current value, there are two corresponding phase-shift times. According to the previous analysis, short T_{shift} allows the the switches have low RMS current. As a result, to allow the converter to achieve the best performance, the range of phase-shift time should vary from 0 to $0.25T_s$.

$$dI_{sw\_avg}/dT_{shift} = 0 \tag{14}$$

$$I_{sw\_avg\_nom} = \frac{16T_{shift}}{T_s^2} * \left(\frac{T_s}{2} - T_{shift}\right) \tag{15}$$

With the information that the presented converter generates the highest output current within its current output capability when $T_{shift} = 0.25T_s$, the next step is to find out the relationship between switching frequency and the output current capability of the converter. By plugging $T_{shift} = 0.25T_s$ into (7), we can derive the maximum average current flow through each switching device under different conditions, which is shown in (16). Consequently, the output current capability of the converter can be calculated using (17). We can tell that the converter's maximum output current is a function of input voltage, switching frequency, and resonant inductance. Fig. 13

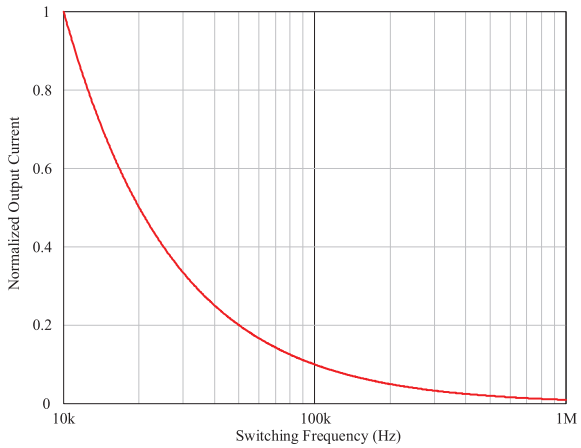

FIGURE 13. Relationship between the switching frequency and normalized converter output current.

shows the converter's normalized output current capability when the switching frequency sweep from 10 kHz to 1 MHz. In this normalization, the base value is the converter's maximum output current when it operates at 10 kHz. Note that the normalized output current is only a function of switching frequency. We can tell that the converter's normalized output current capability drops significantly as the increase of switching frequency at the low-frequency range. In other words, the maximum output current is very sensitive to the switching frequency at low frequency (e.g., less than 100 kHz). To be specific, the converter's output current capability decreases by 90% when the operating frequency of the converter increases from 10 kHz to 100 kHz. However, from 100 kHz to 1 MHz, the change of the converter's output current capability is less than 10%. Although low switching frequency enables the high output current capability of the converter, it requires a large volume of passive components. And for an intermediate bus converter, power density is a very important factor. Therefore, a high switching frequency is preferred in this design example.

$$I_{sw\_avg(max)} = \frac{V_{out}}{32 f_s L_r} \tag{16}$$

$$I_{out(max)} = \frac{N * V_{out}}{32 f_s L_r} = \frac{V_{in}}{32 f_s L_r} \tag{17}$$

Finally, the inductance of the resonant inductor needs to be properly selected to allow the converter has sufficient power delivery capability. It's worth mentioning that the inductors whose inductance values are within a few hundreds of nanohenry have been proven to be good choices in the intermediate bus converter design [35] because they have the potential to allow the converters to achieve both high power density and high efficiency at the same time. Therefore, we start from the off-the-shelf inductors shown in Table 3, whose inductance values are 36 nH, 50 nH, and 70 nH. In order to broaden the range of inductance in this analysis, we also assume that a customized 18 nH inductor can be used in the design. In Fig. 14, the four inductance values are evaluated.

TABLE 3. Inductor Candidates Used in the Design

Part Number	Values
Customized Design	18nH
SLC7649S-360KL	36nH
SLC7649S-500KL	50nH
SLC7649S-700KL	70nH

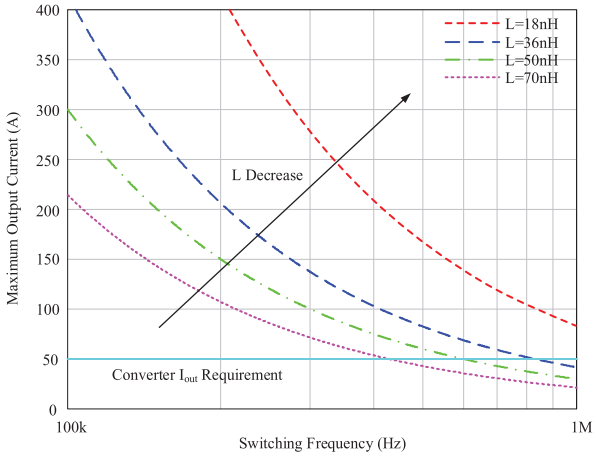

FIGURE 14. Maximum converter output current in terms of switching frequency and resonant inductance.

TABLE 4. Relationship Between Resonant Inductance and Switching Frequency

Resonant Inductance Value	Maximum Switching Frequency
18 nH	>1 MHz
36 nH	831 kHz
50 nH	606 kHz
70 nH	431 kHz

With a certain operating frequency, the converter's output current capability is significantly increased as the inductance value decreases. To meet the converter's output current requirement, Table 4 shows that the 18 nH inductor allows the converter operates at higher than 1 MHz, while the maximum switching frequency of the converter using 36 nH, 50 nH, and 70 nH inductors are limited to 831 kHz, 606 kHz, and 431 kHz, respectively.

B. CONVERTER PARAMETER DETERMINATION AND DISCUSSION

In addition to making sure that T_{shift}, f_s and L_r allow the converter to have enough power delivery capability, some other design criteria need to be further analyzed to achieve the optimized design. As we have emphasized that in the low voltage high current output application, one of the major power loss contributors is semiconductor conduction loss, the primary goal of the optimum design is to achieve low device RMS current in the ZVS operation.

According to (8) and (11), we can tell that the switch RMS current is a function of I_{out}, N, T_s, L_r, and V_{out}. With the given

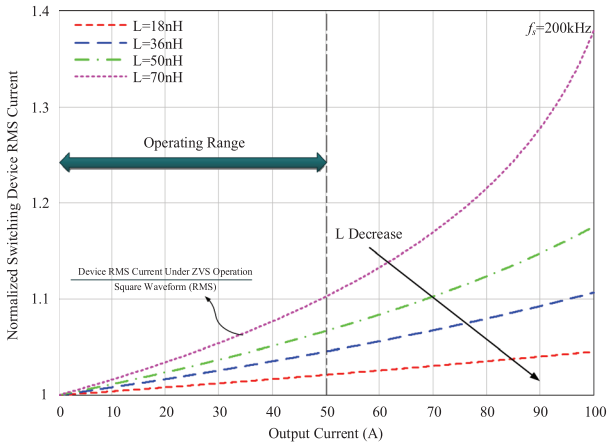

FIGURE 15. Normalized switching device RMS current when different resonant inductance values are used (f_s = 200 k).

L_r and T_s values of the 48–12 V converter, the switch RMS current can be calculated. In order to evaluate the effect of inductance value on the RMS value of switch current, here we use the $T_s = 5\ \mu$s in the evaluation. Then four inductance values shown in Table 4 are used to calculate the normalized switching device RMS current values. Here we define the normalized switching device RMS current as follows:

$$i_{sw\_zvs\_norm}\left(V_{out}, I_{out}, L_r, f_s\right) = \frac{i_{sw\_zvs\_rms}\left(V_{out}, I_{out}, L_r, f_s\right)}{i_{sw\_square\_rms}\left(I_{out}\right)} \tag{18}$$

In (18), the base value used in the normalization is the RMS value of the square current waveform, which is represented by $i_{sw\_suqare\_rms}$. And the RMS values of current flowing through switching devices in the converter are represented by $i_{sw\_zvs\_rms}$.

According to Fig. 15, as the increase of converter output current, a lower inductance value allows the switching devices in the converter to have a lower RMS current value due to the higher di/dt of the switch current during the phase-shift state. To maintain low conduction loss of the switching devices, the normalized switching device current ranges from 1 to 1.1 over the whole operating range is desired in this design. Hence, 70nH resonant inductance will not be considered among the four inductance values. However, it is worth mentioning that the resonant inductance cannot be too small due to two reasons. First, although the low resonant inductance can make sure the high output current capability as well as low device conduction loss, the inductance value cannot be too low so that the inductor has enough energy to charge and discharge the MOSFETs' output capacitors. In other words, a proper inductance value needs to be selected to achieve a reasonable low semiconductor RMS current and soft-switching at the same time. Second, the small inductance will create challenges for the controller because high-resolution PWM signals and very fine phase-shift time are required. With all the aforementioned considerations, the selected resonant inductance is 50nH when the switching frequency is 200 kHz.

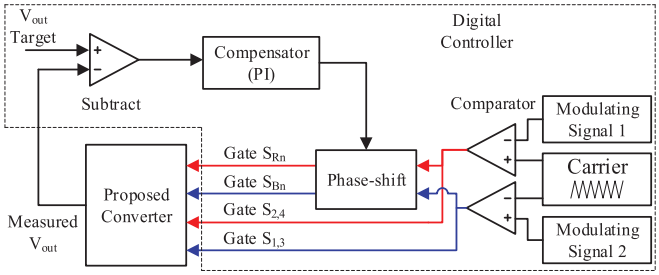

FIGURE 16. Control algorithm of the proposed converter.

TABLE 5. Parameters Used in the Simulation and Experiments

Items	Symbols	Values
Typical input voltage	V_{in}	48 V
Typical output voltage	V_{out}	12 V
Switching Frequency	f_s	200 kHz
Resonant Inductance	L_r	50 nH
Resonant Capacitance	C_r	120 uF
Maxumum Output Power	P_{out_max}	600 W
On-state Resistance– S_1, S_4, S_{Rn}, S_{Bn}	R_{ds_on1}	1.3 mOhm
Output Capacitance – S_1, S_4, S_{Rn}, S_{Bn}	C_{oss1}	900 pF
On-state Resistance - S_2, S_3	R_{ds_on2}	1.5 mOhm
Output Capacitance - S_2, S_3	C_{oss2}	600 pF

C. CONTROL ALGORISM

By adjusting the phase-shift time, the proposed converter can achieve output voltage regulation. However, the voltage regulation function comes at a price of reduced efficiency. So, the main goal of the voltage regulation is to maintain a 4:1 voltage conversion ratio in this design. Fig. 16 shows the control block diagram of the proposed converter. Here the deadtime can be adjusted by shifting the modulation signals up and down in reference to the carrier signal. The phase-shift time will be generated according to the error between the target output voltage and the actual output voltage. Then applied to the synchronous rectifier gate control signals.

Because the controller design needs the dynamic performance of the converter and controller hardware capability to be well considered, a more detailed control circuit analysis will not be covered in this paper.

V. SIMULATION AND EXPERIMENTAL RESULTS

Both simulations and experiments have been performed to verify the analytical analysis and operation of the presented converter. Table 5 shows all the critical parameters that are used in this section. The operating frequency of the converter is 200 kHz, the inductance of the inductor is 50 nH, and the capacitance used in the resonant tank is 120 uF which is aligned with the determined value from the previous section. The parameters of the switching devices are based on Infineon 25 V and 30 V OptiMOS devices, which are also used to build the lab prototype. It is worth mentioning that, the main purpose of the prototype is to validate the converter design methodology.

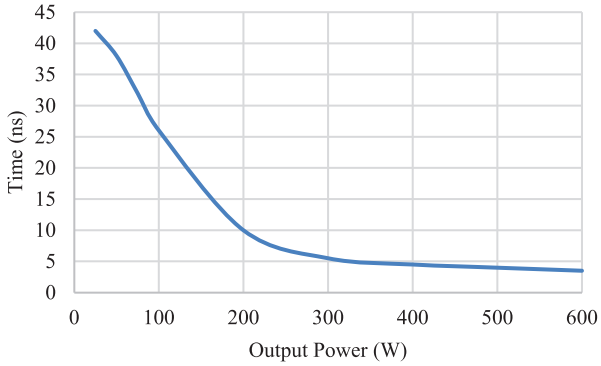

FIGURE 17. Deadtime required to complete ZVS operation.

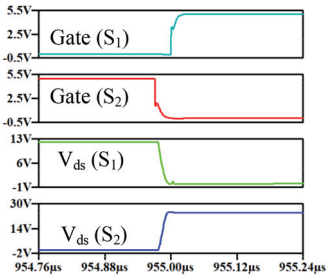

FIGURE 18. Simulated waveforms when P_{out} = 100 W with 30 ns deadtime.

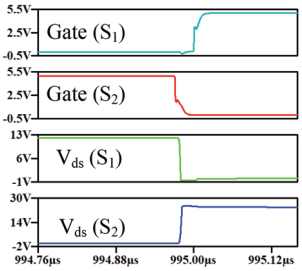

FIGURE 19. Simulated waveforms when P_{out} = 600 W with 30 ns deadtime.

To avoid complexity, we keep the hardware design simplified and used a fixed deadtime in the experiments, which is 30 ns. Fig. 17 shows the deadtime required to finish the ZVS operation, which is the simulated result based on the SPICE model. Fig. 18 and Fig. 19 show the simulation results for the converter operating with 30 ns deadtime at 100 W and 600 W, respectively. The impact of the longer deadtime will result in higher conduction loss on the diode during the deadtime under heavy load conditions.

A 48 V-12 V lab prototype has been built to verify the operation of the presented converter. Table 6 illustrates the actual parts and their part numbers that are used in the lab prototype. Fig. 20 shows the top view of the prototype that is used to verify the theoretical analysis. All the switching devices and resonant inductors are placed on the top side of the board. Fig. 21 shows the bottom side of the lab prototype, where all the gate driving circuits are located on this side. The area of

TABLE 6. Parts Used in the Prototype

Items	Part#
Switching devices	BSZ013NE2LS5I BSZ0500NSI
Gate Driver	LMG1205
Resonant Inductor	SLC7649S-500
Resonant Capacitor	GRM32EC72A106KE05
Micro-controller	TMS320F28335
Level-shifter	ADUM6200CRWZ

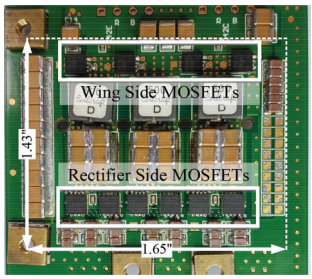

FIGURE 20. Top view of lab prototype with 4:1 voltage conversion ratio.

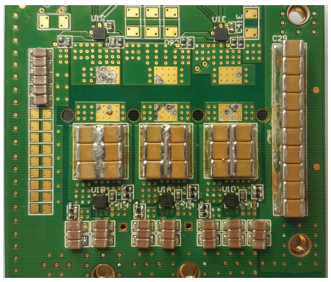

FIGURE 21. Bottom view of lab prototype with 4:1 voltage conversion ratio.

TABLE 7. Dimentsion of the Lab Prototype

Items	Value	Unit
High	0.32	Inch
Length	1.65	Inch
Weigth	1.43	Inch
Maximum Power	600	W
Power Density @ Max Power	795	W/in^3

the active power circuit is 1.43 inches × 1.65 inches, and the height of the converter is 0.32 inches. Therefore, the proposed converter can achieve 795 W/in^3 density, as summarized in Table 7. The power density of this prototype is slightly higher than the switched-tank converter presented in [35].

Three operating points are measured and simulated in this section. First, a 25 W case is simulated to show that when the output power of the converter is not high enough, the C_{oss} of MOSFETs cannot be fully discharged to achieve ZVS operation. Second, a 50 W load operation has been evaluated. This operating point is the boundary condition where all the MOSFETs are about to achieve the ZVS operation. Third, the

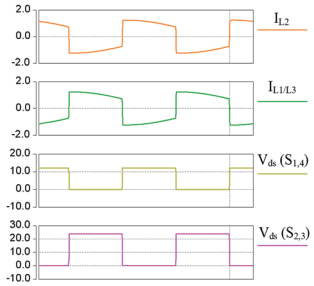

FIGURE 22. Simulated waveforms when P_{out} = 25 W.

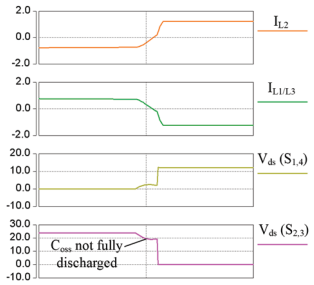

FIGURE 23. ZVS is not achieved when P_{out} = 25 W.

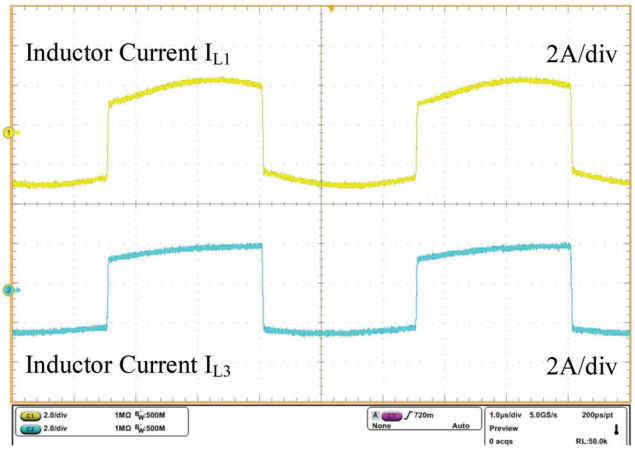

FIGURE 24. Inductor current waveforms when V_{in} = 48 V, V_{out} = 12 V, P_{out} = 50 W.

heavy load is evaluated to verify the theoretical RMS current calculation and the ZVS operation as well.

It is worth emphasizing that there are 2 main purposes for providing the simulation results in this section:

- Verify the correctness of the simulation model by comparing the simulated results with the experimental results
- Use simulated waveforms as a supplement to experimental waveforms due to the limited measurement compatibility of the prototype

Fig. 22 and Fig. 23 show the simulated waveforms of the presented converter delivering 25 W power. At this load condition, the energy stored in the inductor is very limited. Therefore, the MOSFETs' C_{oss} cannot be fully discharged, and ZVS is not achieved. Fig. 24 shows the inductor current

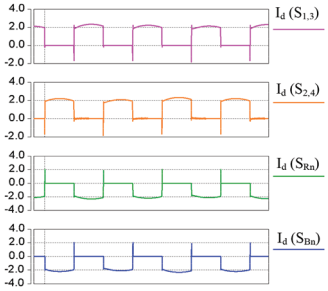

FIGURE 25. Simulated MOSFETs' current waveforms when P_{out} = 50 W.

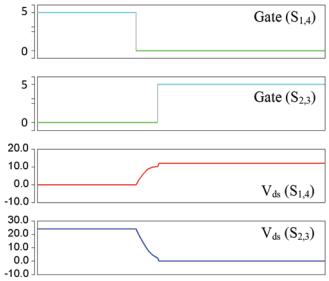

FIGURE 26. Simulated ZVS waveforms of converter when P_{out} = 50 W.

waveforms of L_1 and L_3 when the presented converter outputs 50 W power. The current waveforms are very close to the square shape. Note that due to the challenge of measuring switching devices' current waveforms, inductor current waveforms are measured instead to verify the RMS current calculation. And the Rogowski current transducers are used for the measurement. The RMS values of I_{L1} and I_{L3} are 2.12 A and 2 A, respectively. All the current values are aligned with the calculated values very well. Fig. 25 shows the simulated current waveforms of switching devices in the converter. The shape of the waveforms matches the experimental waveforms. The RMS value of the switch current is 1.49 A.

Furthermore, the boundary of the converter's ZVS operation has been found through simulations and experiments. Fig. 26 shows the simulated results that all the MOSFETs are about to achieve ZVS at this operating point. According to the experimental results shown in Fig. 27, we can also tell the drain-source voltage reaches a very low level before the MOSFET is turned on, which is aligned with the simulated waveforms. Therefore, the ZVS operation can be achieved when the converter's load is between 50 W–70 W.

In Fig. 28, the current waveforms of inductors L_1 and L_3 are demonstrated under heavy load conditions. Due to the limitation of the DC electronic load resolution capability, we have tested the prototype at 550 W output here. According to the measured waveforms, their RMS values are 24.37 A and 23.8 A, respectively. And the calculated value is 24.3 A. For better comparison, the two inductor current waveforms are overlapped each other to show that the current flow through all the resonant branches is almost balanced. Similarly, Fig. 29 shows the MOSFETs' current waveforms at 550 W load. The simulated RMS value of current flow through all the switching

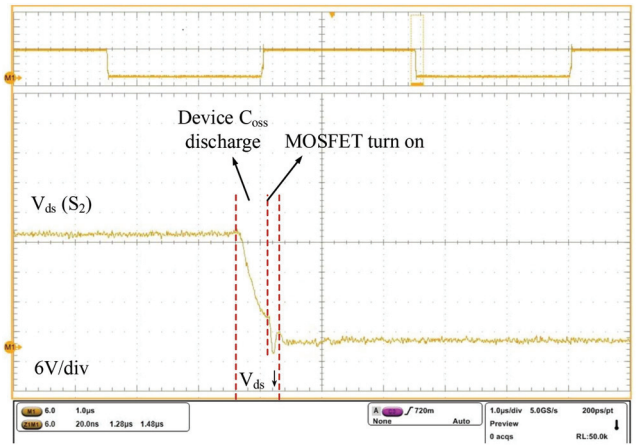

FIGURE 27. Switch achieves ZVS at 50 W Output.

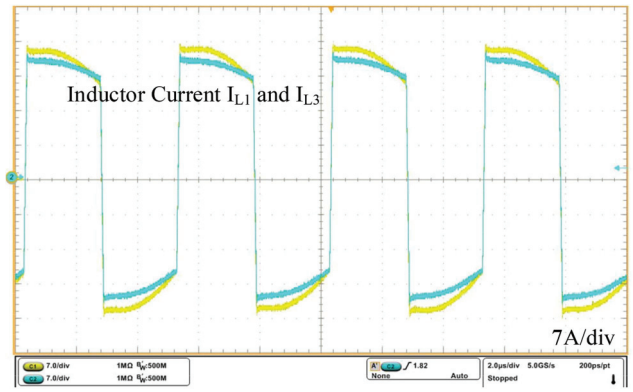

FIGURE 28. Inductor current waveforms when V_{in} = 48 V, V_{out} = 12 V, P_{out} = 550 W.

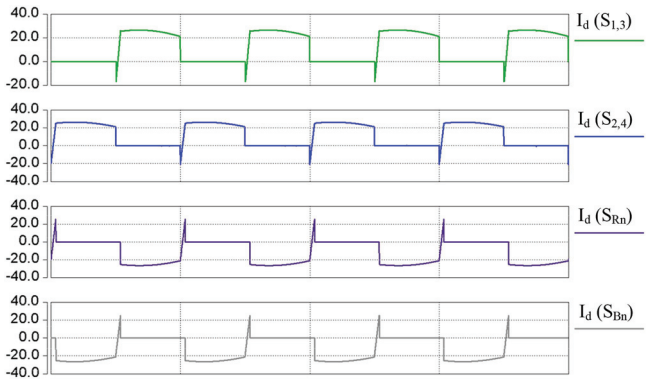

FIGURE 29. MOSFETs' current waveforms when P_{out} = 550 W.

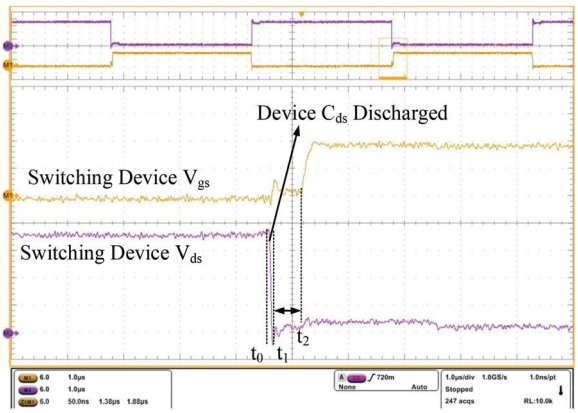

FIGURE 30. ZVS operation V_{in} = 48 V, V_{out} = 12 V, P_{out} = 550 W.

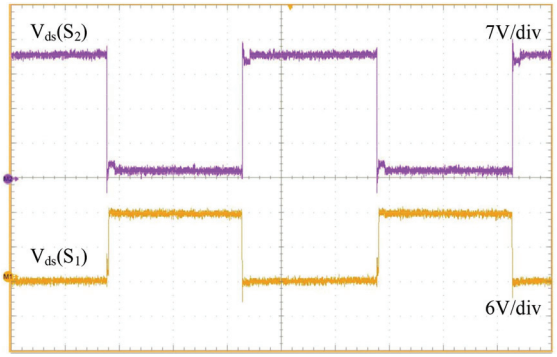

FIGURE 31. Voltage waveforms of the switching devices.

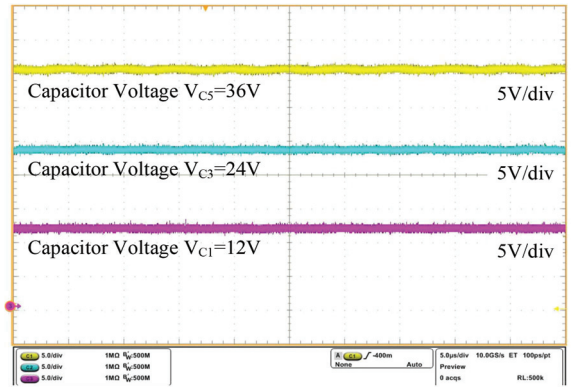

FIGURE 32. Capacitor voltage waveforms when V_{in} = 48 V, V_{out} = 12 V, P_{out} = 550 W.

devices is 17.26 A. And the calculated value is 17.18 A. We can tell that the simulated converter's switch RMS current values matches the theoretical analysis.

The ZVS operation is validated at this operating point as well. In Fig. 30, the MOSFET's drain-source voltage decrease at t_0, and the corresponding V_{gs} remains low at this time, which indicates the MOSFET's output capacitor has been discharged by the resonant inductor. At time t_1, the current commutes to the body diode when the MOSFET's output capacitor is fully discharged. Between t_1 and t_2, the MOSFET's body-diode is conducting. At time t_2, the MOSFET's gate-source voltage starts rising, and the switch turns on in a short time. As a result, the ZVS of the device has been achieved.

In Fig. 31, the voltage waveforms of switches S_1 and S_2 are provided. We can conclude that the voltage stress of S_2 and S_3 is 24 V, while all the other switches' stress is 12 V. Fig. 32, the voltage across capacitors C_1, C_2, and C_3 are

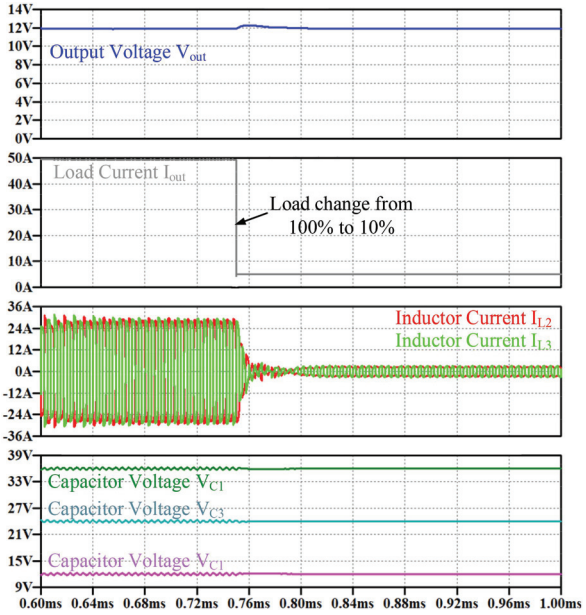

FIGURE 33. Dynamic performance of the proposed 4:1 converter.

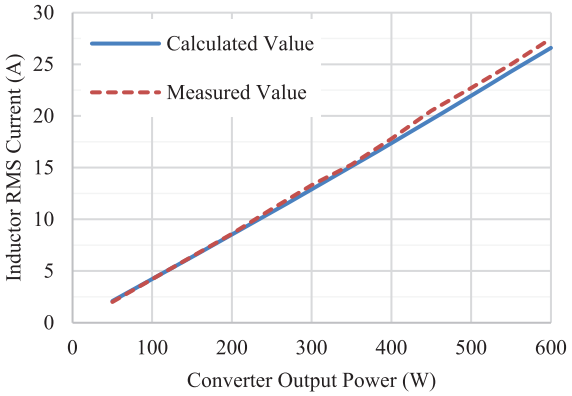

FIGURE 34. Calculated RMS current and experimental measured results.

measured, which are 12 V, 24 V, and 36 V, respectively. The results match the theoretical analysis. In Fig. 33, the dynamic performance of the proposed converter is demonstrated. we can tell that when the load changes from 100% to 10%, the converter output voltage can be regulated within 30 μs. While the inductor current takes about 60 μs to become stabilized. And the voltages across resonant capacitors are always very stable.

In order to validate the mathematical model that is used to estimate the theoretical RMS value of the devices' current within the whole load range, Fig. 34 shows the comparison between the calculated inductor current RMS value and the experimental results. The comparison shows that the discrepancy between the two curves is within 5% of the calculated curve. Fig. 35 shows the thermal performance of the presented converter. When the converter outputs 550 W power, the hottest components on the board are the resonant inductors.

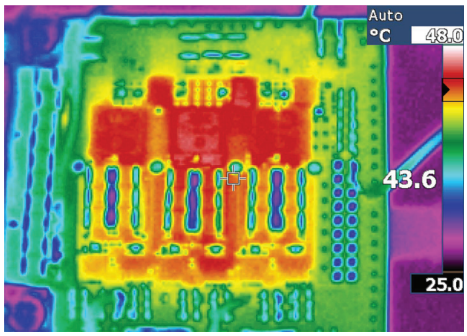

FIGURE 35. Thermal performance when V_{in} = 48 V, V_{out} = 12 V, P_{out} = 550 W.

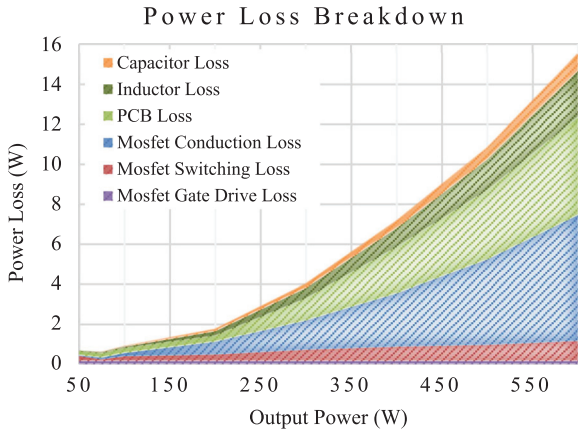

FIGURE 36. Power loss breakdown of the presented converter.

When there is no active cooling used for the prototype, the inductor temperature is 46 °C.

A power loss breakdown is performed to help better understand the power loss distribution and future improvement direction of the proposed converter, as shown in Fig. 36. It is worth mentioning that the ZVS is partially achieved when the load is light, and the C_{oss} loss takes majority part of the MOSFET switching loss. As the increase of converter output power, the converter's switching loss reaches the minimum level when the ZVS is fully achieved and the MOSETs' turn-off loss is not high as well. Under heavy load conditions, the MOSFET conduction loss and PCB loss are the majority losses. Note that the PCB loss is estimated using finite element analysis (FEA) software, which is similar to [41].

In addition, a comparison is performed to highlight the advantage of the proposed converter. Fig. 37 shows the efficiency of the presented converter. Its peak efficiency can reach as high as 99.55% when the gate drive loss is not included in the total loss. If gate drive loss is considered, the prototype reaches 99.35% peak efficiency. Under the nominal and maximum load, it achieves 98.07% and 97.5% efficiency, respectively. When compared with the other state-of-the-art works [42], [43], [44], the proposed converter has a great advantage in terms of efficiency under the light load condition. Table 8 shows a more comprehensive comparative study. The

TABLE 8. Comparison With State-of-the-Art 48-12 V Converters

Reference	Max Power	Soft-Switching	Switch Count	Passive Component Count	Isolated	Efficiency (Peak/Full load)
Proposed	600W	ZVS	10	6	N	99.35% / 97.5%
[36]	450w	ZCS	10	5	N	98.61% / 97.41%
[45]	120W	ZVS on part of the switches	8	5	N	98.6% / 98%
[46]	720W	ZVS	16	8	N	99% / 97.23%
[12]	720W	N/A*	10	5	N	96.2% / 95.7%
[47]	840W	N/A*	24	10	N	99.3% / 97.2%
[48]	900W	ZVS	12	4	Y	98.4% / 98%
[49]	500	ZVS + ZCS	8	2	Y	97.8% / 97.4%
[50]	450	ZVS	8	1	Y	96.2% / 95.7%

* N/A means no soft-switching is implemented in the converter.

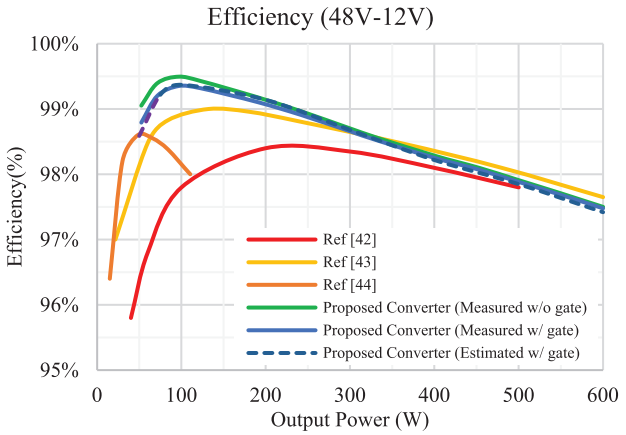

FIGURE 37. Measured efficiency of the presented converter.

study shows that both the switching device and the passive component usage in the proposed converter are very low. And the proposed converter achieves superior performance that is similar to all the other top-tier converters [12], [45], [46], [47], [48], [49], [50].

VI. CONCLUSION

A high-efficiency modular multilevel resonant DC-DC converter, as well as its design methodology, have been proposed in this paper. The basic operating principle and the ZVS operation of the presented circuit are demonstrated. A mathematical analysis of the components' RMS current is performed in this paper. A 48 V to 12 V converter design example shows the design constraints based on the given converter specifications. With the design constraints, detailed design procedures that ensure the high-efficiency operation of the proposed converter are presented. Based on the designed converter parameters, a lab prototype has been built to verify the effectiveness of the presented design method and the operation of the presented converter. Both light load and full load tests are carried out to verify the theoretically calculated RMS current values. The measured RMS values of device currents match with the theoretical calculation, with higher than 95% accuracy. The ZVS operation is verified through the experiments as well. The measured peak efficiency is 99.35% when gate drive loss is considered. And its power density can achieve 795 W/in^3.

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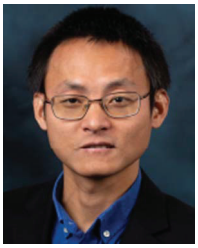

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